Texas Instruments

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Linear Circuits

Data Conversion, DSP Analog Interface, and Video Interface

Data Book

Volume 2

1992

Linear Products

Linear Products Quick Reference Guide

Data Book	Contents	Document No.
• Optoelectronics and Image Sensors	Optocouplers CCD Image Sensors and Support Phototransistors IR-Emitting Diodes Hybrid Displays	SOYD002A, 1990
• Speech System Manuals	TSP50C4X Family TSP50C10/11 Synthesizer TSP53C30 Synthesizer	SPSS010, 1990 SPSS011, 1990 SPSV006, 1991
• Interface Circuits	Data Transmission and Control Circuits, Peripheral Drivers/Power Actuators, Display Drivers	SLYD006, 1991
• Telecommunications Circuits	Transmission, Switching, Subscriber, Transient Suppressors	SCTD001B, 1991
• Linear and Interface Circuits Applications	Op Amps/Comparators, Video Amps, VRegs, Power Supply Design, Timers, Display Drivers, Datran, Peripheral Drivers, Data Acq., Special Functions	SLYA005, 1991
• Mass Storage ICs Designer's Reference Guide	Disk Drivers: Read/Write, Servo/System Control, Interface/Linear, Digital ASIC, LinASIC™, Applications	SSCA001, 1992
• Macromodel Data Manual	Level I: Operational Amplifiers, Voltage Comparators, Building Blocks Level II: Selected Operational Amplifiers, Buildilng Blocks	SLOS047B, 1992

January 1992

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Linear Circuits Data Book 1992

Volume 2
Data Conversion, DSP Analog Interface, and Video Interface

TEXAS INSTRUMENTS

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INTRODUCTION

Texas Instruments offers an extensive line of industry-standard integrated circuits designed to provide highly reliable circuits for peripheral support applications of microprocessor-based systems, DSP (digital signal processing) related analog interfaces, video interfaces, video and high-speed converters, digitizing requirements that demand ADC and DAC conversion, and general-purpose functions.

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This data book (Volume 2 of 3) provides information on the following types of products.

- Single-Slope and Dual-Slope Analog-to-Digital Converters (ADC)
- Successive-Approximation Semi-Flash, and Flash ADC Converters
- Current Multiplying and Video DAC Converters
- High-Speed Converters for Control Applications
- Color Palette Chips for Computer Graphics
- Analog Interface Circuits for DSP Interface
- Analog Switches and Multiplexers
- Switched-Capacitor Filter ICs
- Other General-Purpose Functions

These products cover the requirments of PC and workstation multimedia applications such as audio, graphics, communication applications, modems and cellular phones, video capture and image processing, industrial control and disk-drive servo-loop control, automotive, electronic instrumentaion, consumer, digital audio and any DSP or microprocessor-based system. New surface-mount packages (8-to-28 leads) include both ceramic and plastic chip carriers, and the small-outline (D) plastic packages that optimize board density with minimum impact on power-dissipation capability. Test equipment with handlers and automated assembly bonders strengthen the production capabilities to provide a lower cost-to-performance ratio. TI continues to enhance quality and reliability of integrated circuits by improving materials, processes, test methods, and test equipment. In addition, specifications and programs are contiuously updated. Quality and performance are monitored throughout all phases of manufacturing.

The alphanumeric listing in this data book includes all devices contained in Volumes 1, 2, and 3. Products in this book are shown in **BOLD** type. Thus, the reader can easily find the particular volume for a given device. Also included are those new products added to this volume as indicated by a dagger(†). The selection guide includes a functional description of each device by providing key parametric information and packaging options. Ordering information and mechanical data are in the last section of the book.

Complete technical data for all TI semiconductor products are available from your nearest TI Field Sales Office, local authorized TI distributor, or by writing directly to:

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We sincerely feel that this new 1992 Linear Circuits Data Book, Volume 2, will be a significant addition to your technical literature from Texas Instruments.

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†New devices added to this volume.

single-slope and dual-slope A/D converters

CONVERSION FUNCTION	RESOLUTION	SPEED (ms)	TYPE	PACKAGE	PAGE NO.
Dual-Slope A/D with BCD Output	4 1/2 Digits	34	TLC7135 ICL7135	FN, N	2–59
Dual-Slope Analog Processors	4 1/2 Digits	80	TL500	DW, J	2–77
	3 1/2 Digits		TL501		
Digital Processors With Seven-Segment Outputs	4 1/2 Digits		TL502	N	
Digital Processors With BCD Outputs	4 1/2 Digits		TL503		
Dual-Slope Analog	10 Bits	50	TL505		2–91
Pulse-Width Modulator for Single-Slope Converter	7 Bits	1	TL507	P	2–99

successive-approximation and semi-flash converters

ADDRESS AND DATA I/O FORMAT	SIGNAL INPUTS: ANALOG DEDICATED	SIGNAL INPUTS: ANALOG† DIGITAL	RESOLUTION (BITS)	CONVERSION SPEED (μs)‡	POWER DISSIPATION (mW TYP)	UNADJUSTED ERROR (MAX) ±LSB	TYPE	PACKAGE	PAGE NO.
Parallel	1§	0	8	100	10	0.5	ADC0803	N	2–3
						1.0	ADC0804		2–9
							ADC0805		2–3
	8					0.75	ADC0808	FN, N	2–15
						0.75	ADC0808M	FK, JD	2–21
						1.25	ADC0809	FN, N	2–15
					0.5	0.75	TL0808		2–71
						1.25	TL0809		2–71
	1§			1	35	0.5	ADC0820B	DW, FN, FK, J, N	2–29
						1.0	ADC0820C		2–29
						1.0	TLC0820A		2–29
						0.5	TLC0820B		2–29
	5	6		15	6	0.5	TLC532A	FN, N	2–105
				30			TLC533A		2–105
	1	0	10	6	10	±0.5	TLC1550	FN, N	5–29
						±1	TLC1551		
	1	0	12	12	45	±2	TLC1125	FN, N	5–3
	1	0	12	12	45	1.0	TLC1225	DW, J, N	5–15

† Analog/digital inputs can be used either as digital logic inputs or inputs for analog to digital conversion. For example: The TLC532/3A can have 11 analog inputs, 5 analog inputs, and 6 digital inputs, or any combination in between.
‡ Includes access time
§ Differential input

DATA ACQUISITION AND CONVERSION SELECTION GUIDE

successive-approximation converters

ADDRESS AND DATA I/O FORMAT	SIGNAL INPUTS: ANALOG DEDICATED	SIGNAL INPUTS: ANALOG† DIGITAL	RESOLUTION (BITS)	CONVERSION SPEED (μs)‡	POWER DISSIPATION (mW TYP)	UNADJUSTED ERROR (MAX) ±LSB	TYPE	PACKAGE	PAGE NO.
Serial	1§	0	8	84	10	1.0	ADC0831A	P	2–39
						0.5	ADC0831B		
	2§					1.0	ADC0832A		
						0.5	ADC0832B		
	4§					1.0	ADC0834A	N	2–47
						0.5	ADC0834B		
	8					1.0	ADC0838A	FN, N	
						0.5	ADC0838B		
	11			13	6	0.5	TLC540	DW, FN, N	2–115
				25			TLC541		
	8			40	10		TLC542	FN, N	2–123
	19			13	6		TLC545	FN, N	2–131
				25			TLC546		
	1			22			TLC548	D, P	2–139
				25			TLC549		
	11			31			TLC1540	FK, FN, J, N	2–147
						1.0	TLC1541		

† Analog/digital inputs can be used either as digital logic inputs or inputs for analog to digital conversion. For example: The TLC532/3A can have 11 analog inputs, 5 analog inputs, and 6 digital inputs, or any combination in between.
‡ Includes access time
§ Differential input

D/A converters (5 V to 15 V)

FUNCTION	TTL COMPATIBLITY AT 15 V	RESOLUTION (BITS)	SETTLING TIME (ns)	TYPE	PACKAGE	PAGE NO.
Single Multiplying D/A	No	8	100	AD7524A	N	3–3
Single Multiplying D/A				AD7524J	FN, N	3–3
				AD7524M	FK, J	3–11
				TLC7524	D, FN, N	3–53
Dual Multiplying D/A				AD7528B AD7528K	FN, N	3–19
				TLC7528M	FK, J	3–31
				TLC7528	DW, FN, N	3–61
	Yes			AD7628	FN, N	3–43
				TLC7628	DW, FN, N	3–75

video interface palettes

FUNCTION	RESOLUTION	SPEED	TYPE	PACKAGE	PAGE NO.
Color Palette	Triple 8-bit	80, 110, 135 MHz	TLC34058	FN, PGA	6–3
	Triple 8-bit with programmable pixel bus	66, 85, 110, 135 MHz	TLC34075	FN	9–109

analog interface for digital signal processors

FUNCTION	TRANSFER CHARACTERISTICS	DYNAMIC RANGE (BITS)	RESOLUTION (BITS)	SAMPLING RATE	ON-BOARD FILTERS	TYPE	PAGE NO.
Discrete Interfaces A/D and D/A	Linear	8	8	1 MHz (A/D)	No	TLC0820/ ADC0820	2–29
				5 MHz (D/A)		TLC7524	3–53
						AD7524	3–3
				5 MHz (Dual D/A)		TLC7528	3–61
						AD7528	3–19
High-Performance Combo	Linear	14	14	16 kHz (Programmable)	Yes (Programmable)	TLC32040† TLC32041† TLC32042†	5–37
Voiceband AIC	Linear	14	14	16 kHz	Yes	TLC32044	5–69
						TLC32044M	5–103
						TLC32045	5–135
				25 kHz		TLC32046	9–3
						TLC32047	9–57
High-Speed AIC	Linear	8	8	1.5 µs ADC 100 ns DAC Settling	Yes	TLC32071	5–173

† The TLC32040 and TLC32041 have two differential inputs for the 14-bit A/D and a serial port input for the 14-bit D/A. The A/D conversion accuracy for this device is measured in terms of signal-to-quantization distortion and also in LSB over certain converter ranges. The package types are FN and N. Please refer to the data sheet.

high-speed converters

CONVERSION FUNCTION	RESOLUTION (BITS)	CONVERSION FREQUENCY (MHz)	POWER DISSIPATION (mW)	TYPE	PACKAGE	PAGE NO.
Video A/D Converter	6	20	300	TL5501	N	4–3
	8			TLC5503-2	DW, N	4–27
Video D/A Converter	6		325	TL5601	N	4–9
	8		375	TL5602	N	4–13
			125	TLC5602	DW, N	4–47
Flash A/D	8	10	300	TLC5503-5	DW, N	4–37
				TLC5502-5		4–17

analog switches and multiplexers

FUNCTION	POWER SUPPLIES (V)	VOLTAGE RANGE (V)	TYPICAL IMPEDANCE (OHMS)	TYPE	PACKAGE	PAGE NO.
Twin SPDT	±15	±10	100	TL182	N	7–3
			150	TL185		
Dual SPST			100	TL188		
Twin Dual SPST			150	TL191		
SPDT	±25	−17 to +25	100	TL601	JG, P	7–9
Dual SPDT				TL604		
SPST With Enable			100	TL607		
SPST With Logic Inputs			80	TL610		
Quad Bilateral Analog Switch	12	2 to 12	50	TLC4016	D, J, N	7–15
			30	TLC4066		7–23

switched-capacitor filter ICs

FUNCTION	FILTER ORDER	POWER SUPPLIES (V)	TYPE	PACKAGE	PAGE NO.
Dual Filter, General Purpose	2	±4 to ±5	TLC10/MF10A	FN, N	8–15
			TLC20/MF10C		
Low Pass, Butterworth	4	±2.5 to ±6	TLC04/MF4-A-50	D, P	8–3
			TLC14/MF4-A-100		

Replacements are based on similarity of electrical and mechanical characteristics shown in currently published data. Interchangeability in particular applications is not guaranteed. Before using a device as a substitute, the user should compare the specifications of the substitute device with the specifications of the original.

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Manufacturers are arranged in alphabetical order.

ANALOG DEVICES	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
AD570JN		ADC0803CN	2–3
AD7512DIJN		TL182CN	7–3
AD7512DIJQ		TL182IN	7–3
AD7512DIKN		TL182CN	7–3
AD7512DIKQ		TL182IN	7–3
AD7512DISD		TL182MJ	7–3
AD7512DITD		TL182MJ	7–3
AD7524AD	AD7524AN	TLC7524IN	3–53
AD7524JN	AD7524JN	TLC7524CN	3–53
AD7528BQ	AD7528BN	TLC7528IN	3–61
AD7528KN	AD7528KN	TLC7528CN	3–61
AD7820K/B/T	TLC0820A, ADC0820CC		2–29
AD7820L/C/U	TLC0820B, ADC0820BC		2–29
AD7820	TLC0820, ADC0820		2–29
ADC82AG		TLC0820BIN,	2–29
		ADC0820BCIN	2–29
ADC82AM		TLC0820AIN,	2–29
		ADC0820CCIN	2–29
ADC-830C		ADC0803CN	2–3
ADC-EK12DC		TL500/1/3CN	2–77
		TLC7135CN	2–59
		TLC7135CFN	2–59
		ICL7135CN	2–59
		ICL7135CFN	2–59
ADC-EK12DR		TL500/1/3CN	7–77
		TLC7135CN	2–59
		TLC7135CFN	2–59
		ICL7135CN	2–59
		ICL7135CFN	2–59

FUJITSU	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
MB4053P		TL507IN	2–99
MB40576	TL5501		4–3
MB40578	TLC5502		4–17
MB40776	TL5601		4–9
MB40778	TLC5602		4–47

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HARRIS	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
CD4016AD	TLC4016MJ		7–15
CD4016AE	TLC4016IN		7–15
CD4066AD	TLC4066MJ		7–23
CD4066AE	TLC4066IN		7–23
CA3162E		TL501CN/TL503CN	2–77

INTERSIL	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
ADC0803LCD	ADC0803IN		2–3
ADC0803LCN	ADC0803CN		2–3
ADC0804LCD	ADC0804IN		2–9
ADC0804LCN	ADC0804CN		2–9
DGM182AK	TL182MN	TL604MP	7–3 / 7–9
DGM182BJ	TL182CN/IN	TL604CP/IP	7–3 / 7–9
DGM185AK	TL185MN	TL604MP	7–3 / 7–9
DGM185BJ	TL185CN/IN	TL604CP/IP	7–3 / 7–9
DGM188AK	TL188MN	TL610MP	7–3 / 7–9
DGM188BJ	TL188CN/IN	TL610CP/IP	7–3 / 7–9
DGM191AK	TL191MN	TL610MP	7–3 / 7–9
DGM191BJ	TL191CN/IN	TL610CP/IP	7–3 / 7–9
ICL7135CPI	ICL7135CN		2–59
	ICL7135CFN		2–59
	TLC7135CN		2–59
	TLC7135CFN		2–59

LINEAR TECHNOLOGY	DIRECT TI REPLACEMENT	PAGE NO.
LTC1060ACN	TLC10N	8–15
LTC1060CN	TLC20N	8–15

MAXIM	DIRECT TI REPLACEMENT	PAGE NO.
MF10BN	TLC10N	8–15
MF10CN	TLC20N	8–15

MICRO NETWORKS	SUGGESTED TI REPLACEMENT	PAGE NO.
MN5100/5101	TLC0820ACN/TLC0820BCN,	2–29
	ADC0820BCN/ADC0820CCN	2–29
MN5120/5130/5140	TLC0820ACN/TLC0820BCN,	2–29
	ADC0820BCN/ADC0820CCN	2–29

MICRO POWER SYSTEMS	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
MP7138AN		TL500/1/3CN	2–77
		TLC7135CN	2–59
		TLC7135CFN	2–59
		ICL7135CN	2–59
		ICL7135CFN	2–59
MP7574AD/BD		ADC0805IN series	2–3
MP7574JN/KN		ADC0804CN or	2–9
		ADC0805CN series	2–5
MP7581/JN/KN/AD/BD		ADC0808N/ADC0809N	2–15 / 2–15

MOTOROLA	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
MC1405L		TL500CN/TL501CN	2–77
		TL505CN	2–91
MC14433P		TL500/1/3CN	2–77
		TLC7135CN	2–59
		TLC7135CFN	2–59
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		ICL7135CFN	2–59
MC14442L	TLC533AMJ	TLC532AMJ	2–105
MC14442P	TLC533AIN	TLC532AIN	2–105
MC14443P		TL507IN	2–99
MC14444P		TLC546IN	2–131
MC14447P		TL507IP	2–99
MC145040FN	TLC541MFN	TLC540MFN	2–115 / 2–115
MC145040L	TLC541MJ	TLC540MJ	2–115 / 2–115
MC145040P	TLC541MN	TLC540MN	2–115 / 2–115
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MC54HC4016J	TLC4016MJ		7–15
MC74HC4016J	TLC4016IN		7–15
MC74HC4016N	TLC4016IN		7–15
MC54HC4066J	TLC4066MJ		7–23
MC74HC4066J	TLC4066IN		7–23
MC74HC4066N	TLC4066IN		7–23

NATIONAL	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
ADC0803LCD	ADC0803IN		2–3
ADC0803LCN	ADC0803IN		2–3
ADC0804LCD	ADC0804IN		2–9
ADC0804LCN	ADC0804CN		2–9
ADC0805LCN	ADC0805IN		2–3
ADC0808CCJ	ADC0808N/TL0808N		2–15 / 2–71
ADC0808CCN	ADC0808N/TL0808N		2–15 / 2–71
ADC0809CCN	ADC0809N/TL0809N		2–15 / 2–71
ADC0811BCJ	TLC541IN	TLC540IN	2–115 / 2–115

NATIONAL (Continued)	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
ADC0811BCN	TLC541IN	TLC540IN	2–115 / 2–115
ADC0811BCV	TLC541IFN	TLC540IFN	2–115 / 2–115
ADC0811BJ	TLC541MJ	TLC540MJ	2–115 / 2–115
ADC0811CCJ	TLC541IN	TLC540IN	2–115 / 2–115
ADC0811CCN	TLC541IN	TLC540IN	2–115 / 2–115
ADC0811CCV	TLC541IFN	TLC540IFN	2–115 / 2–115
ADC0811CJ	TLC541MJ	TLC540MJ	2–115 / 2–115
ADC0820BCD	TLC0820BIN,		2–29
	ADC0820BCIN		2–29
ADC0820BCN	TLC0820BCN,		2–29
	ADC0820BCN		2–29
ADC0820BD	TLC0820BMJ,		2–29
	ADC0820BJ		2–29
ADC0820CCD	TLC0820AIN,		2–29
	ADC0820CCIN		2–29
ADC0820CCN	TLC0820ACN,		2–29
	ADC0820CCN		2–29
ADC0820CD	TLC0820AMJ,		2–29
	ADC0820CJ		2–29
ADC0829BCN	TLC533AIN	TLC532AIN	2–105 / 2–105
ADC0829CCN	TLC533AIN	TLC532AIN	2–105 / 2–105
ADC0830BCN		TLC546IN	2–131
ADC0830CCN		TLC546IN	2–131
ADC0831BCJ	ADC0831BIP	TLC549IN	2–39 / 2–139
ADC0831BCN	ADC0831BCP	TLC549IN	2–39 / 2–139
ADC0831CCJ	ADC0831AIP	TLC549IN	2–39 / 2–139
ADC0831CCN	ADC0831ACP	TLC549IN	2–39 / 2–139
ADC0832BCJ	ADC0832BIP		2–39
ADC0832BCN	ADC0832BCP		2–39
ADC0832CCJ	ADC0832AIP		2–39
ADC0832CCN	ADC0832ACP		2–39
ADC0834BCJ	ADC0834BIN		2–47
ADC0834BCN	ADC0834BCN		2–47
ADC0834CCJ	ADC0834AIN		2–47
ADC0834CCN	ADC0834ACN		2–47
ADC0838BCJ	ADC0838BIN		2–47
ADC0838BCN	ADC0838BCN		2–47
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ADC1001CCJ		TLC1541IN	2–147
ADC1005BCJ		TLC1541IN	2–147
ADC1005CCJ		TLC1541IN	2–147
ADC1225		TLC1225	5–15
ADC3511CCN		TL500/1/3CN	2–77
		TLC7135CN	2–59
		TLC7135CFN	2–59
		ICL7135CN	2–59
		ICL7135CFN	2–59

NATIONAL (Continued)	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
ADC3711CCN		TL500/1/3CN	2–77
		TLC7135CN	2–59
		TLC7135CFN	2–59
		ICL7135CN	2–59
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ADD3501CCN		TL500/1/2CN	2–77
ADD3701CCN		TL500/1/2CN	2–77
MF10AN	TLC10CN		8–15
MF10CN	TLC20CN		8–15
MM54HC4016J	TLC4016MJ		7–15
MM54HC4066J	TLC4066MJ		7–23
MM74HC4016N/J	TLC4016IN		7–15
MM74HC4066N/J	TLC4066IN		7–23
MF4-50	TLC04/MF4A-50		8–3
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PRECISION MONOLITHICS	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
PM7524FQ		TLC7524IN, AD7524AN	3–53 / 3–3
PM7524FP		TLC7524CN, AD7524JN	3–53 / 3–3
PM7528		TLC7528, AD7528	3–61 / 3–19

SIGNETICS	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
ADC0803/4/5-1LCN	ADC0803/5IN		2–3
	ADC0804IN		2–3
ADC0804-1CN	ADC0804CN		2–9
NE5034F		TLC532AIN	2–105
NE5036FE/N/D		TLC549CN/CD	2–139
NE5037F/N/D		TLC549CN/CD	2–139

SILICONIX	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
DG182AP	TL182MN	TL610MP	7–9
DG182BP	TL182CN/IN	TL610CP/IP	7–9
DG185AP	TL185MN	TL604MP	7–9
DG185BP	TL185CN/IN	TL604CP/IP	7–9
DG188AP	TL188MN	TL604MP	7–9
DG188BP	TL188CN/IN	TL604CP/IP	7–9
DG191AP	TL191MN	TL604MP	7–9
DG191BP	TL191CN/IN	TL604CP/IP	7–9
LD110CJ		TL503CN	2–77
		TLC7135CN	2–59
		TLC7135CFN	2–59
		ICL7135CN	2–59
		ICL7135CFN	2–59
LD111ACJ		TL501CN	2–77
		TLC7135CN	2–59
		TLC7135CFN	2–59
		ICL7135CN	2–59
		ICL7135CFN	2–59
LD120CJ		TL500CN	2–77
		TLC7135CN	2–59
		TLC7135CFN	2–59
		ICL7135CN	2–59
		ICL7135CFN	2–59
LD121ACJ		TL503CN	2–77
		TLC7135CN	2–59
		TLC7135CFN	2–59
		ICL7135CN	2–59
		ICL7135CFN	2–59
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Si7135CJ	TLC7135CN		2–59
	TLC7135CFN		2–59
	ICL7135CN		2–59
	ICL7135CFN		2–59

TELEDYNE	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
TSC7135CPI	TLC7135CN		2–59
	TLC7135CFN		2–59
	ICL7135CN		2–59
	ICL7135CFN		2–59
TSC8700		ADC0808N	2–15
TSC8701		TLC1541IN	2–147
TSC8703		ADC0808N	2–15
TSC8704		TLC1541IN	2–147
TSC14433CN		TLC7135CN	2–59
		TLC7135CFN	2–59
		ICL7135CN	2–59
		ICL7135CFN	2–59

TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR ANALOG-TO-DIGITAL AND DIGITAL-TO-ANALOG CONVERTERS

INTRODUCTION

These terms, definitions, and letter symbols are in accordance with those currently approved by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

1. GENERAL TERMS

Analog-to-Digital Converter (ADC)

A converter that uniquely represents all analog input values within a specified total input range by a limited number of digital output codes, each of which exclusively represents a fractional part of the total analog input range. (See Figure 1.)

NOTE: This quantization procedure introduces inherent errors of one-half LSB (least significant bit) in the representation since, within this fractional range, only one analog value can be represented free of error by a single digital output code.

CONVERSION CODE

Range of Analog Input Values	Digital Output Code
4.5-5.5	0...101
3.5-4.5	0...100
2.5-3.5	0...011
1.5-2.5	0...010
0.5-1.5	0...001
0-0.5	0...000

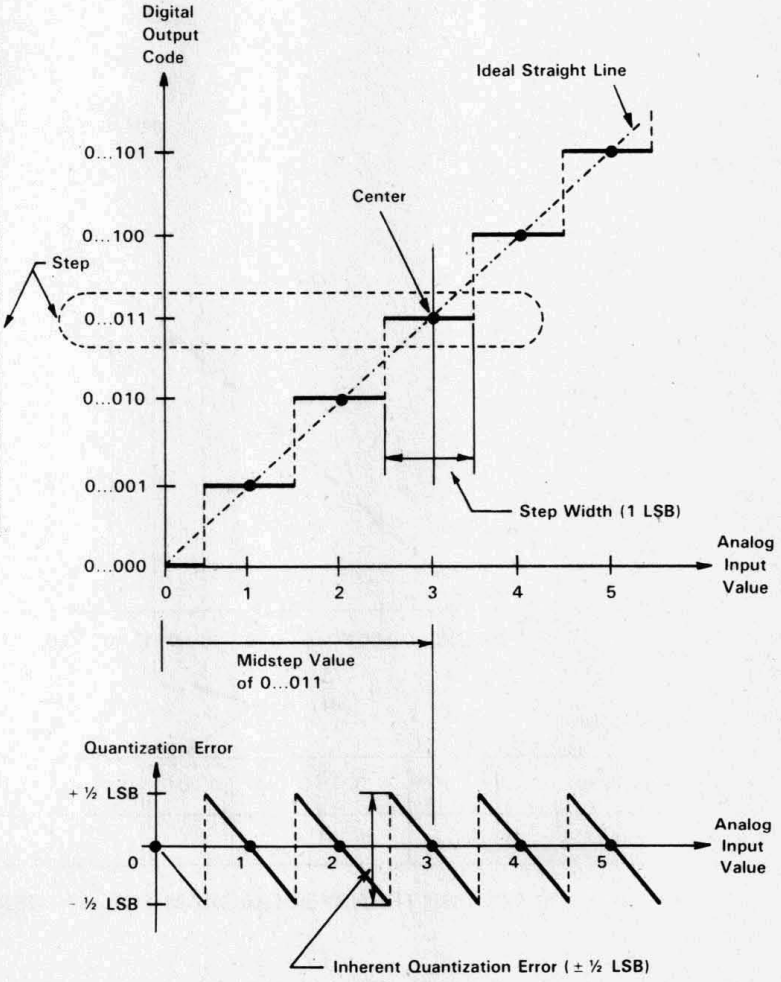


FIGURE 1. ELEMENTS OF TRANSFER DIAGRAM FOR AN IDEAL LINEAR ADC

Analog-to-Digital Processor

An integrated circuit providing the analog part of an ADC; provision of external timing, counting, and arithmetic operations is necessary for implementing a full analog-to-digital converter.

Companding DAC

A DAC whose transfer function complies with a compression or expansion law.

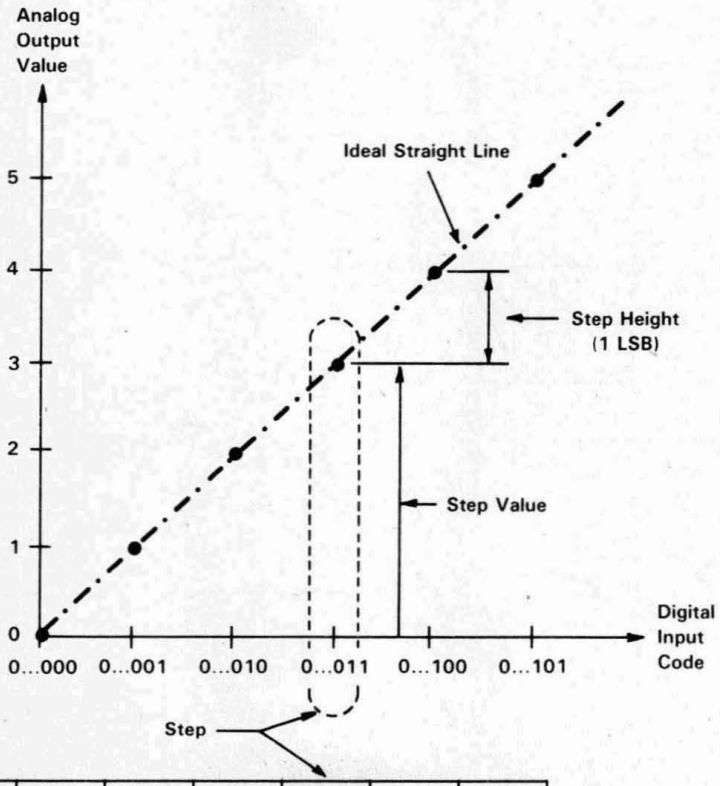
NOTE 1: The corresponding ADC normally consists of such a companding DAC and additional external circuitry.

NOTE 2: The compression or expansion law is usually a logarithmic function, e.g., A-law or μ-law.

Conversion Code (of an ADC or a DAC)

The set of correlations between each of the fractional parts of the total analog input range or each of the digital input codes, respectively, and the corresponding digital output codes or analog output values, respectively. (See Figures 1 and 2.)

NOTE: Examples of output code formats are straight binary, 2's complement, and binary-coded decimal.



CONVERSION CODE

Digital Input Code	0...000	0...001	0...010	0...011	0...100	0...101
Analog Output Value	0	1	2	3	4	5

FIGURE 2. ELEMENTS OF TRANSFER DIAGRAM FOR AN IDEAL LINEAR DAC

Digital-to-Analog Converter (DAC)

A converter that represents a limited number of different digital input codes by a corresponding number of discrete analog output values. (See Figure 2.)

NOTE: Examples of input code formats are straight binary, 2's complement, and binary-coded decimal.

Full Scale (of a unipolar ADC or DAC)

A term used to refer a characteristic to that step within the transfer diagram whose nominal midstep value or nominal step value has the highest absolute value. (See Figure 3a for a linear unipolar ADC.)

NOTE 1: The subscript for the letter symbol of a characteristic at full scale is "FS".

NOTE 2: In place of a letter symbol, the abbreviation "FS" is in common use.

Full Scale, Negative (of a bipolar ADC or DAC) (See Figures 3b and 3c)

A term used to refer a characteristic to the negative end of the transfer diagram, that is, to the step whose nominal midstep value or nominal step value has the most-negative value.

NOTE 1: The subscript for the letter symbol of a characteristic at negative full scale is "FS−" (V_{FS-}, I_{FS-}).

NOTE 2: In place of a letter symbol, the abbreviation "FS−" is in common use.

Full Scale, Positive (of a bipolar ADC or DAC) (See Figure 3b and 3c)

A term used to refer a characteristic to the positive end of the transfer diagram, that is, to the step whose nominal midstep value or nominal step value has the most-positive value.

NOTE 1: The subscript for the letter symbol of a characteristic at positive full scale is "FS+" (V_{FS+}, I_{FS+}).

NOTE 2: In place of a letter symbol, the abbreviation "FS+" is in common use.

Full-Scale Range, Nominal (of a linear ADC or DAC) (V_{FSRnom}, I_{FSRnom}) (See Figure 3)

The total range in analog values that can be coded with uniform accuracy by the total number of steps with this number rounded to the next higher power of 2.

NOTE: In place of the letter symbols, the abbreviation "FSR(nom)" can be used.

Example: Using a straight binary n-bit code format, it follows:
- for an ADC: FSR(nom) = $2^n \times$ (nominal value of step width)
- for a DAC: FSR(nom) = $2^n \times$ (nominal value of step height)

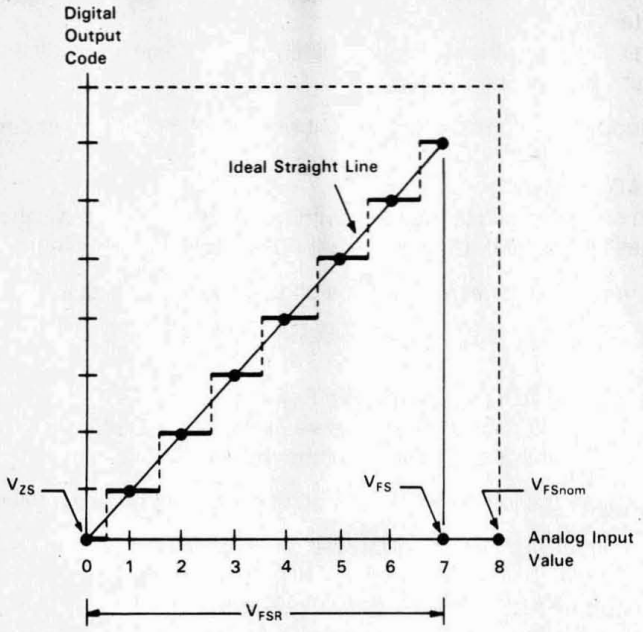
Full-Scale Value, Nominal (V_{FSnom}, I_{FSnom})

A value derived from the nominal full-scale range:
- for a unipolar converter: $V_{FSnom} = V_{FSRnom}$
- for a bipolar converter: $V_{FSnom} = 1/2\ V_{FSRnom}$

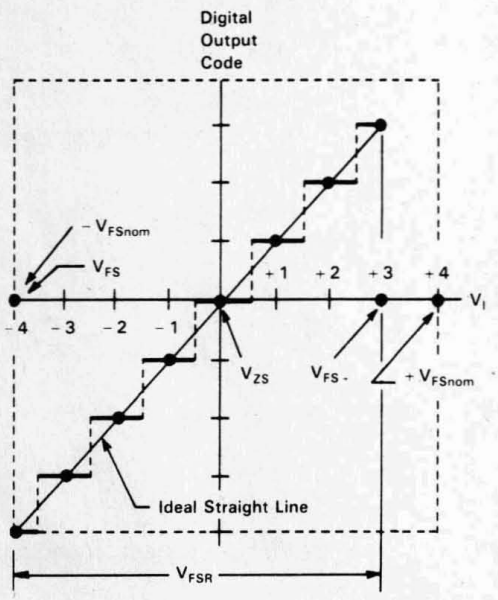
(See Figure 3.)

NOTE 1: In a few data sheets, this analog value is used as a reference value for adjustment procedures or as a rounded value for the full-scale range(s).

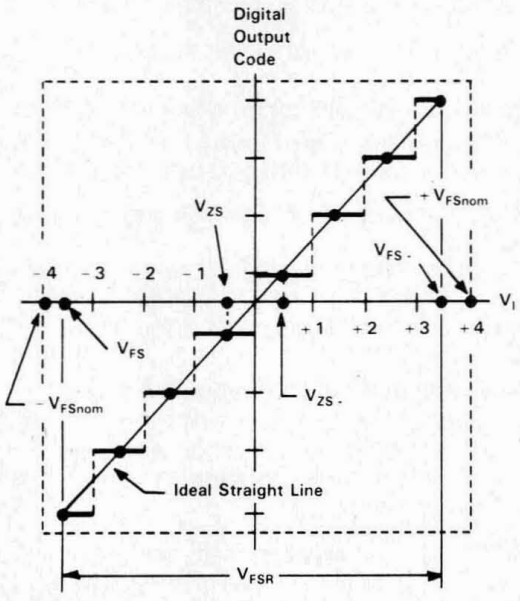
NOTE 2: In place of letter symbols, the abbreviation "FS(nom)" is in common use.



a. UNIPOLAR ADC



b. BIPOLAR ADC WITH TRUE ZERO



c. BIPOLAR ADC WITH NO TRUE ZERO

V_I = Analog Input Value

FIGURE 3. IDEAL STRAIGHT LINE, FULL-SCALE VALUE AND ZERO-SCALE VALUE (SHOWN FOR IDEAL LINEAR ADCs)

Full-Scale Range, (Practical) (of a linear ADC or DAC) (V_{FSR}, I_{FSR}) (V_{FSRpr}, I_{FSRpr}) (See Figure 3)
The total range of analog values that correspond to the ideal straight line.

NOTE 1: The qualifying adjective "practical" can usually be deleted from this term provided that, in a very few critical cases, the term "nominal full-scale range" is not also shortened in the same way. This permits use of the shorter letter symbols or abbreviations. (See Note 2.)

NOTE 2: In place of the letter symbols, the abbreviations "FSR" and "FSR(pr)" are in common use.

NOTE 3: The (practical) full-scale range has only a nominal value because it is defined by the end points of the ideal straight line.

Example: Using a straight binary n-bit code format, it follows:
– for an ADC: FSR = $(2^n - 1) \times$ (nominal value of step width)
– for a DAC: FSR = $(2^n - 1) \times$ (nominal value of step height)

Gain Point (of an adjustable ADC or DAC)
The point in the transfer diagram corresponding to the midstep value (for an ADC) or the step value (for a DAC) of the step for which gain error is specified (usually full scale), and in reference to which the gain adjustment is performed. (See Figures 4 and 5.)

NOTE: Gain adjustment causes only a change of the slope of the transfer diagram, without changing the offset error.

Ideal Straight Line (of a linear ADC or DAC)
In the transfer diagram, a straight line between the specified points for the most-positive (least-negative) and most-negative (least-positive) nominal midstep values or nominal step values, respectively. (See Figures 1, 2, and 3.)

NOTE: The ideal straight line passes through all the points for nominal midstep values or nominal step values, respectively.

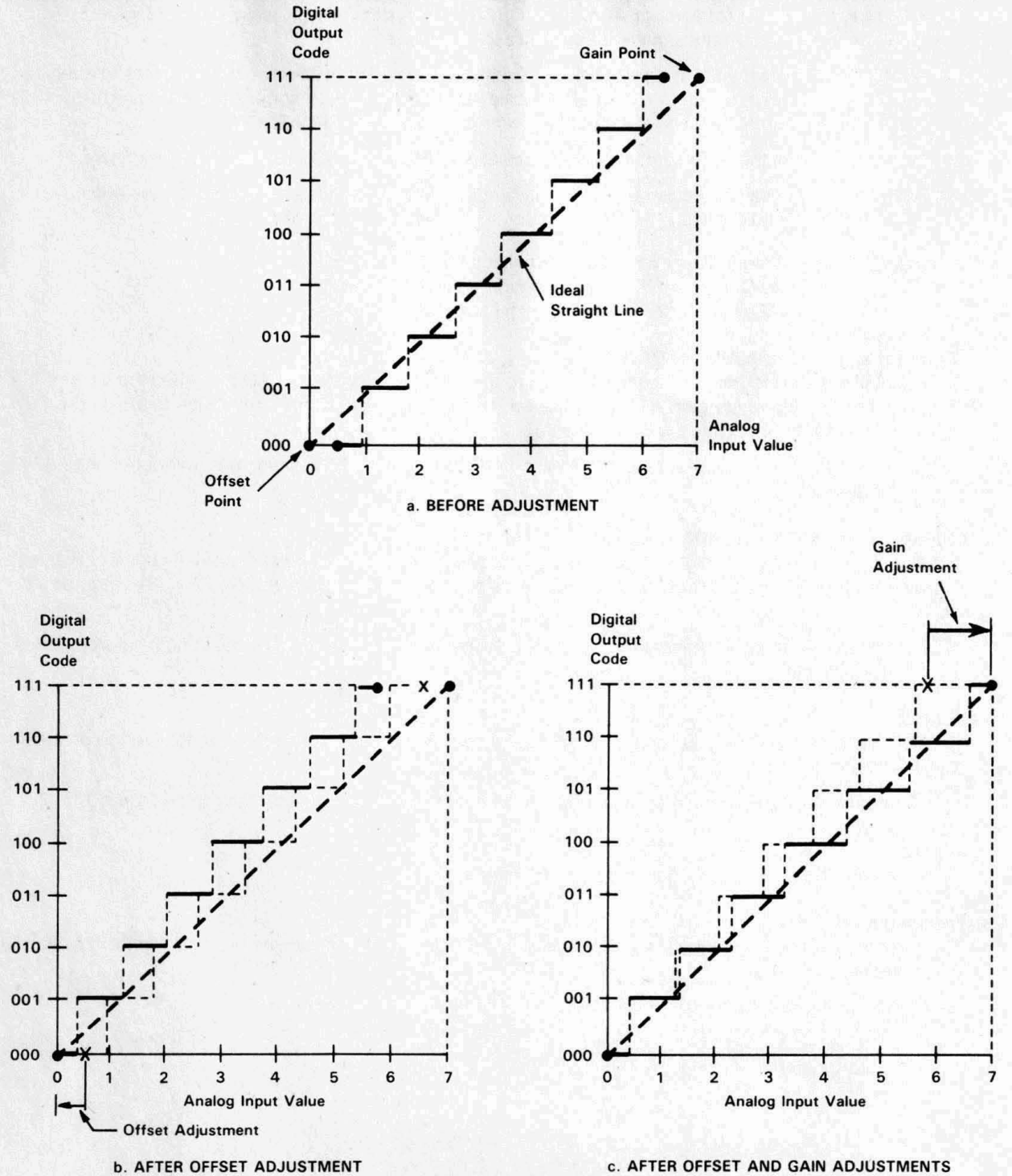
Linear ADC
An ADC having steps ideally of equal width excluding the steps at the two ends of the total range of analog input values.

NOTE: Ideally, the width of each end steps is one half of the width of any other step. (See Figure 1.)

Linear DAC
A DAC having steps ideally of equal height. (See Figure 2.)

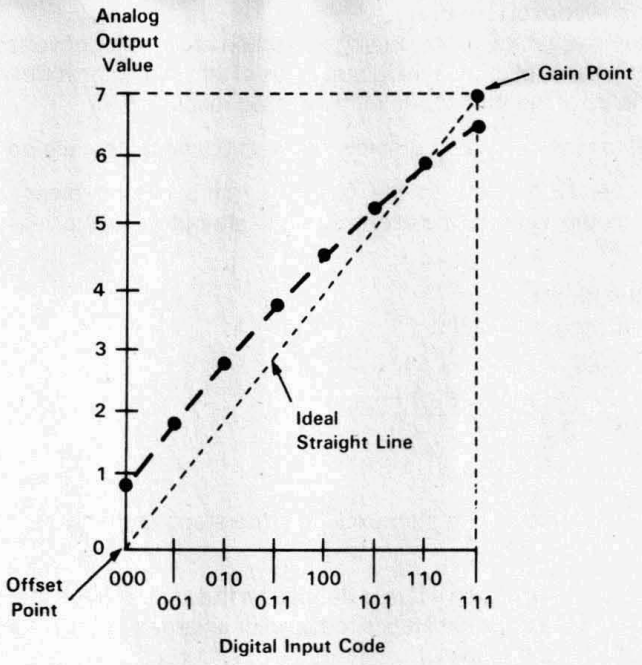
LSB, Abbreviation
The abbreviation for "Least Significant Bit", that is, for the bit that has the lowest positional weight in a natural binary numeral.

Example: In the natural binary numeral "1010", the rightmost bit "0" is the LSB.

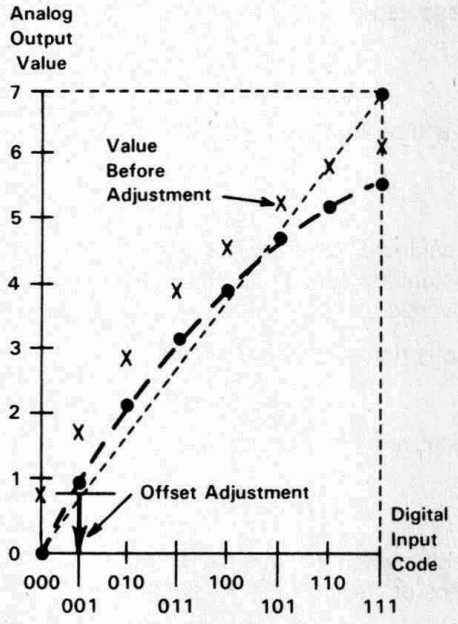


NOTE: In the above examples, the offset point is referred to the step with the digital code 000, and the gain point is referred to the step with the digital code 111.

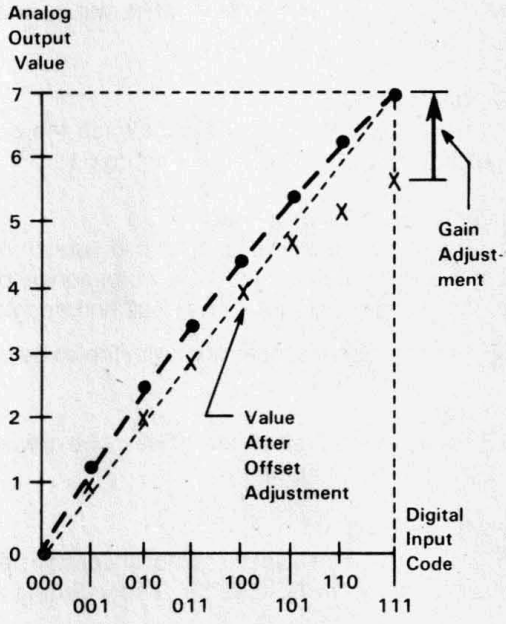
FIGURE 4. ADJUSTMENT IN OFFSET POINT AND GAIN POINT FOR AN ADC



a. BEFORE ADJUSTMENT



b. AFTER OFFSET ADJUSTMENT



c. AFTER OFFSET AND GAIN ADJUSTMENTS

NOTE: In the above examples, the offset point is referred to the step with the digital code 000, and the gain point is referred to the step with the digital code 111.

FIGURE 5. ADJUSTMENT IN OFFSET AND GAIN POINT FOR A DAC

LSB, Unit Symbol (for linear converters only)

The unit symbol for the magnitude of the analog resolution of a linear converter, which serves as a reference unit to express the magnitude of other analog quantities of that same converter, especially of analog errors, as multiples or submultiples of the magnitude of the analog resolution.

Example: "1/2 LSB" means an analog quantity equal to 0.5 times the analog resolution.

NOTE: The unit symbol LSB refers to the fact that, for a natural binary code, the analog resolution corresponds to the nominal positional weight attributed to the least significant bit of the binary numeral.

In this case, the identity:

1 LSB = analog resolution

leads, for an n-bit resolution, to:

$$1\ \text{LSB} = \frac{\text{FSR}}{2^n - 1} = \frac{\text{FSR(nom)}}{2^n}$$

Midstep Value (of an ADC)

The analog value for the center of the step excluding the steps at the two ends of the total range of analog input values.

NOTE: For the end steps, the midstep value is defined as the analog value that results when the analog value for the transition to the adjacent step is reduced or enlarged, as appropriate, by half the nominal value of the step width. (See Figure 1.)

Midstep Value, Nominal (of an ADC)

A specified analog value within a step that is ideally represented free of error by the corresponding digital output code. (See Figure 1.)

Missing Code (of an ADC)

An intermediate code that is absent when the changing analog input to an ADC causes a multiple code change in the digital output. (See Figure 6.)

Monotonicity (of an ADC or a DAC)

A property of the transfer function that ensures the consistent increase or decrease of the analog output of a DAC or the digital output of an ADC in response to a consistent increase or decrease of the digital or analog input, respectively. (Figure 7 illustrates nonmonotonic conversion.)

NOTE: An intermediate increment with the value of zero does not invalidate monotonicity.

Multiplying DAC

A DAC having at least two inputs, at least one of which is digital, and whose analog output value is proportional to the product of the inputs.

Nonlinear ADC or DAC

An ADC or a DAC with a specified nonlinear transfer function between the nominal midstep values or nominal step values, respectively, and the corresponding step widths or step heights, respectively.

NOTE: The function may be continuously nonlinear or piece-wise linear.

Offset Point (of an adjustable ADC or DAC)

The point in the transfer diagram corresponding to the midstep value (for an ADC) or the step value (for a DAC) of the step about which the transfer diagram rotates when gain is adjusted. (See Figures 4 and 5.)

NOTE: Offset adjustment must be performed with respect to this point so that it causes only a parallel displacement of the transfer diagram, without changing its slope.

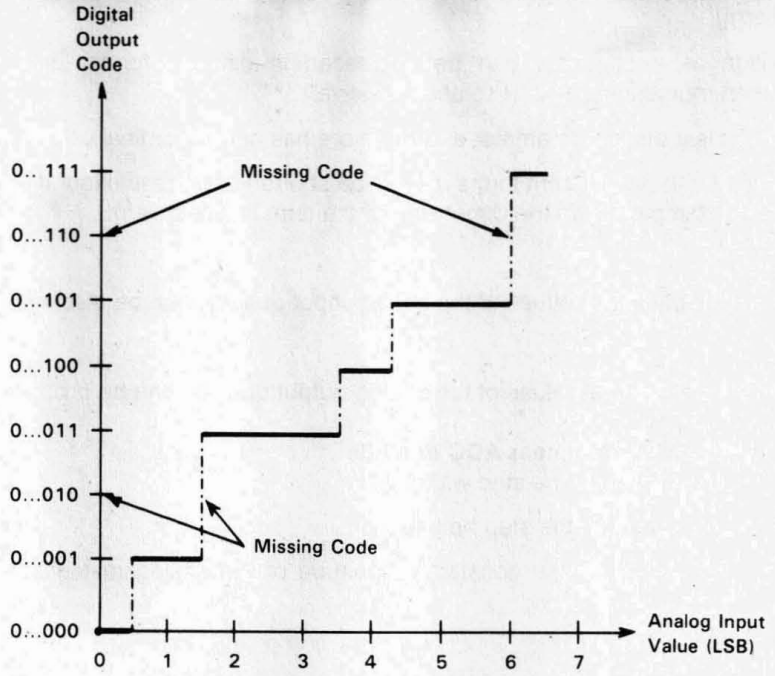
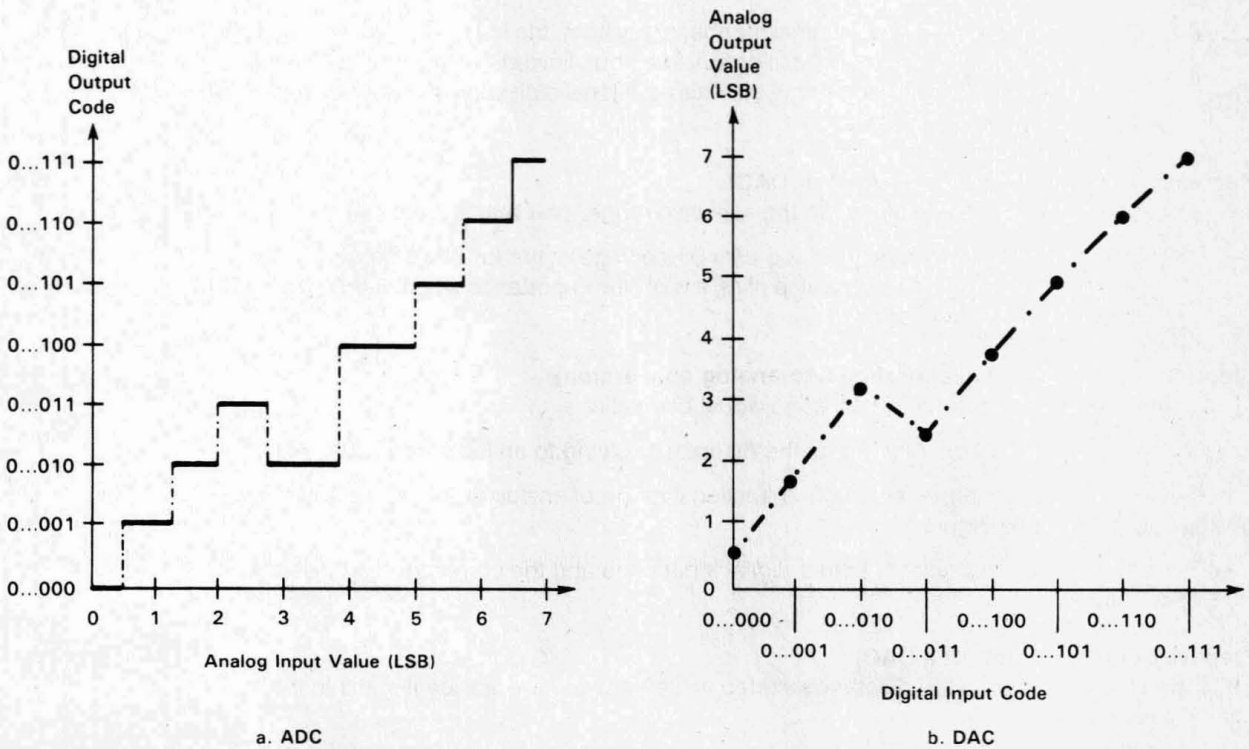


FIGURE 6. MISSING CODE FOR AN ADC



a. ADC

b. DAC

FIGURE 7. NONMONOTONIC CONVERSION OF AN ADC OR DAC

Resolution (general term)

NOTE 1: Resolution as a capability can be expressed in different forms: (see "resolution, analog", "resolution, numerical", and "resolution, relative").

NOTE 2: Resolution is a design parameter and therefore has only a nominal value.

NOTE 3: The terms for these different forms may all be shortened to "resolution" if no ambiguity is likely to occur (for example, when the dimension of the term is also given).

Resolution (of an ADC)

The degree to which nearly equal values of the analog input quantity can be discriminated.

Resolution (of a DAC)

The degree to which nearly equal values of the analog output quantity can be produced.

Resolution, Analog (of a linear or nonlinear ADC or DAC)

For an ADC: The nominal value of the step width.

For a DAC: The nominal value of the step height.

NOTE: For a linear ADC or DAC, the constant magnitude of the analog resolution is often used as the reference unit LSB.

Resolution, Numerical

The number (n) of digits in the chosen numbering system necessary to express the total number of steps.

NOTE 1: The numbering system is normally a binary or a decimal system.

NOTE 2: In the binary-coded-decimal numbering system, the term "1/2 digit" refers to an additional decimal digit with the highest positional value, but limited to the decimal figures "0" or "1" as it is represented by only a single bit. This additional digit serves to double the range of values covered by the other "n" digits.

Resolution, Relative (of a linear ADC or DAC)

The ratio of the analog resolution to the full-scale range (practical or nominal).

NOTE: This ratio is normally expressed as a percentage of the full-scale range [% of FSR, % of FSR(nom)]. For high resolutions (high value of n), it is of little importance whether this ratio refers to the practical or nominal full-scale range.

Step (of an analog-to-digital or digital-to-analog conversion)

In the conversion code: Any of the individual correlations.

In the transfer diagram: Any part of the diagram equating to an individual correlation.

For an ADC, a step represents both a fractional range of analog input values and the corresponding digital output code. (See Figure 1.)

For a DAC, a step represents both a digital input code and the corresponding discrete analog output value. (See Figure 2.)

Step Height (Step Size) (of a DAC)

The absolute value of the difference in step value between two adjacent steps in the transfer diagram. (See Figure 2.)

NOTE: For companding DACs, the term "step size" is in general use.

Step Value (of a DAC)
The value of the analog output representing a digital input code. (See Figure 2.)

Step Value, Nominal (of a DAC)
A specified step value that represents free of error the corresponding digital input code. (See Figure 2.)

Step Width (of an ADC)
The absolute value of the difference between the two ends of the range of analog values corresponding to one step. (See Figure 1.)

Temperature Coefficients of Analog Characteristics (α)

NOTE 1: The letter symbol for the temperature coefficient of an analog characteristic consists of the letter symbol α with a subscript referring to the relevant characteristic.

Example: Temperature coefficient of the gain error: α_{EG}

NOTE 2: Temperature coefficients are usually specified in "parts per million (relative to the full-scale value) per degrees Celsius", that is, in "ppm/°C".

Zero Scale (of an ADC or a DAC with true zero) (See Figures 3a and 3b)
A term used to refer a characteristic to the step whose nominal midstep value or nominal step value equals zero.

NOTE 1: The subscript for the letter symbol of a characteristic at zero scale is "ZS".

NOTE 2: In place of a letter symbol, the abbreviation "ZS" is in common use.

Zero Scale, Negative (of an ADC or a DAC with no true zero) (See Figure 3c)
A term used to refer a characteristic to the negative step closest to analog zero.

NOTE 1: The subscript for the letter symbol of a characteristic at negative zero scale is "ZS−" (V_{ZS-}, I_{ZS-}).

NOTE 2: In place of a letter symbol, the abbreviation "ZS−" is in common use.

Zero Scale, Positive (of an ADC or a DAC with no true zero) (See Figure 3c)
A term used to refer a characteristic to the positive step closest to analog zero.

NOTE 1: The subscript for the letter symbol of a characteristic at positive zero scale is "ZS+" (V_{ZS+}, I_{ZS+})

NOTE 2: In place of a letter symbol, the abbreviation "ZS+" is in common use.

2. STATIC PERFORMANCE

Accuracy (see "Errors", Part 4)

Asymmetry, Full-Scale (of a DAC with a bipolar analog range) (ΔI_{FSS}, ΔV_{FSS})
The difference between the absolute values of the two full-scale analog values.

Compliance, Current (of a DAC) ($I_{O(op)}$)
The permissible range of output current within which the specifications are valid.

Compliance, Voltage (of a DAC) ($V_{O(op)}$)
The permissible range of output voltage within which the specifications are valid.

Errors (see Part 4)

Supply Voltage Sensitivity, (of a DAC) (k_{SVS})
The change in full scale output current (or voltage) caused by a change in supply voltage.

NOTE: This sensitivity is usually expressed as the ratio of the percent change of full-scale current (or voltage) to the percent change of supply voltage.

3. DYNAMIC PERFORMANCE

Conversion Rate (of an externally controlled ADC) (f_c)
The number of conversions per unit time.

NOTE 1: The maximum conversion rate should be specified for full resolution.

NOTE 2: The conversion rate is usually expressed as the number of conversions per second.

NOTE 3: Due to additionally needed settling or recovery times, the maximum specified conversion rate is smaller than the reciprocal of the worst-case conversion time.

Conversion Time (of an ADC) (t_c)
The time elapsed between the command to perform a conversion and the appearance at the converter output of the complete digital representation of the analog input value.

Delay Time, (Digital) (of a linear or a multiplying DAC) (t_d, t_{dd})
The time interval between the instant when the digital input changes and the instant when the analog output passes a specified value that is close to its initial value, ignoring glitches. (See Figure 8.)

NOTE: For a multiplying DAC, the full term and the additional subscript d must be used to distinguish between the digital and the delay time.

Delay Time, Reference (of a multiplying DAC) (t_{dr})
The time interval between the instant when a step change of the reference voltage occurs and the instant when the analog output passes a specified value that is close to its initial value.

Feedthrough Capacitance (C_F)
The value of the capacitance for a specified value of R in an equivalent circuit for the calculation of the feedthrough error.

NOTE: The equivalent circuit consists of a high-pass R-C filter between the reference input and the analog output.

Feedthrough Error (see Part 4)

Glitch (of a DAC)
A short, undesirable transient in the analog output occurring following a code change at the digital input. (See Figure 8.)

Glitch Area (of a DAC)
The time integral of the analog value of the glitch transient.

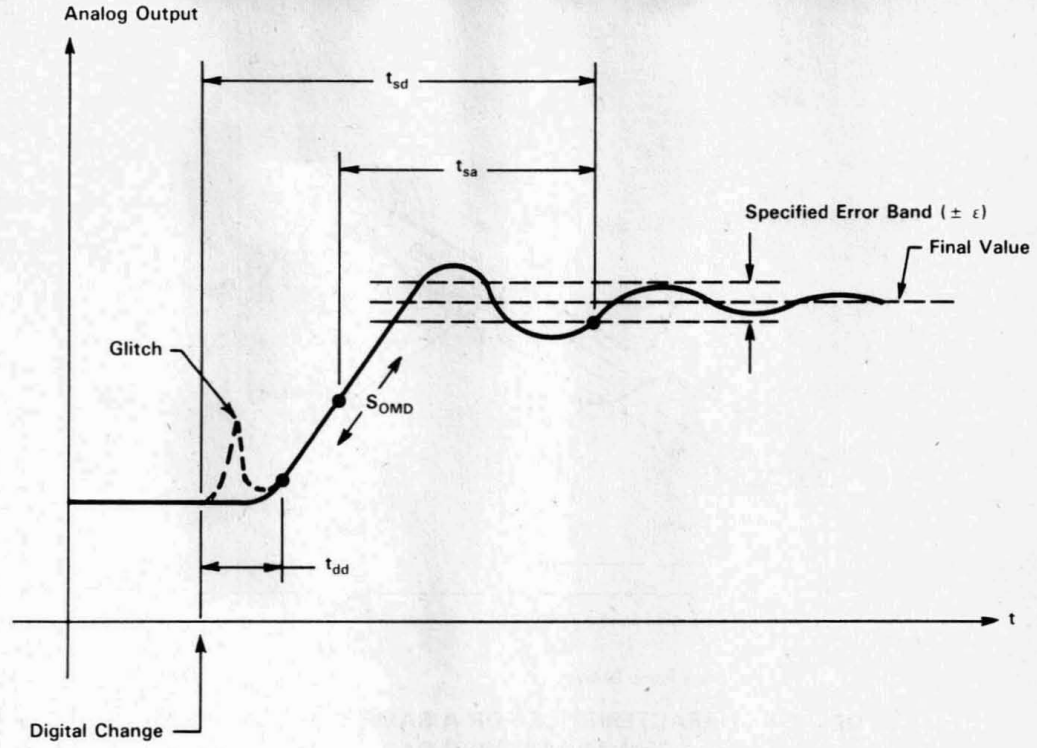
NOTE 1: Usually, the maximum specified glitch area refers to a specified worst-case code change.

NOTE 2: Instead of a letter symbol, the abbreviation "GA" is in use.

Glitch Energy (of a DAC)
The time integral of the electrical power of the glitch transient.

NOTE 1: Usually, the maximum specified glitch energy refers to a specified worst-case code change.

NOTE 2: Instead of a letter symbol, the abbreviation "GE" is in use.



t_{sd} = (Digital) Settling Time
t_{sa} = Analog Settling Time
S_{OMD} = (Digital) Slew Rate
t_{dd} = (Digital) Delay Time

FIGURE 8. OUTPUT CHARACTERISTICS OF A LINEAR OR A MULTIPLYING DAC FOR A STEP CHANGE IN THE DIGITAL INPUT CODE

Pedestal (Error) (E_p) (see Part 4)

Ramp Delay, Steady-State (of a multiplying DAC) ($t_{d(ramp)}$)
The time separation between the actual curve of the analog output and the theoretical curve (with no delay) for a ramp in reference voltage, after the settling time to steady-state ramp has elapsed. (See Figure 9.)

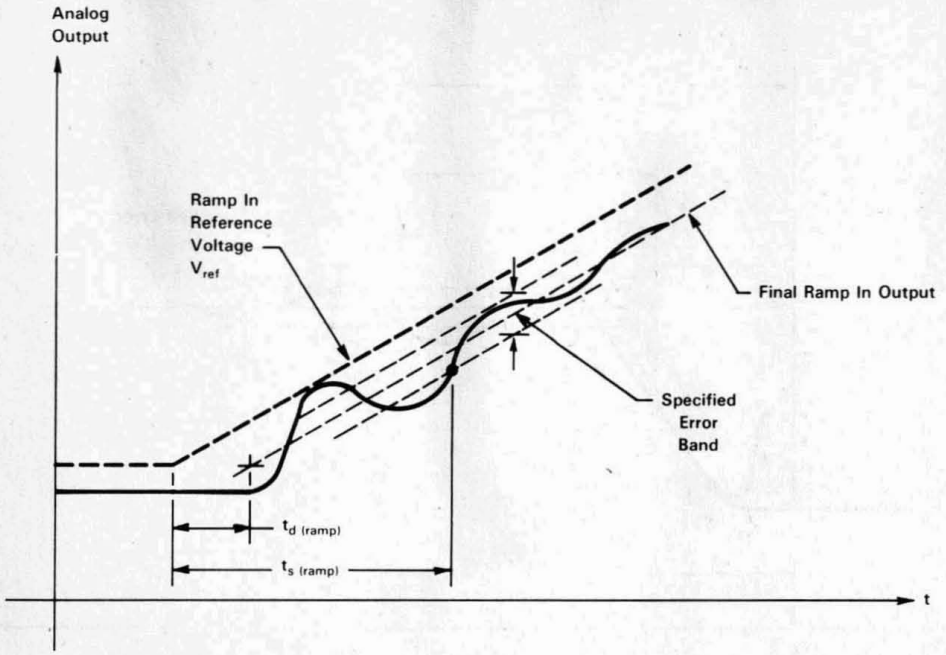
Settling Time, Analog (of a DAC) (t_{sa})
The time interval between the instant when the analog output passes a specified value and the instant when the analog output enters for the last time a specified error band about its final value. (See Figures 8 and 10.)

Settling Time, (Digital) (of a linear or a multiplying DAC) (t_s, t_{sd})
The time interval between the instant when the digital input changes and the instant when the analog output value enters for the last time a specified error band about its final value. (See Figure 8.)

NOTE: For a multiplying DAC, the full term and the additional subscript d must be used to distinguish between the digital and the settling time.

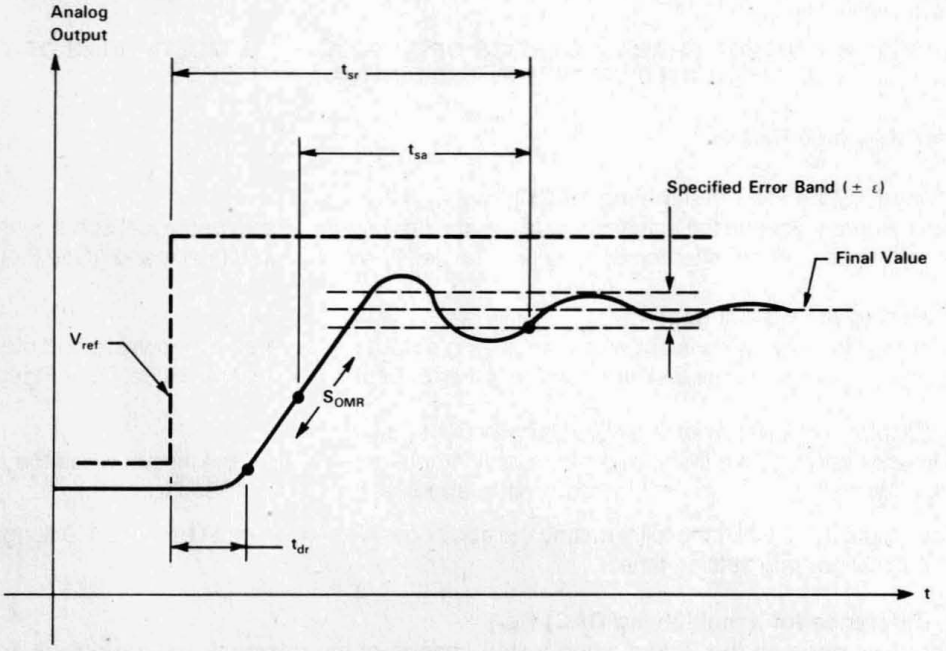
Settling Time, Reference (of a multiplying DAC) (t_{sr})
The time interval between the instant when a step change of the reference voltage occurs and the instant when the analog output enters for the last time a specified error band about its final value. (See Figure 10.)

NOTE: Specifications for the reference settling time are usually given for the highest allowed step change in reference voltage.



$t_{s\ (ramp)}$ = Settling Time To Steady-State Ramp Delay $t_{d\ (ramp)}$ = Steady-State Ramp Delay

FIGURE 9. OUTPUT CHARACTERISTICS FOR A RAMP IN REFERENCE VOLTAGE OF A MULTIPLYING DAC



t_{dr} = Reference Delay Time t_{sr} = Reference Settling Time S_{OMR} = Reference Slew Rate
t_{sa} = Analog Settling Time

FIGURE 10. OUTPUT CHARACTERISTICS FOR A STEP CHANGE IN REFERENCE VOLTAGE OF A MULTIPLYING DAC

Settling Time to Steady-State Ramp (of a multiplying DAC) ($t_{s(ramp)}$)

The time interval between the instant a ramp in the reference voltage starts and the instant when the analog output value enters for the last time a specified error band about the final ramp in the output. (See Figure 9.)

Skewing Time, Internal (of a DAC)

The difference in internal delay between the individual output transitions for a given change of digital input.

NOTE: The internal (and external) skew has a major influence on the settling time for critical changes in the digital input, for example, for a 1-LSB change from 011 . . . 111 to 100 . . . 000, and is an important source of commutation noise.

Slew Rate, (Digital) (of a linear or a multiplying DAC) (S_{OM}, S_{OMD})

The maximum rate of change of the analog output value when a change of the digital input code causes a large step change of the analog output value. (See Figure 8.)

NOTE 1: For a multiplying DAC, the full term and the additional subscript D must be used to distinguish between the digital and the slew rate.

NOTE 2: The abbreviations "SR" and "SR(dig)" are also used.

Slew Rate, Reference (of a multiplying DAC) (S_{OMR})

The maximum rate of change of the analog output following a large step change of the reference voltage. (See Figure 10.)

NOTE: The abbreviation "SR(ref)" is also used.

4. ERRORS, ACCURACY

The definitions in this section describe the errors as the difference between the actual value and the nominal value of the analog quantity. As such they may be expressed in conventional units (for example, millivolts) or as multiples or submultiples of 1 LSB. An error can also be expressed as a relative value, for example, in "% of FSR". In this case, it is common practice to use the same term as for the analog value.

Absolute Accuracy Error

Synonym for total error.

Feedthrough Error (of a multiplying DAC) (E_F)

An error in analog output due to variation in the reference voltage that appears as an offset error and is proportional to frequency and amplitude of the reference signal.

NOTE 1: The specification for the feedthrough error is given for the digital input for which the offset error is specified, and for a reference signal of specified frequency and amplitude.

NOTE 2: This error may also be expressed as a peak-to-peak analog value.

Full-Scale Error (of a linear ADC or DAC) (E_{FS})

The difference between the actual midstep value or step value and the nominal midstep value or step value, respectively, at specified full scale.

NOTE: Normally, this error specification is applied to converters that have no arrangement for an external adjustment of offset error and gain error.

Gain Error (of a linear ADC or DAC) (E_G)

For an ADC: The difference between the actual midstep value and the nominal midstep value in the transfer diagram at the specified gain point after the offset error has been adjusted to zero. (See Figure 11a.)

For a DAC: The difference between the actual step value and the nominal step value in the transfer diagram at the specified gain point after the offset error has been adjusted to zero. (See Figure 11b.)

NOTE: See Notes 1 and 2 under "Offset Error".

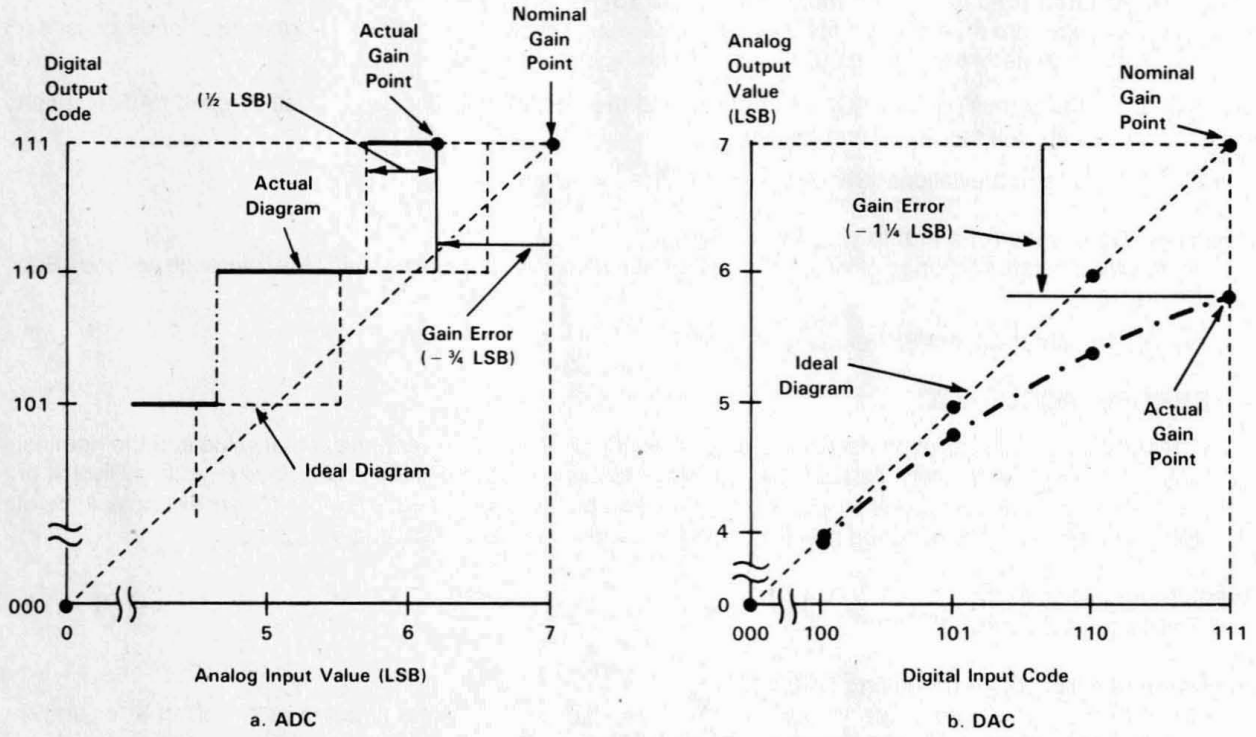


FIGURE 11. GAIN ERROR OF A LINEAR 3-BIT NATURAL BINARY CODE CONVERTER (SPECIFIED AT STEP 111), AFTER CORRECTION OF THE OFFSET ERROR

Instability, Long-Term (Accuracy) ($\Delta E_{(\Delta t)}$, $\Delta E_{(t)}$)

The additional error caused by the aging of the components and specified for a longer period in time.

Linearity Error, Best-Straight-Line (of a linear and adjustable ADC) ($E_{L(adj)}$)

The difference between the actual analog value at the transition between any two adjacent steps and its ideal value after offset error and gain error have been adjusted to minimize the magnitude of the extreme values of this difference. (See Figure 12a.)

NOTE 1: The inherent quantization error is not included in the best-straight-line linearity error of an ADC. The ideal value for the transition corresponds to the nominal midstep value ±1/2 LSB.

NOTE 2: For a uniformly curved transfer diagram, the extreme values will be very close to half of the magnitude of the end-point linearity error. (See Figure 12a.)

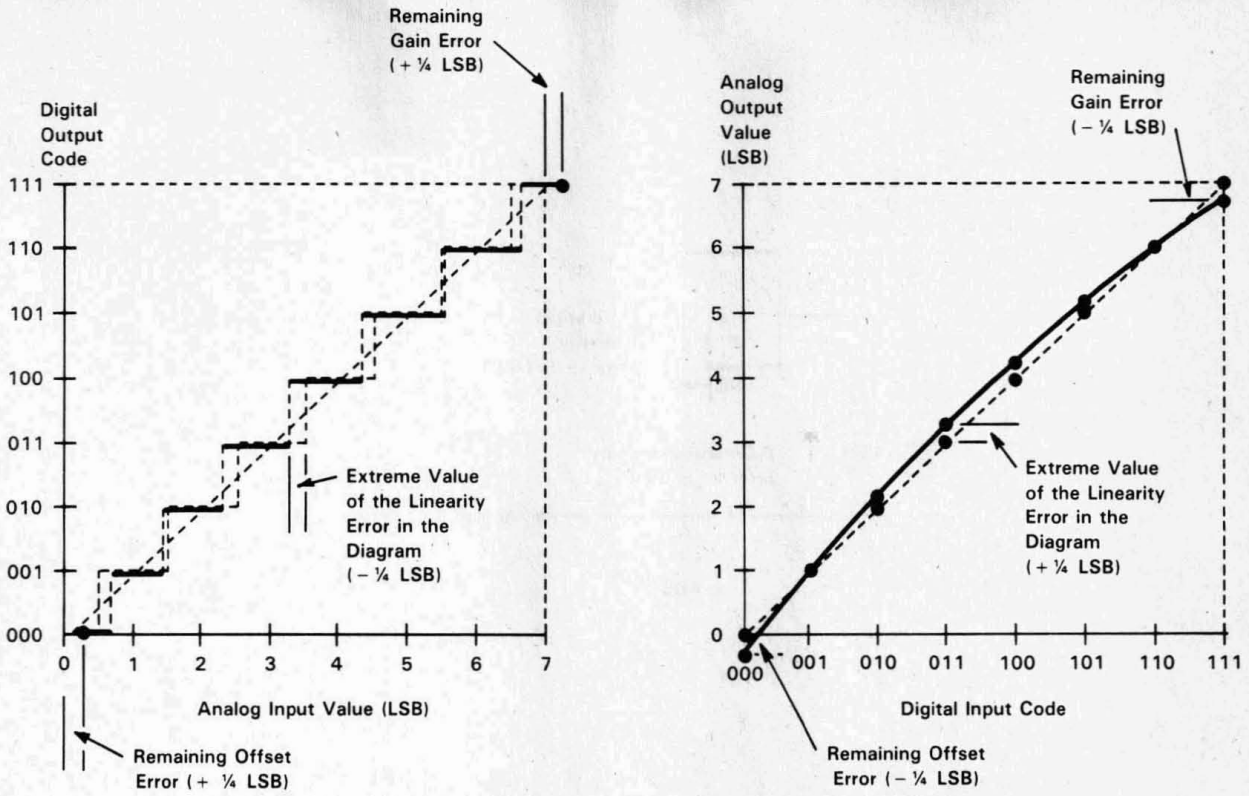


FIGURE 12. BEST-STRAIGHT-LINE LINEARITY ERROR OF A LINEAR 3-BIT NATURAL BINARY-CODED CONVERTER (VALUES BETWEEN ± ¼ LSB)

Linearity Error, Best-Straight-Line (of a linear and adjustable DAC) ($E_{L(adj)}$)

The difference between the actual step value and the nominal step value after offset error and gain error have been adjusted to minimize the magnitude of the extreme values of this difference. (See Figure 12b.)

NOTE: For a uniformly curved transfer diagram, the extreme values will be very close to half of the magnitude of the end-point linearity error. (See Figure 12b.)

Linearity Error, Differential (of a linear ADC or DAC) (E_D)

The difference between the actual step width or step height and the ideal value (1 LSB). (See Figure 13.)

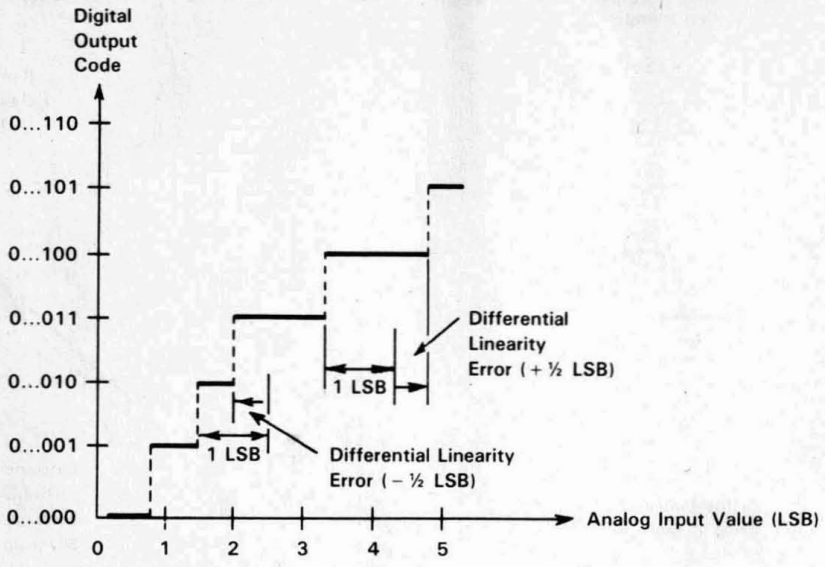
NOTE: A differential linearity error greater than 1 LSB can lead to missing codes in an ADC or to nonmonotonicity of an ADC or a DAC. (See Figures 6 and 7.)

Linearity Error, End-Point (of a linear and adjustable ADC) (E_L)

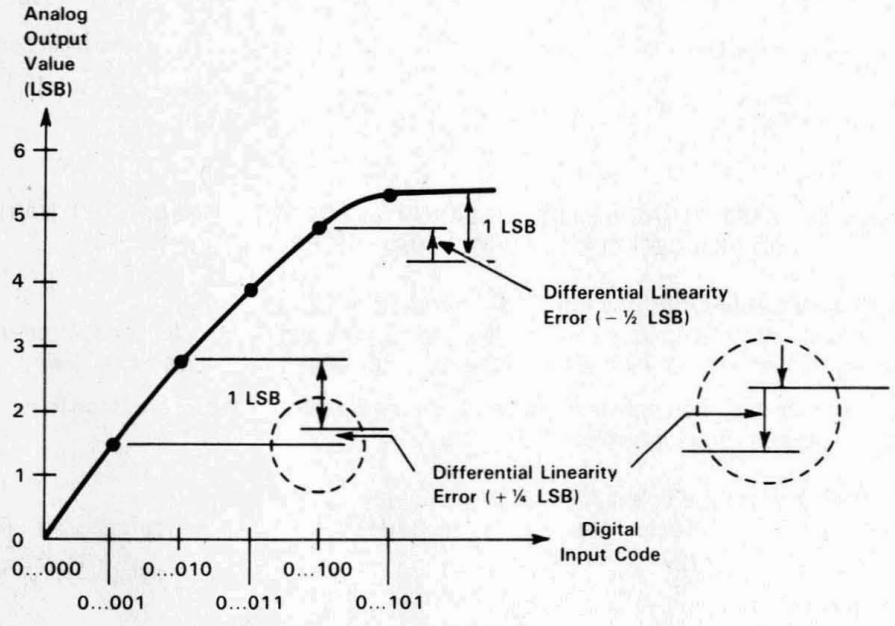
The difference between the actual analog value at the transition between any two adjacent steps and its ideal value after offset error and gain error have been adjusted to zero. (See Figure 14a.)

NOTE 1: The short term "linearity error" is in common use and is sufficient if no ambiguity with the "best-straight-line linearity error" is likely to occur.

NOTE 2: The inherent quantization error is not included in the linearity error of an ADC. The ideal value for the transition corresponds to the nominal midstep value ±1/2 LSB.



a. ADC



b. DAC

FIGURE 13. DIFFERENTIAL LINEARITY ERROR OF A LINEAR ADC OR DAC

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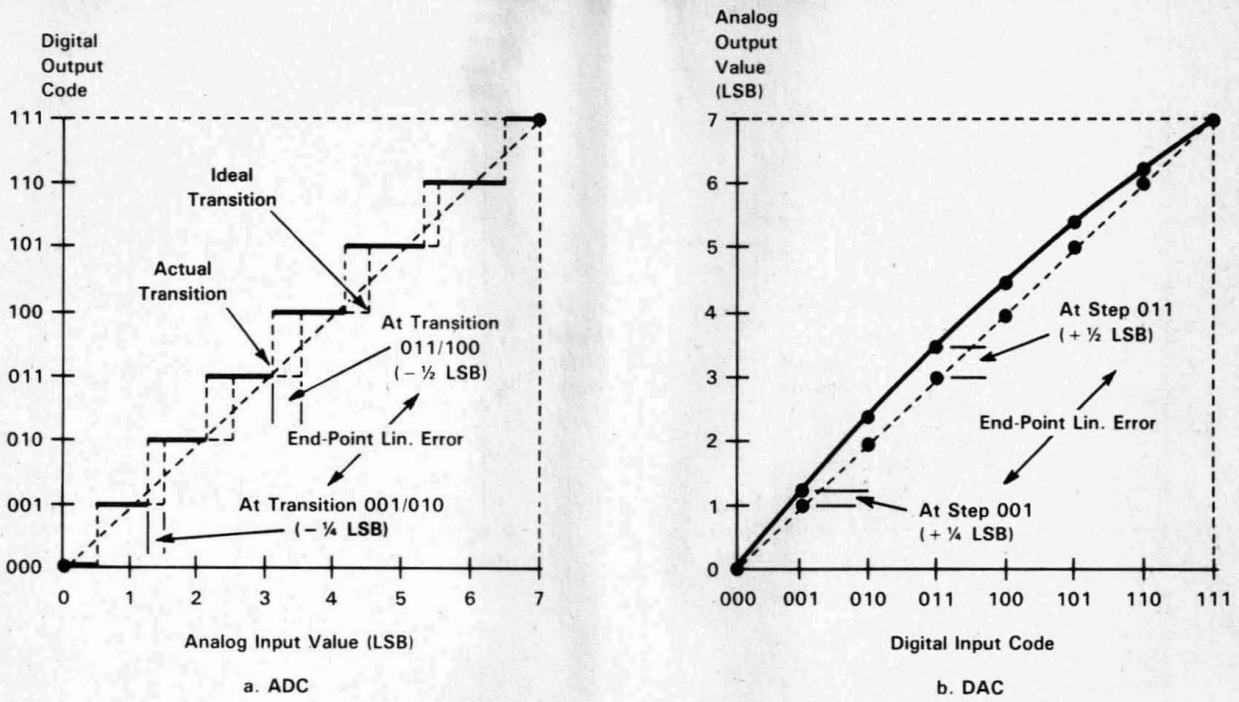

FIGURE 14. END-POINT LINEARITY ERROR OF A LINEAR 3-BIT NATURAL BINARY-CODED ADC OR DAC (OFFSET ERROR AND GAIN ERROR ARE ADJUSTED TO THE VALUE ZERO)

Linearity Error, End-point (of a linear and adjustable DAC) (E_L)

The difference between the actual step value and the nominal step value after offset error and gain error have been adjusted to zero. (See Figure 14b.)

NOTE: The short term "linearity error" is in common use and is sufficient if no ambiguity with the "best-straight-line linearity error" is likely to occur.

Offset Error (of a linear ADC or DAC) (E_O)

For an ADC: The difference between the actual midstep value and the nominal midstep value at the offset point. (See Figure 15a.)

For a DAC: The difference between the actual step value and the nominal step value at the offset point. (See Figure 15b.)

NOTE 1: Usually, the specified steps for the specification of offset error and gain error are the steps at the ends of the practical full-scale range. For an ADC, the midstep value of these steps is defined as the value for a point 1/2 LSB apart from the adjacent transition. (See Figures 11 and 15.)

NOTE 2: The terms "offset error" and "gain error" should be used only for errors that can be adjusted to zero. Otherwise, the terms "zero-scale error" and "full-scale error" should be used.

Pedestal (Error) (E_P)

A dynamic offset error produced in the commutation process.

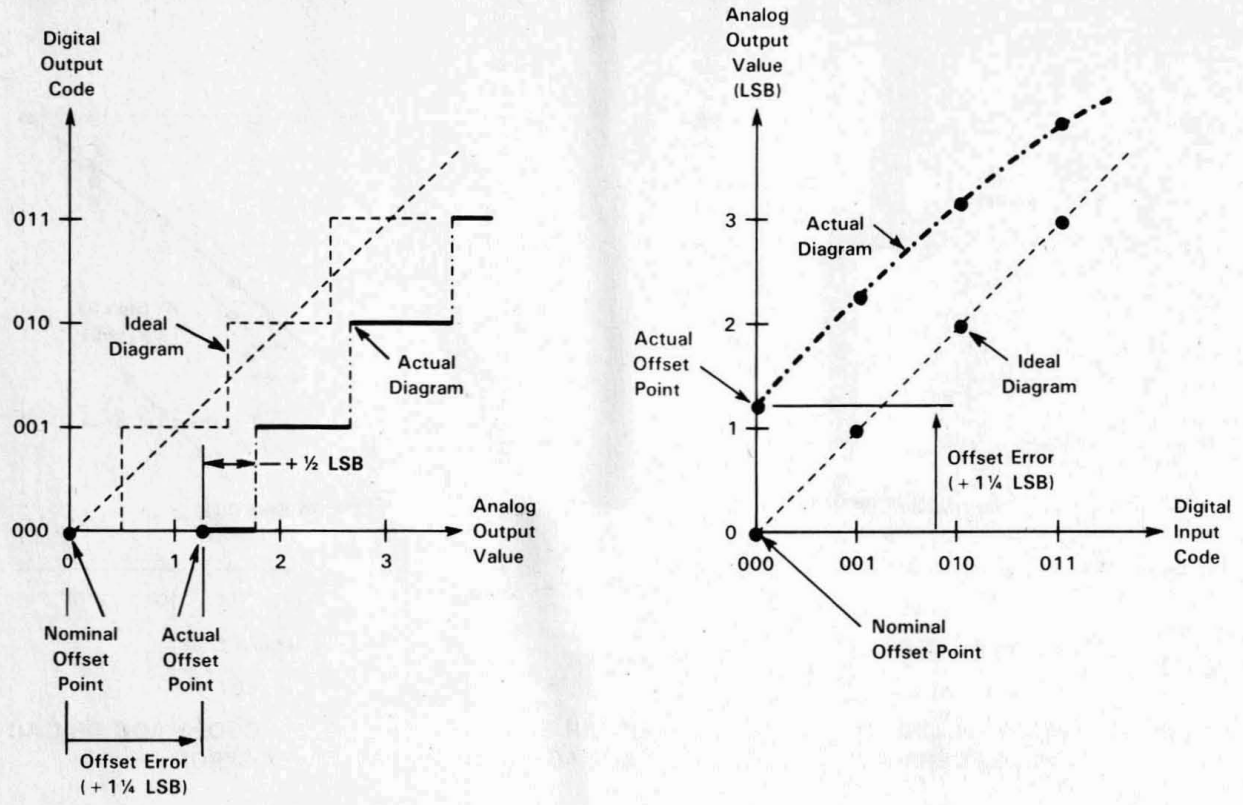

FIGURE 15. OFFSET ERROR OF A LINEAR 3-BIT NATURAL BINARY CODE CONVERTER (SPECIFIED AT STEP 000)

Quantization Error, Inherent (of an ideal ADC)

Within a step, the maximum (positive or negative) possible deviation of the actual analog input value from the nominal midstep value.

NOTE 1: This error follows necessarily from the quantization procedure. For a linear ADC, its value equals ±1/2 LSB. (See Figure 1.)

NOTE 2: The term "resolution error" for the "inherent quantization error" is deprecated, because "resolution" as a design parameter has only a nominal value.

Rollover Error (of an ADC with decimal output and auto-polarity) (E_{RO})

The difference in output readings with the analog input switched between positive and negative values of the same magnitude (close to full scale).

Total Error (of a linear ADC) (E_T)

The maximum difference (positive or negative) between an analog value and the nominal midstep value within any step. (See Figure 16a.)

NOTE 1: If this error is expressed as a relative value, the term "relative accuracy error" should be used instead of "absolute accuracy error".

NOTE 2: This error includes contributions from offset error, gain error, linearity error, and the inherent quantization error.

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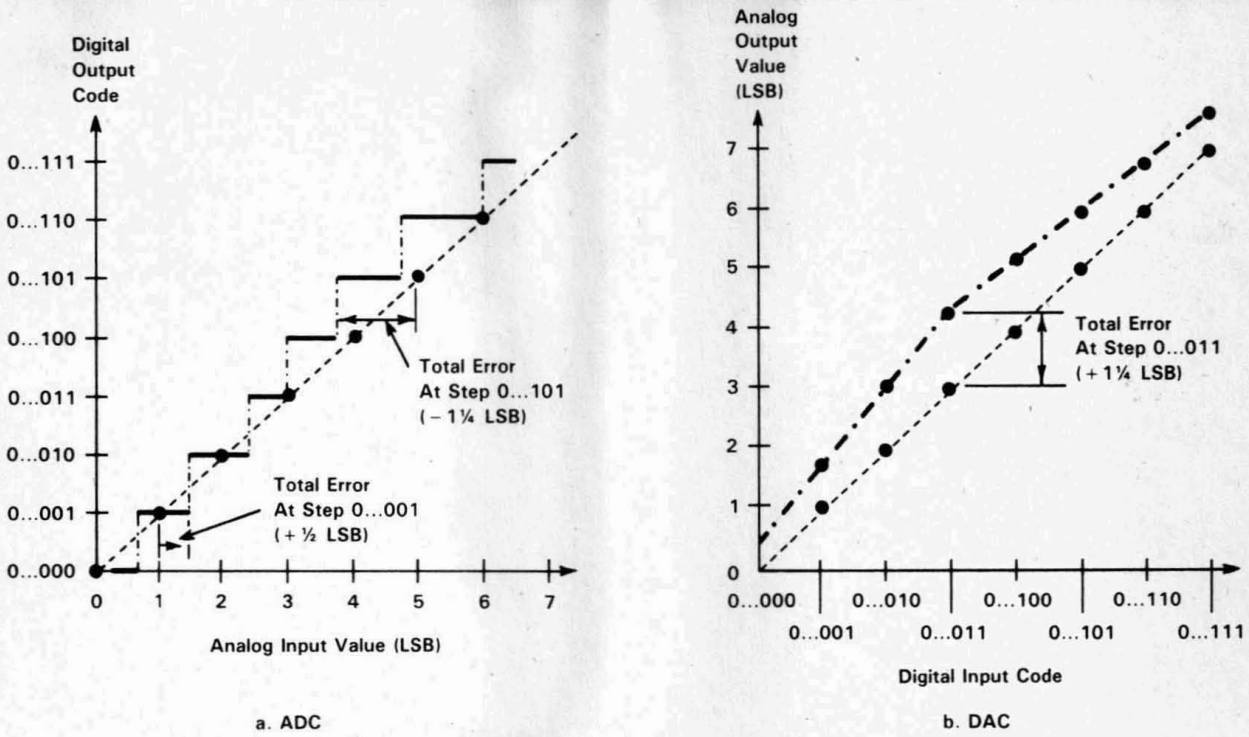

FIGURE 16. ABSOLUTE ACCURACY ERROR, TOTAL ERROR OF A LINEAR ADC OR DAC

Total Error (of a linear DAC) (E_T)

The difference (positive or negative) between the actual step value and the nominal step value for any step. (See Figure 16b.)

NOTE 1: If this error is expressed as a relative value, the term "relative accuracy error" should be used instead of "absolute accuracy error".

NOTE 2: This error includes contributions from offset error, gain error, and linearity error.

Zero-Scale Error (of a linear ADC or DAC) (E_{ZS})

The difference between the actual midstep value or step value and the nominal midstep value or step value, respectively, at specified zero scale.

NOTE: Normally, this error specification is applied to converters that have no arrangement for an external adjustment of offset error and gain error.

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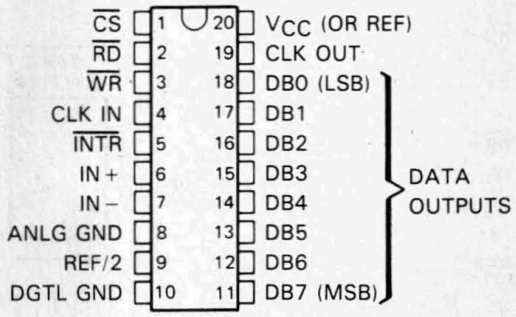
ADC0803, ADC0805
8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH DIFFERENTIAL INPUTS

D2754, NOVEMBER 1983—REVISED SEPTEMBER 1986

- **8-Bit Resolution**
- **Ratiometric Conversion**
- **100-μs Conversion Time**
- **135-ns Access Time**
- **Guaranteed Monotonicity**
- **High Reference Ladder Impedance . . . 8 kΩ Typical**
- **No Zero Adjust Requirement**
- **On-Chip Clock Generator**
- **Single 5-V Power Supply**
- **Operates with Microprocessor or as Stand-Alone**
- **Designed to be Interchangeable with National Semiconductor and Signetics ADC0803 and ADC0805**

N PACKAGE
(TOP VIEW)



description

The ADC0803 and ADC0805 are CMOS 8-bit, successive-approximation, analog-to-digital converters that use a modified potentiometric (256R) ladder. These devices are designed to operate from common microprocessor control buses with the three-state output latches driving the data bus. The devices can be made to appear to the microprocessor as a memory location or an I/O port. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

A differential analog voltage input allows increased common-mode rejection and offset of the zero-input analog voltage value. Although a reference input (REF/2) is available to allow 8-bit conversion over smaller analog voltage spans or to make use of an external reference, ratiometric conversion is possible with the REF/2 input open. Without an external reference, the conversion takes place over a span from V_{CC} to analog ground (ANLG GND). The devices can operate with an external clock signal or, with an additional resistor and capacitor, using an on-chip clock generator.

The ADC0803I and ADC0805I are characterized for operation from −40°C to 85°C. The ADC0803C and ADC0805C are characterized for operation from 0°C to 70°C.

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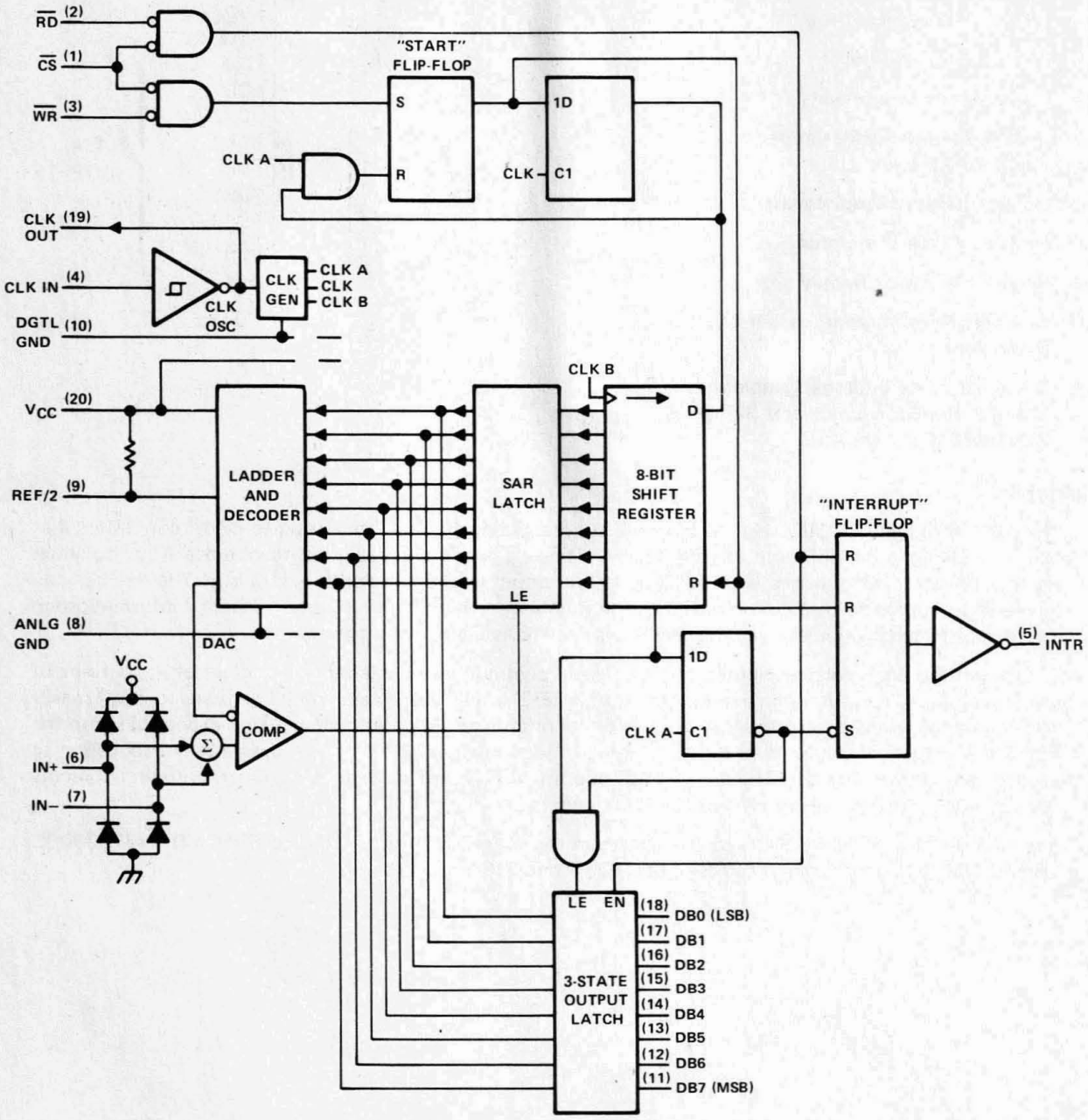
functional block diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range: $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ . . . . . −0.3 V to 18 V
Other inputs . . . . . −0.3 V to V_{CC} +0.3 V
Output voltage range . . . . . −0.3 V to V_{CC} +0.3 V
Operating free-air temperature range: ADC080_I . . . . . −40°C to 85°C
ADC080_C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to digital ground (DGTL GND) with DGTL GND and ANLG GND connected together unless otherwise noted.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	6.3	V
Analog input voltage (see Note 2)		−0.05		V_{CC} +0.05	V
Voltage at REF/2 (see Note 3), $V_{REF/2}$		0.25	2.5		V
High-level input voltage at $\overline{CS}$, $\overline{RD}$, or $\overline{WR}$, V_{IH}		2		15	V
Low-level input voltage at $\overline{CS}$, $\overline{RD}$, or $\overline{WR}$, V_{IL}				0.8	V
Analog ground voltage (see Note 4)		−0.05	0	1	V
Clock input frequency (see Note 5), f_{clock}		100	640	1460	kHz
Duty cycle for f_{clock} above 640 kHz (see Note 5)		40%		60%	
Pulse duration, clock input (high or low) for f_{clock} below 640 kHz, t_w(CLK)		275	781		ns
Pulse duration, $\overline{WR}$ input low, t_w(WR)		100			ns
Operating free-air temperature, T_A	ADC080_I	−40		85	°C
	ADC080_C	0		70	

NOTES: 2. When the differential input voltage ($V_{I+} - V_{I-}$) is less than or equal to 0 V, the output code is 0000 0000.
3. The internal reference voltage is equal to the voltage applied to REF/2 or approximately equal to one-half of the V_{CC} when REF/2 is left open. The voltage at REF/2 should be one-half the full-scale differential input voltage between the analog inputs. Thus, the differential input voltage range when REF/2 is open and V_{CC} = 5 V is 0 V to 5 V. $V_{REF/2}$ for an input voltage range from 0.5 V to 3.5 V (full-scale differential voltage of 3 V) is 1.5 V.
4. These values are with respect to DGTL GND.
5. Total unadjusted error is specified only at an f_{clock} of 640 kHz with a duty cycle of 40% to 60% (pulse duration 625 ns to 937 ns). For frequencies above this limit or pulse duration below 625 ns, error may increase. The duty cycle limits should be observed for an f_{clock} greater than 640 kHz. Below 640 kHz, this duty cycle limit can be exceeded provided t_w(CLK) remains within limits.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5 V, f_{clock} = 640 kHz, $V_{REF/2}$ = 2.5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	All outputs	V_{CC} = 4.75 V,	I_{OH} = −360 μA	2.4			V
		DB and $\overline{INTR}$	V_{CC} = 4.75 V,	I_{OH} = −10 μA	4.5			
V_{OL}	Low-level output voltage	Data outputs	V_{CC} = 4.75 V,	I_{OL} = 1.6 mA			0.4	V
		$\overline{INTR}$ output	V_{CC} = 4.75 V,	I_{OL} = 1 mA			0.4	
		CLK OUT	V_{CC} = 4.75 V,	I_{OL} = 360 μA			0.4	
V_{T+}	Clock positive-going threshold voltage				2.7	3.1	3.5	V
V_{T-}	Clock negative-going threshold voltage				1.5	1.8	2.1	V
$V_{T+} - V_{T-}$	Clock input hysteresis				0.6	1.3	2	V
I_{IH}	High-level input current					0.005	1	μA
I_{IL}	Low-level input current					−0.005	−1	μA
I_{OZ}	Off-state output current		V_O = 0				−3	μA
			V_O = 5 V				3	
I_{OHS}	Short-current output current	Output high	V_O = 0,	T_A = 25°C	−4.5	−6		mA
I_{OLS}	Short-circuit output current	Output low	V_O = 5 V,	T_A = 25°C	9	16		mA
I_{CC}	Supply current plus reference current		$V_{REF/2}$ = open, $\overline{CS}$ = 5 V	T_A = 25°C,		1.1	1.8	mA
$R_{REF/2}$	Input resistance to reference ladder		See Note 6		2.5	8		kΩ
C_i	Input capacitance (control)					5	7.5	pF
C_o	Output capacitance (DB)					5	7.5	pF

NOTE 6: Resistance is calculated from the current drawn from a 5-V supply applied to pins 8 and 9.

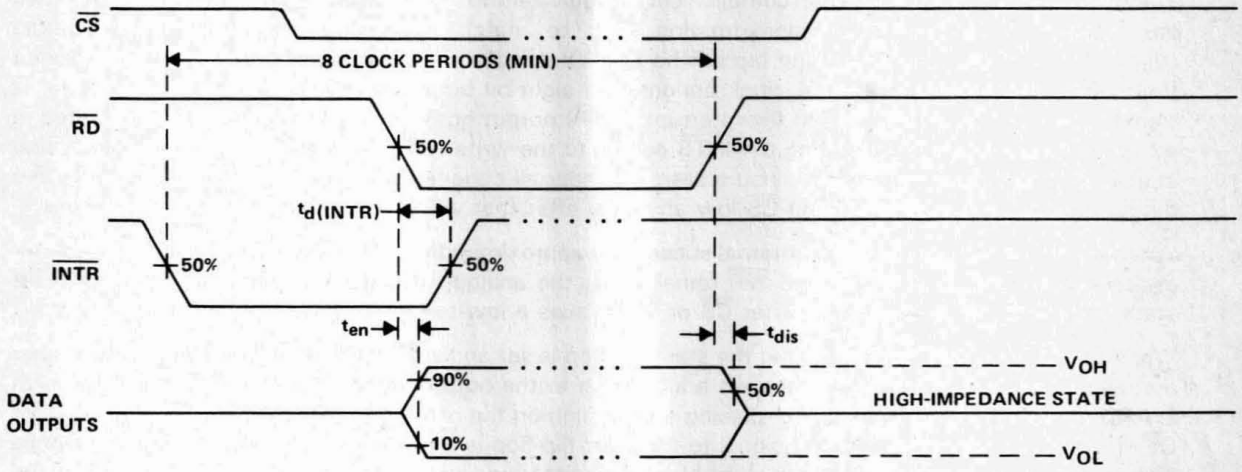
operating characteristics over recommended operating free-air temperature, V_{CC} = 5 V, $V_{REF/2}$ = 2.5 V, f_{clock} = 640 kHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
	Supply-voltage-variation error		V_{CC} = 4.5 V to 5.5 V,	See Note 7		±1/16	±1/8	LSB
	Total adjusted error	ADC0803	With full-scale adjust,	See Notes 7 and 8			±1/4	LSB
							±1/2	
	Total unadjusted error	ADC0805	$V_{REF/2}$ = 2.5 V,	See Notes 7 and 8			±1/2	LSB
			$V_{REF/2}$ open,	See Notes 7 and 8			±1	
	DC common-mode error		See Notes 7 and 8			±1/16	±1/8	LSB
t_{en}	Output enable time		T_A = 25°C,	C_L = 100 pF		135	200	ns
t_{dis}	Output disable time		T_A = 25°C, C_L = 10 pF,	R_L = 10 kΩ		125	200	ns
$t_{d(INTR)}$	Delay time to reset $\overline{INTR}$		T_A = 25°C			300	450	ns
t_{conv}	Conversion cycle time		f_{clock} = 100 kHz to 1.46 MHz, T_A = 25°C,	See Note 9	66		73	clock cycles
CR	Free-running conversion rate		$\overline{INTR}$ connected to $\overline{WR}$,	$\overline{CS}$ at 0 V			8770	conv/s

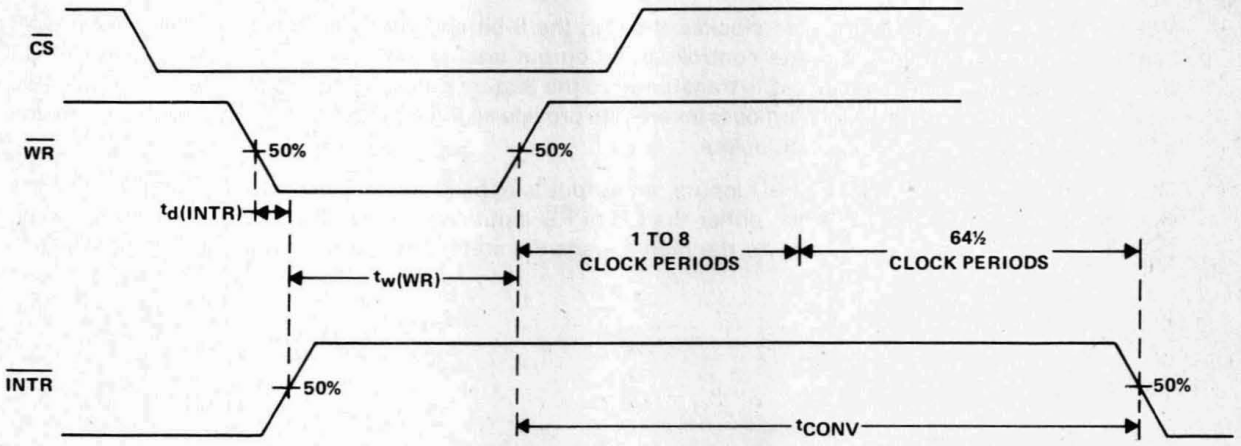
†All typical values are at T_A = 25°C.

NOTES: 7. These parameters are specified over the recommended analog input voltage range.
8. All errors are measured with reference to an ideal straight line through the end-points of the analog-to-digital transfer characteristic.
9. Although internal conversion is completed in 64 clock periods, a $\overline{CS}$ or $\overline{WR}$ low-to-high transition is followed by 1 to 8 clock periods before conversion starts. After conversion is complete, part of another clock period is required before a high-to-low transition of $\overline{INTR}$ completes the cycle.

PARAMETER MEASUREMENT INFORMATION



READ OPERATION TIMING DIAGRAM



WRITE OPERATION TIMING DIAGRAM

PRINCIPLES OF OPERATION

The ADC0803 and ADC0805 each contain a circuit equivalent to a 256-resistor network. Analog switches are sequenced by successive-approximation logic to match an analog differential input voltage ($V_{in+} - V_{in-}$) to a corresponding tap on the 256R network. The most significant bit (MSB) is tested first. After eight comparisons (64 clock periods), an eight-bit binary code (1111 1111 = full scale) is transferred to an output latch and the interrupt ($\overline{INTR}$) output goes low. The device can be operated in a free-running mode by connecting the $\overline{INTR}$ output to the write ($\overline{WR}$) input and holding the conversion start ($\overline{CS}$) input at a low level. To ensure start-up under all conditions, a low-level $\overline{WR}$ input is required during the power-up cycle. Taking $\overline{CS}$ low any time after that will interrupt a conversion in process.

When the $\overline{WR}$ input goes low, the internal successive approximation register (SAR) and 8-bit shift register are reset. As long as both $\overline{CS}$ and $\overline{WR}$ remain low, the analog-to-digital converter remains in a reset state. One to eight clock periods after $\overline{CS}$ or $\overline{WR}$ makes a low-to-high transition, conversion starts.

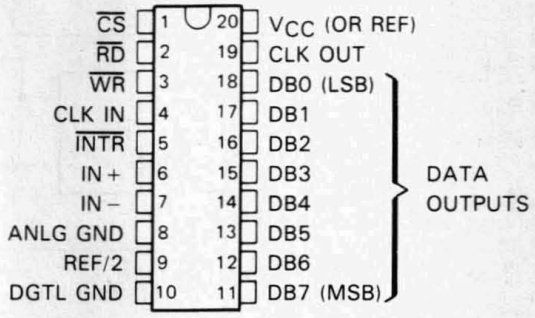
When the $\overline{CS}$ and $\overline{WR}$ inputs are low, the start flip-flop is set and the interrupt flip-flop and 8-bit register are reset. The next clock pulse transfers a logic high to the output of the start flip-flop. The logic high is ANDed with the next clock pulse, placing a logic high on the reset input of the start flip-flop. If either $\overline{CS}$ or $\overline{WR}$ have gone high, the set signal to the start flip-flop is removed, causing it to be reset. A logic high is placed on the D input of the eight-bit shift register and the conversion process is started. If the $\overline{CS}$ and $\overline{WR}$ inputs are still low, the start flip-flop, the 8-bit shift register, and the SAR remain reset. This action allows for wide $\overline{CS}$ and $\overline{WR}$ inputs, with conversion starting from one to eight clock periods after one of the inputs goes high.

When the logic high input has been clocked through the 8-bit shift register, which completes the SAR search, it is applied to an AND gate controlling the output latches and to the D input of a flip-flop. On the next clock pulse, the digital word is transferred to the 3-state output latches and the interrupt flip-flop is set. The output of the interrupt flip-flop is inverted to provide an $\overline{INTR}$ output that is high during conversion and low when the conversion is complete.

When a low is at both the $\overline{CS}$ and $\overline{RD}$ inputs, an output is applied to the DB0 through DB7 outputs and the interrupt flip-flop is reset. When either the $\overline{CS}$ or $\overline{RD}$ inputs return to a high state, the DB0 through DB7 outputs are disabled (returned to the high-impedance state). The interrupt flip-flop remains reset.

- **8-Bit Resolution**
- **Ratiometric Conversion**
- **100-μs Conversion Time**
- **135-ns Access Time**
- **No Zero Adjust Requirement**
- **On-Chip Clock Generator**
- **Single 5-V Power Supply**
- **Operates with Microprocessor or as Stand-Alone**
- **Designed to be Interchangeable with National Semiconductor and Signetics ADC0804**

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The ADC0804 is a CMOS 8-bit successive-approximation analog-to-digital converter that uses a modified potentiometric (256R) ladder. The ADC0804 is designed to operate from common microprocessor control buses, with the three-state output latches driving the data bus. The ADC0804 can be made to appear to the microprocessor as a memory location or an I/O port. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

A differential analog voltage input allows increased common-mode rejection and offset of the zero-input analog voltage value. Although a reference input (REF/2) is available to allow 8-bit conversion over smaller analog voltage spans or to make use of an external reference, ratiometric conversion is possible with the REF/2 input open. Without an external reference, the conversion takes place over a span from V_{CC} to analog ground (ANLG GND). The ADC0804 can operate with an external clock signal or, with an additional resistor and capacitor, can operate using an on-chip clock generator.

The ADC0804I is characterized for operation from −40°C to 85°C. The ADC0804C is characterized for operation from 0°C to 70°C.

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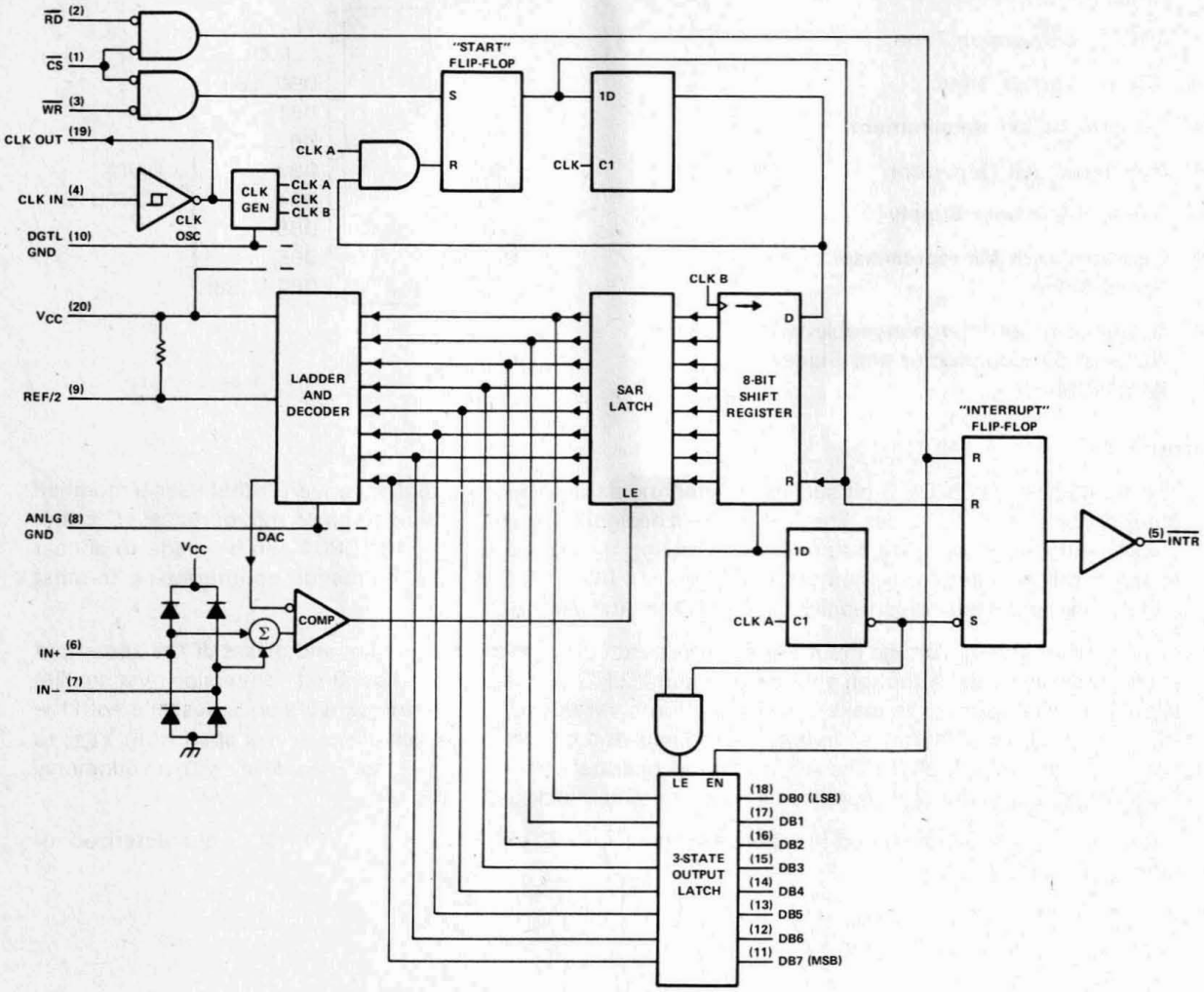
functional block diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range: $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ . . . . . −0.3 V to 18 V
other inputs . . . . . −0.3 V to V_{CC} + 0.3 V
Output voltage range . . . . . −0.3 V to V_{CC} + 0.3 V
Operating free-air temperature range: ADC0804I . . . . . −40°C to 85°C
ADC0804C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to digital ground (DGTL GND) with DGTL GND and ANLG GND connected together (unless otherwise noted).

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	6.3	V
Voltage at REF/2, $V_{REF/2}$ (see Note 2)		0.25	2.5		V
High-level input voltage at $\overline{CS}$, $\overline{RD}$, or $\overline{WR}$, V_{IH}		2		15	V
Low-level input voltage at $\overline{CS}$, $\overline{RD}$, or $\overline{WR}$, V_{IL}				0.8	V
Analog ground voltage (see Note 3)		−0.05	0	1	V
Analog input voltage (see Note 4)		−0.05		V_{CC}+0.05	V
Clock input frequency, f_{clock} (see Note 5)		100	640	1460	kHz
Duty cycle for $f_{clock} \geq 640$ kHz (see Note 5)		40		60	%
Pulse duration clock input (high or low) for $f_{clock} < 640$ kHz, $t_{w(CLK)}$ (see Note 5)		275	781		ns
Pulse duration, $\overline{WR}$ input low (start conversion), $t_{w(WR)}$		100			ns
Operating free-air temperature, T_A	ADC0804I	−40		85	°C
	ADC0804C	0		70	

NOTES: 2. The internal reference voltage is equal to the voltage applied to REF/2, or approximately equal to one-half of the V_{CC} when REF/2 is left open. The voltage at REF/2 should be one-half the full-scale differential input voltage between the analog inputs. Thus, the differential input voltage when REF/2 is open and V_{CC} = 5 V is 0 to 5 V. VREF/2 for an input voltage range from 0.5 V to 3.5 V (full-scale differential voltage of 3 V) is 1.5 V.
3. These values are with respect to DGTL GND.
4. When the differential input voltage ($V_{IN+} - V_{in-}$) is less than or equal to 0 V, the output code is 0000 0000.
5. Total unadjusted error is specified only at an f_{clock} of 640 kHz with a duty cycle of 40% to 60% (pulse duration 625 ns to 937 ns). For frequencies above this limit or pulse duration below 625 ns, error may increase. The duty cycle limits should be observed for an f_{clock} greater than 640 kHz. Below 640 kHz, this duty cycle limit can be exceeded provided $t_{w(CLK)}$ remains within limits.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5 V, f_{clock} = 640 kHz, REF/2 = 2.5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	All outputs	V_{CC} = 4.75 V, I_{OH} = −360 μA	2.4			V
		DB and $\overline{INTR}$	V_{CC} = 4.75 V, I_{OH} = −10 μA	4.5			
V_{OL}	Low-level output voltage	Data outputs	V_{CC} = 4.75 V, I_{OL} = 1.6 mA			0.4	V
		$\overline{INTR}$ output	V_{CC} = 4.75 V, I_{OL} = 1 mA			0.4	
		CLK OUT	V_{CC} = 4.75 V, I_{OL} = 360 μA			0.4	
V_{T+}	Clock positive-going threshold voltage			2.7	3.1	3.5	V
V_{T-}	Clock negative-going threshold voltage			1.5	1.8	2.1	V
$V_{T+} - V_{T-}$	Clock input hysteresis			0.6	1.3	2	V
I_{IH}	High-level input current				0.005	1	μA
I_{IL}	Low-level input current				−0.005	−1	μA
I_{OZ}	Off-state output current		V_O = 0			−3	μA
			V_O = 5 V			3	
I_{OHS}	Short-circuit output current	Output high	V_O = 0, T_A = 25°C	−4.5	−6		mA
I_{OLS}	Short-circuit output current	Output low	V_O = 5 V, T_A = 25°C	9	16		mA
I_{CC}	Supply current plus reference current		REF/2 open, $\overline{CS}$ at 5 V, T_A = 25°C		1.9	2.5	mA
$R_{REF/2}$	Input resistance to reference ladder		See Note 6	1	1.3		kΩ
C_i	Input capacitance (control)				5	7.5	pF
C_o	Output capacitance (DB)				5	7.5	pF

operating characteristics over recommended operating free-air temperature range, V_{CC} = 5 V, $V_{REF/2}$ = 2.5 V, f_{clock} = 640 kHz (unless otherwise noted)

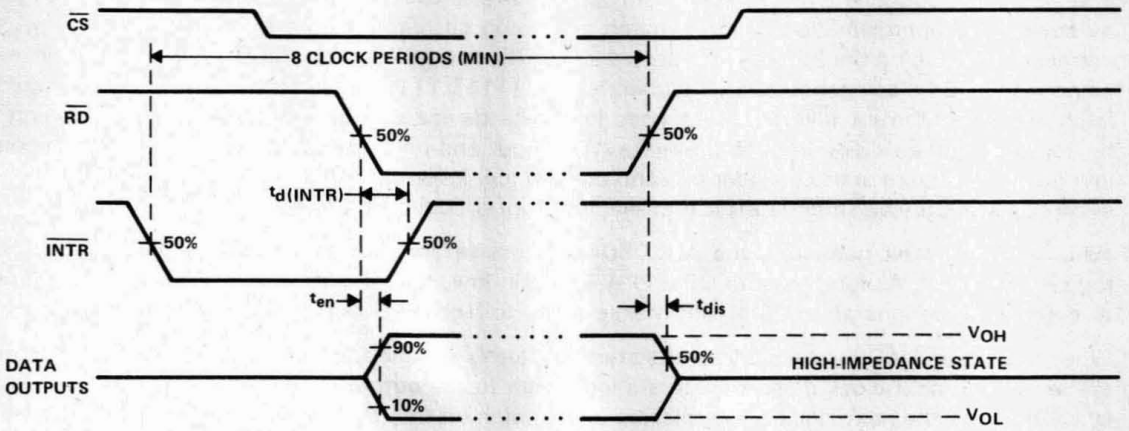
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	Supply-voltage-variation error (See Notes 2 and 7)	V_{CC} = 4.5 V to 5.5 V		±1/16	±1/8	LSB
	Total unadjusted error (See Notes 7 and 8)	$V_{REF/2}$ = 2.5 V			±1	LSB
	DC common-mode error (See Note 8)			±1/16	±1/8	LSB
t_{en}	Output enable time	C_L = 100 pF		135	200	ns
t_{dis}	Output disable time	C_L = 10 pF, R_L = 10 kΩ		125	200	ns
$t_{d(INTR)}$	Delay time to reset $\overline{INTR}$			300	450	ns
t_{conv}	Conversion cycle time (See Note 9)	f_{clock} = 100 kHz to 1.46 MHz	65½		72½	clock cycles
	Conversion time		103		114	μs
CR	Free-running conversion rate	$\overline{INTR}$ connected to $\overline{WR}$, $\overline{CS}$ at 0 V			8827	conv/s

†All typical values are at T_A = 25°C.

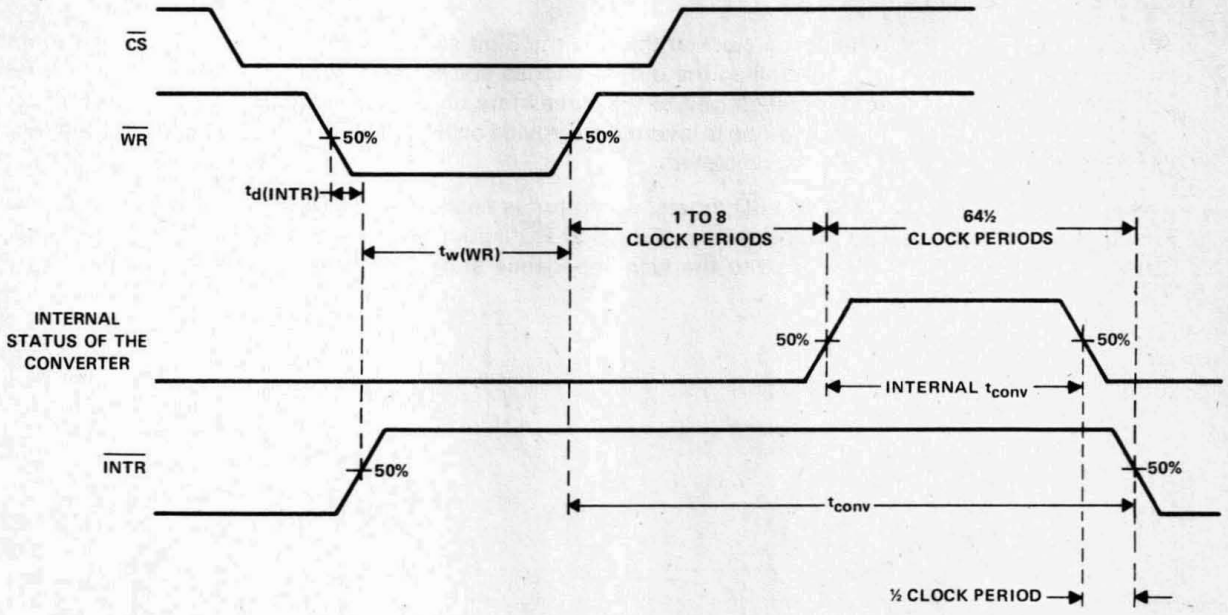
NOTES: 2. The internal reference voltage is equal to the voltage applied to REF/2, or approximately equal to one-half of the V_{CC} when REF/2 is left open. The voltage at REF/2 should be one-half the full-scale differential input voltage between the analog inputs. Thus, the differential input voltage when REF/2 is open and V_{CC} = 5 V is 0 to 5 V. $V_{REF/2}$ for an input voltage range from 0.5 V to 3.5 V (full-scale differential voltage of 3 V) is 1.5 V.

6. The resistance is calculated from the current drawn from a 5-V supply applied to pins 8 and 9.
7. These parameters are specified for the recommended analog input voltage range.
8. All errors are measured with reference to an ideal straight line through the end-points of the analog-to-digital transfer characteristic.
9. Although internal conversion is completed in 64 clock periods, a $\overline{CS}$ or $\overline{WR}$ low-to-high transition is followed by 1 to 8 clock periods before conversion starts. After conversion is completed, part of another clock period is required before a high-to-low transition of $\overline{INTR}$ completes the cycle.

timing diagrams



READ OPERATION TIMING DIAGRAM



WRITE OPERATION TIMING DIAGRAM

PRINCIPLES OF OPERATION

The ADC0804 contains a circuit equivalent to a 256-resistor network. Analog switches are sequenced by successive approximation logic to match an analog differential input voltage ($V_{in+} - V_{in-}$) to a corresponding tap on the 256-resistor network. The most-significant bit (MSB) is tested first. After eight comparisons (64 clock periods), an 8-bit binary code (1111 1111 = full scale) is transferred to an output latch and the interrupt ($\overline{INTR}$) output goes low. The device can be operated in a free-running mode by connecting the $\overline{INTR}$ output to the write ($\overline{WR}$) input and holding the conversion start ($\overline{CS}$) input at a low level. To ensure start-up under all conditions, a low-level $\overline{WR}$ input is required during the power-up cycle. Taking $\overline{CS}$ low anytime after that will interrupt a conversion in process.

When the $\overline{WR}$ input goes low, the ADC0804 successive approximation register (SAR) and 8-bit shift register are reset. As long as both $\overline{CS}$ and $\overline{WR}$ remain low, the ADC0804 remains in a reset state. One to eight clock periods after $\overline{CS}$ or $\overline{WR}$ makes a low-to-high transition, conversion starts.

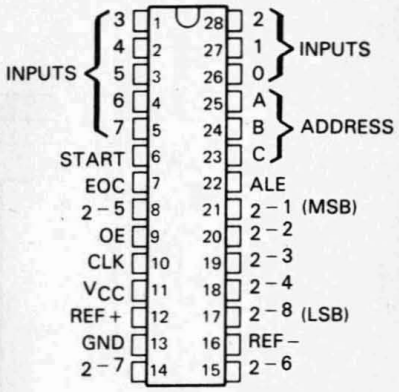
When the $\overline{CS}$ and $\overline{WR}$ inputs are low, the start flip-flop is set and the interrupt flip-flop and 8-bit register are reset. The next clock pulse transfers a logic high to the output of the start flip-flop. The logic high is ANDed with the next clock pulse, placing a logic high on the reset input of the start flip-flop. If either $\overline{CS}$ or $\overline{WR}$ have gone high, the set signal to the start flip-flop is removed, causing it to be reset. A logic high is placed on the D input of the 8-bit shift register and the conversion process is started. If the $\overline{CS}$ and $\overline{WR}$ inputs are still low, the start flip-flop, the 8-bit shift register, and the SAR remain reset. This action allows for wide $\overline{CS}$ and $\overline{WR}$ inputs with conversion starting from one to eight clock periods after one of the inputs goes high.

When the logic high input has been clocked through the 8-bit shift register, completing the SAR search, it is applied to an AND gate controlling the output latches and to the D input of a flip-flop. On the next clock pulse, the digital word is transferred to the three-state output latches and the interrupt flip-flop is set. The output of the interrupt flip-flop is inverted to provide an $\overline{INTR}$ output that is high during conversion and low when the conversion is completed.

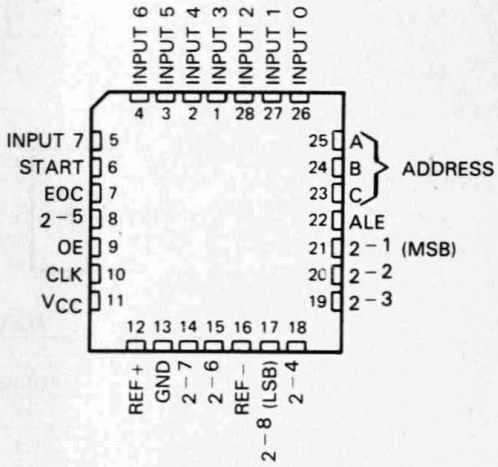
When a low is at both the $\overline{CS}$ and $\overline{RD}$ inputs, an output is applied to the DB0 through DB7 outputs and the interrupt flip-flop is reset. When either the $\overline{CS}$ or $\overline{RD}$ inputs return to a high state, the DB0 through DB7 outputs are disabled (returned to the high-impedance state). The interrupt flip-flop remains reset.

- **Total Unadjusted Error . . . ±0.75 LSB Max for ADC0808 and ±1.25 LSB Max for ADC0809**
- **Resolution of 8 Bits**
- **100 μs Conversion Time**
- **Ratiometric Conversion**
- **Monotonicity Over the Entire A/D Conversion Range**
- **No Missing Codes**
- **Easy Interface with Microprocessors**
- **Latched 3-State Outputs**
- **Latched Address Inputs**
- **Single 5-V Supply**
- **Low Power Consumption**
- **Designed to be Interchangeable with National Semiconductor ADC0808, ADC0809**

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The ADC0808 and ADC0809 are monolithic CMOS devices with an 8-channel multiplexer, an 8-bit analog-to-digital (A/D) converter, and microprocessor-compatible control logic. The 8-channel multiplexer can be controlled by a microprocessor through a 3-bit address decoder with address load to select any one of eight single-ended analog switches connected directly to the comparator. The 8-bit A/D converter uses the successive-approximation conversion technique featuring a high-impedance threshold detector, a switched-capacitor array, a sample-and-hold, and a successive-approximation register (SAR). Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The comparison and converting methods used eliminate the possibility of missing codes, nonmonotonicity, and the need for zero or full-scale adjustment. Also featured are latched 3-state outputs from the SAR and latched inputs to the multiplexer address decoder. The single 5-V supply and low power requirements make the ADC0808 and ADC0809 especially useful for a wide variety of applications. Ratiometric conversion is made possible by access to the reference voltage input terminals.

The ADC0808 and ADC0809 are characterized for operation from −40°C to 85°C.

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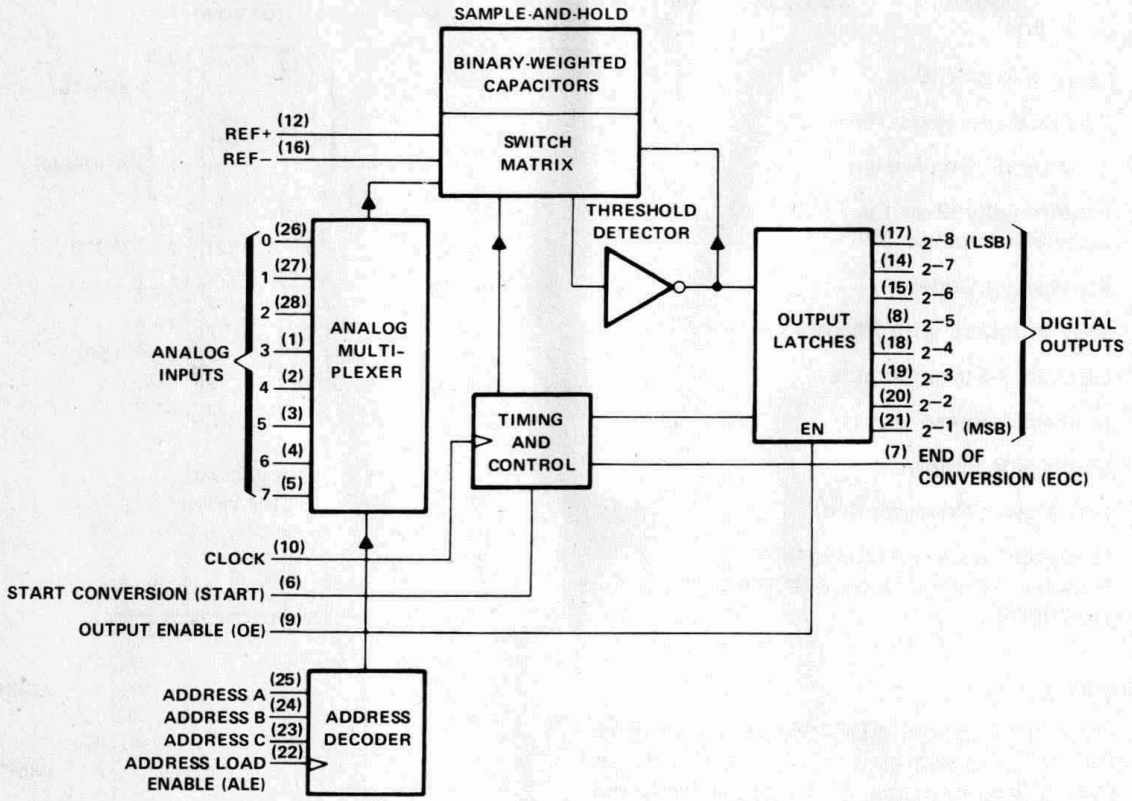
functional block diagram (positive logic)



MULTIPLEXER FUNCTION TABLE

INPUTS				SELECTED
ADDRESS			ADDRESS	ANALOG
C	B	A	STROBE	CHANNEL
L	L	L	↑	0
L	L	H	↑	1
L	H	L	↑	2
L	H	H	↑	3
H	L	L	↑	4
H	L	H	↑	5
H	H	L	↑	6
H	H	H	↑	7

H = high level, L = low level
↑ = low-to-high transition

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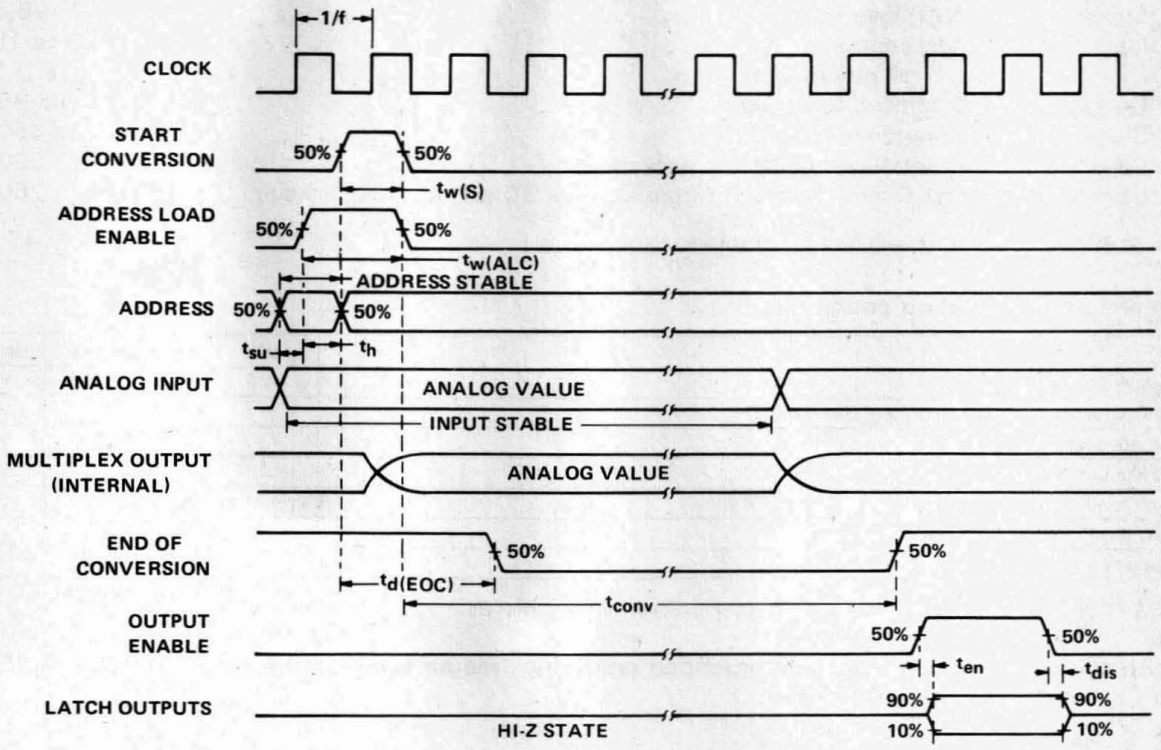
operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range: control inputs . . . . . −0.3 to 15 V
all other inputs . . . . . −0.3 V to V_{CC} + 0.3 V
Operating free-air temperature range . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	6	V
Positive reference voltage, V_{ref+} (see Note 2)		V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{ref-}		0	−0.1	V
Differential reference voltage, $V_{ref+} - V_{ref-}$		5		V
High-level input voltage, V_{IH}	$V_{CC}-1.5$			V
Low-level input voltage, V_{IL}			1.5	V
Operating free-air temperature, T_A	−40		85	°C

NOTE 2: Care must be taken that this rating is observed even during power-up.

electrical characteristics over recommended operating free-air temperature range. V_{CC} = 4.75 V to 5.25 V (unless otherwise noted)

total device

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_O = −360 μA	$V_{CC}-0.4$			V
V_{OL}	Low-level output voltage	Data outputs	I_O = 1.6 mA			0.45	V
		End of conversion	I_O = 1.2 mA			0.45	
I_{OZ}	Off-state (high-impedance-state) output current		$V_O = V_{CC}$			3	μA
			V_O = 0			−3	
I_I	Control input current at maximum input voltage		V_I = 15 V			1	μA
I_{IL}	Low-level control input current		V_I = 0			−1	μA
I_{CC}	Supply current		f_{clock} = 640 kHz		0.3	3	mA
C_i	Input capacitance, control inputs		T_A = 25°C		10	15	pF
C_o	Output capacitance, data outputs		T_A = 25°C		10	15	pF
	Resistance from pin 12 to pin 16				1000		kΩ

analog multiplexer

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{on}	Channel on-state current (see Note 3)	$V_I = V_{CC}$,	f_{clock} = 640 kHz			2	μA
		V_I = 0.1 V,	f_{clock} = 640 kHz			−2	
I_{off}	Channel off-state current	V_{CC} = 5 V, T_A = 25°C	V_I = 5 V		10	200	nA
			V_I = 0		−10	−200	
		V_{CC} = 5 V	V_I = 5 V			1	μA
			V_I = 0			−1	

†Typical values are at V_{CC} = 5 V and T_A = 25°C.
NOTE 3: Channel on-state current is primarily due to the bias current into or out of the threshold detector, and it varies directly with clock frequency.

timing requirements, $V_{CC} = V_{ref+} = 5$ V, $V_{ref-} = 0$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Clock frequency		10	640	1280	kHz
t_{conv}	Conversion time	See Note 4	90	100	116	μs
$t_{w(s)}$	Pulse duration, START		200			ns
$t_{w(ALE)}$	Pulse duration, ALE		200			ns
t_{su}	Setup time, ADDRESS		50			ns
t_h	Hold time, ADDRESS		50			ns
t_d	Delay time, EOC	See Notes 4 and 5	0		14.5	μs

operating characteristics, $T_A = 25°C$, $V_{CC} = V_{ref+} = 5$ V, $V_{ref-} = 0$ V, $f_{clock} = 640$ kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	ADC0808			ADC0809			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
k_{SVS}	Supply voltage sensitivity	$V_{CC} = V_{ref+} = 4.75$ V to 5.25 V, $T_A = -40°C$ to 85°C, See Note 6		±0.05			±0.05		%/V
	Linearity error (see Note 7)			±0.25			±0.5		LSB
	Zero error (see Note 8)			±0.25			±0.25		LSB
	Total unadjusted error (See Note 9)	$T_A = 25°C$		±0.25	±0.5		±0.5		LSB
		$T_A = -40°C$ to 85°C			±0.75			±1.25	
		$T_A = 0°C$ to 70°C						±1	
t_{en}	Output enable time	$C_L = 50$ pF, $R_L = 10$ kΩ		80	250		80	250	ns
t_{dis}	Output disable time	$C_L = 10$ pF, $R_L = 10$ kΩ		105	250		105	250	ns

†Typical values for all except supply voltage sensitivity are at $V_{CC} = 5$ V, and all are at $T_A = 25°C$.

NOTES: 4. Refer to the operating sequence diagram.
5. For clock frequencies other than 640 kHz, $t_{d(EOC)}$ maximum is 8 clock periods plus 2 μs.
6. Supply voltage sensitivity relates to the ability of an analog-to-digital converter to maintain accuracy as the supply voltage varies. The supply and V_{ref+} are varied together and the change in accuracy is measured with respect to full-scale.
7. Linearity error is the maximum deviation from a straight line through the end points of the A/D transfer characteristic.
8. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
9. Total unadjusted error is the maximum sum of linearity error, zero error, and full-scale error.

PRINCIPLES OF OPERATION

The ADC0808 and ADC0809 each consists of an analog signal multiplexer, an 8-bit successive-approximation converter, and related control and output circuitry.

multiplexer

The analog multiplexer selects 1 of 8 single-ended input channels as determined by the address decoder. Address load control loads the address code into the decoder on a low-to-high transition. The output latch is reset by the positive-going edge of the start pulse. Sampling also starts with the positive-going edge of the start pulse and lasts for 32 clock periods. The conversion process may be interrupted by a new start pulse before the end of 64 clock periods. The previous data will be lost if a new start of conversion occurs before the 64th clock pulse. Continuous conversion may be accomplished by connecting the End-of-Conversion output to the start input. If used in this mode an external pulse should be applied after power up to assure start up.

converter

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (Figure 1). In the first phase of the conversion process, the analog input is sampled by closing switch S_C and all S_T switches, and by simultaneously charging all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference voltage. In the switching sequence, all eight capacitors are examined separately until all 8 bits are identified, and then the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 128). Node 128 of this capacitor is switched to the reference voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF−. If the voltage at the summing node is greater than the trip-point of the threshold detector (approximately one-half the V_{CC} voltage), a bit is placed in the output register, and the 128-weight capacitor is switched to REF−. If the voltage at the summing node is less than the trip point of the threshold detector, this 128-weight capacitor remains connected to REF+ through the remainder of the capacitor-sampling (bit-counting) process. The process is repeated for the 64-weight capacitor, the 32-weight capacitor, and so forth down the line, until all bits are counted.

With each step of the capacitor-sampling process, the initial charge is redistributed among the capacitors. The conversion process is successive approximation, but relies on charge redistribution rather than a successive-approximation register (and reference DAC) to count and weigh the bits from MSB to LSB.

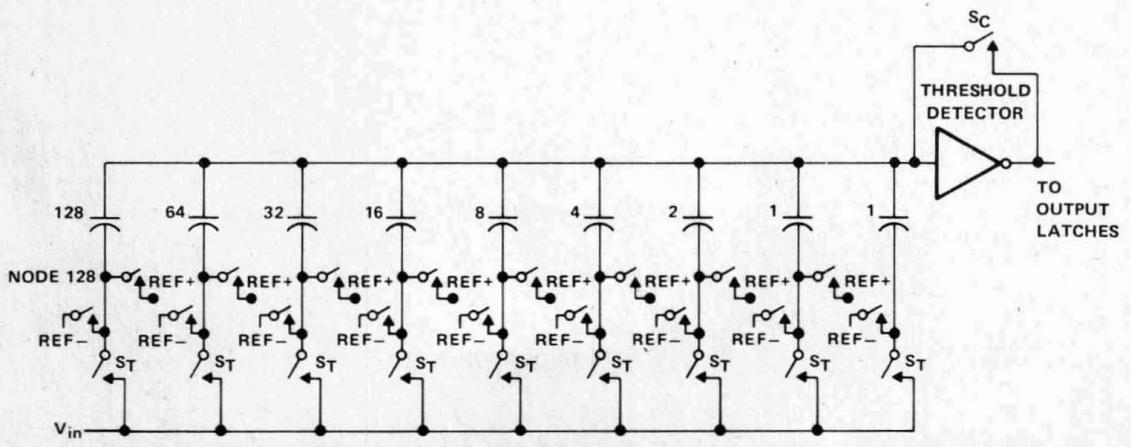
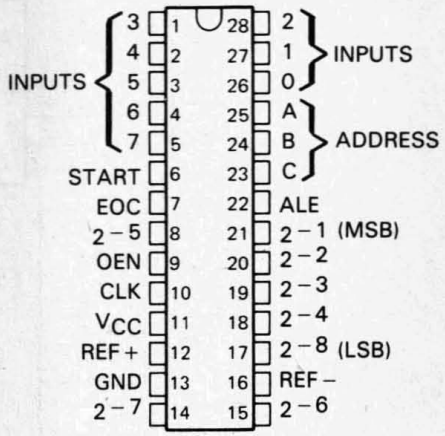


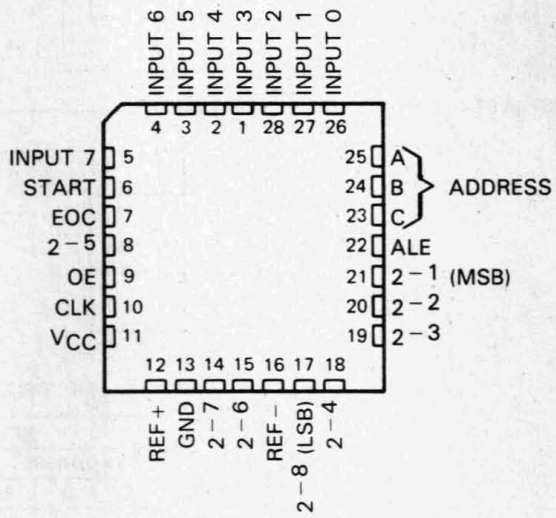
FIGURE 1. SIMPLIFIED MODEL OF THE SUCCESSIVE-APPROXIMATION SYSTEM

- **Total Unadjusted Error . . . ±0.75 LSB Max**
- **Resolution of 8 Bits**
- **100 μs Conversion Time**
- **Ratiometric Conversion**
- **Monotonous Over the Entire A/D Conversion Range**
- **No Missing Codes**
- **Easy Interface with Microprocessors**
- **Latched 3-State Outputs**
- **Latched Address Inputs**
- **Single 5-Volt Supply**
- **Low Power Consumption**
- **Designed to be Interchangeable with National Semiconductor ADC0808CJ**

J
DUAL-IN-LINE PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



description

The ADC0808M is a monolithic CMOS device with an 8-channel multiplexer, an 8-bit analog-to-digital (A/D) converter, and microprocessor-compatible control logic. The 8-channel multiplexer can be controlled by a microprocessor through a 3-bit address decoder with address load to select any one of eight single-ended analog switches connected directly to the comparator. The 8-bit A/D converter uses the successive-approximation conversion technique featuring a high-impedance threshold detector, a switched capacitor array, a sample-and-hold, and a successive-approximation register (SAR). Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The comparison and converting methods used eliminate the possibility of missing codes, nonmonotonicity, and the need for zero or full-scale adjustment. Also featured are latched 3-state outputs from the SAR and latched inputs to the multiplexer address decoder. The single 5-volt supply and low power requirements make the ADC0808M especially useful for a wide variety of applications. Ratiometric conversion is made possible by access to the reference voltage input terminals.

The ADC0808M is characterized for operation over the full military temperature range of −55°C to 125°C.

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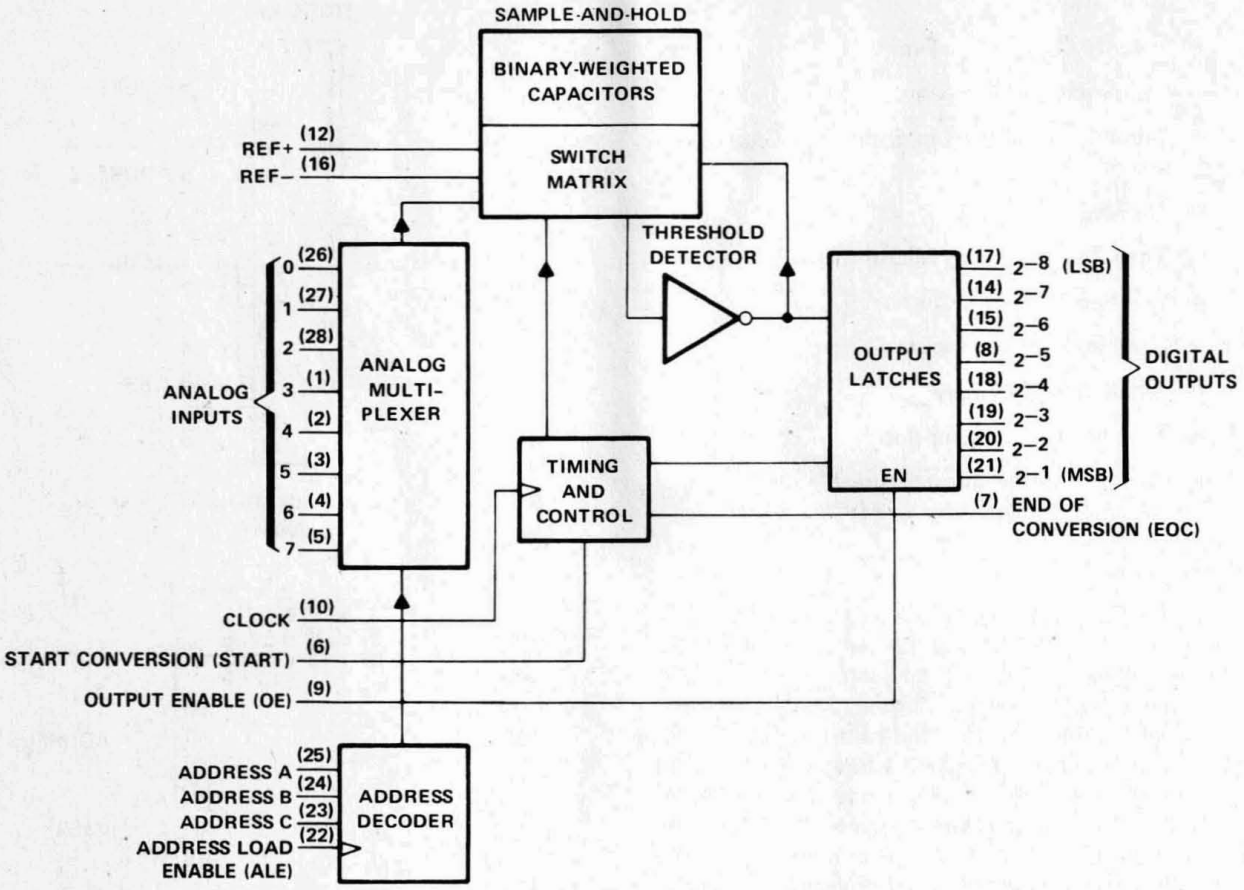
functional block diagram (positive logic)

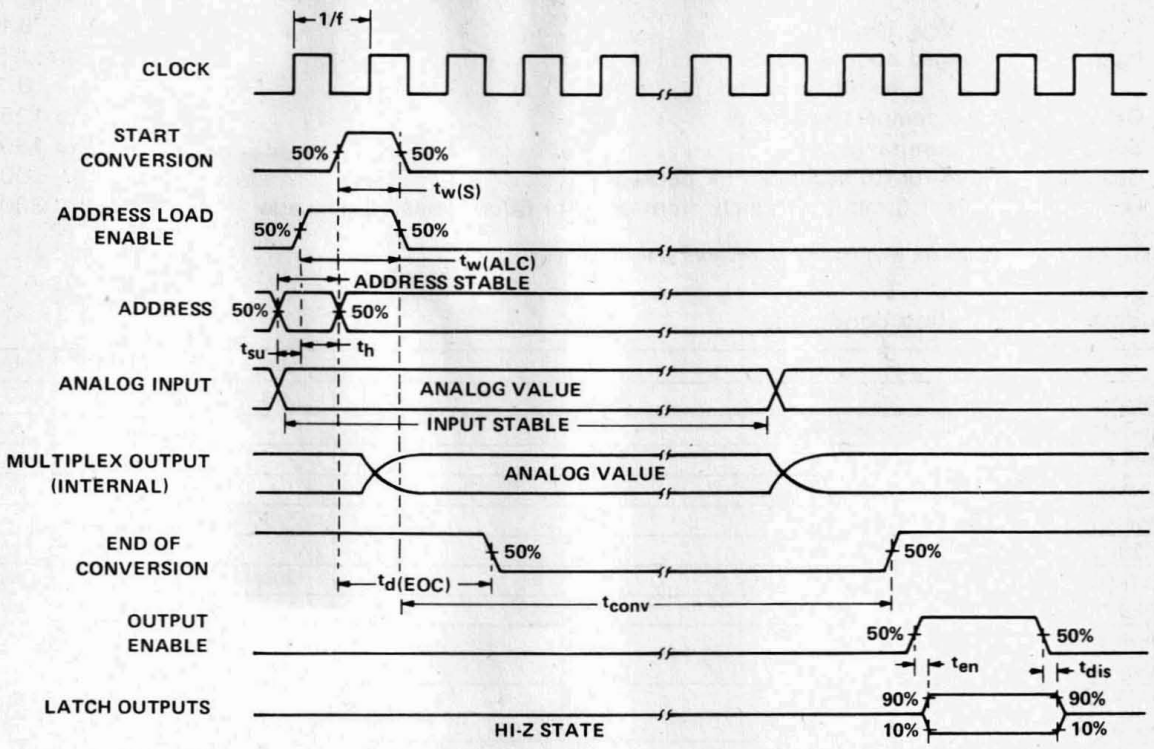


MULTIPLEXER FUNCTION TABLE

INPUTS				SELECTED
ADDRESS			ADDRESS	ANALOG
C	B	A	STROBE	CHANNEL
L	L	L	↑	0
L	L	H	↑	1
L	H	L	↑	2
L	H	H	↑	3
H	L	L	↑	4
H	L	H	↑	5
H	H	L	↑	6
H	H	H	↑	7

H = high level, L = low level
↑ = low-to-high transition

operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range: control inputs . . . . . −0.3 to 15 V
all other inputs . . . . . −0.3 V to V_{CC} + 0.3 V
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	6	V
Positive reference voltage, V_{ref+} (see Note 2)		V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{ref-}		0	−0.1	V
Differential reference voltage, $V_{ref+} - V_{ref-}$		5		V
High-level input voltage, V_{IH}	$V_{CC}-1.5$			V
Low-level input voltage, V_{IL}			1.5	V
Start pulse duration, $t_{w(S)}$	200			ns
Address load control pulse duration, $t_{w(ALC)}$	200			ns
Address setup time, t_{su}	50			ns
Address hold time, t_h	50			ns
Clock frequency, f_{clock}	10	640	1280	kHz
Operating free-air temperature, T_A	−55		125	°C

NOTE 2: Care must be taken that this rating is observed even during power-up.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 4.5 V to 5.5 V (unless otherwise noted)

total device

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_O = −360 μA	V_{CC}−0.4			V
V_{OL}	Low-level output voltage	Data outputs	I_O = 1.6 mA			0.45	V
		End of conversion	I_O = 1.2 mA			0.45	
I_{OZ}	Off-state (high-impedance-state) output current		V_O = V_{CC}			3	μA
			V_O = 0			−3	
I_I	Control input current at maximum input voltage		V_I = 15 V			1	μA
I_{IL}	Low-level control input current		V_I = 0			−1	μA
I_{CC}	Supply current		f_{clock} = 640 kHz		0.3	3	mA
C_i	Input capacitance, control inputs		T_A = 25°C		10		pF
C_o	Output capacitance, data outputs		T_A = 25°C		10		pF
	Resistance from pin 12 to pin 16				1000		kΩ

analog multiplexer

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{on}	Channel on-state current (see Note 3)	V_I = V_{CC},	f_{clock} = 640 kHz			2	μA
		V_I = 0,	f_{clock} = 640 kHz			−2	
I_{off}	Channel off-state current	V_{CC} = 5 V, T_A = 25°C	V_I = 5 V		10	200	nA
			V_I = 0		−10	−200	
		V_{CC} = 5 V	V_I = 5 V			1	μA
			V_I = 0			−1	

† Typical values are at V_{CC} = 5 V and T_A = 25°C.

NOTE 3: Channel on-state current is primarily due to the bias current into or out of the threshold detector, and it varies directly with clock frequency.

timing characteristics, V_{CC} = V_{ref+} = 5 V, V_{ref-} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Clock frequency		10	640	1280	kHz
t_{conv}	Conversion time	See Notes 4 and 5 and Figure 1	90	100	116	μs
t_{enH}	Enable time, high	See Figure 1		150	360	ns
t_{enL}	Enable time, low	See Figure 1		90	250	ns
t_{dis}	Output disable time	See Figure 1		200	405	ns
$t_{w(s)}$	Pulse duration, START		200			ns
$t_{w(ALE)}$	Pulse duration, ALE		200			ns
t_{su}	Setup time, ADDRESS		50			ns
t_h	Hold time, ADDRESS		50			ns
$t_{d(EOC)}$	Delay time, EOC	See Notes 4 and 6 and Figure 1	0		14.5	μs

NOTES: 4. Refer to the operating sequence diagram.

5. For clock frequencies other than 640 kHz, t_{conv} is 57 clock cycles minimum and 74 clock cycles maximum.

6. For clock frequencies other than 640 kHz, $t_{d(EOC)}$ maximum is 8 clock cycles plus 2 μs.

operating characteristics, T_A = 25°C, V_{CC} = V_{ref+} = 5 V, V_{ref-} = 0 V, f_{clock} = 640 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
k_{SVS}	Supply voltage sensitivity	V_{CC} = V_{ref+} = 4.5 V to 5.5 V, T_A = −55°C to 125°C, See Note 7		±0.05		%/V
	Linearity error (see Note 8)			±0.25		LSB
	Zero error (see Note 9)			±0.25		LSB
	Total unadjusted error (see Note 10)	T_A = 25°C		±0.25	±0.5	LSB
		T_A = −55°C to 125°C			±0.75	

† Typical values for all except supply voltage sensitivity are at V_{CC} = 5 V, and all are at T_A = 25°C.

NOTES: 7. Supply voltage sensitivity relates to the ability of an analog-to-digital converter to maintain accuracy as the supply voltage varies. The supply and V_{ref+} are varied together and the change in accuracy is measured with respect to full-scale.

8. Linearity error is the maximum deviation from a straight line through the end points of the A/D transfer characteristic.

9. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.

10. Total unadjusted error is the maximum sum of linearity error, zero error, and full-scale error.

PARAMETER MEASUREMENT INFORMATION

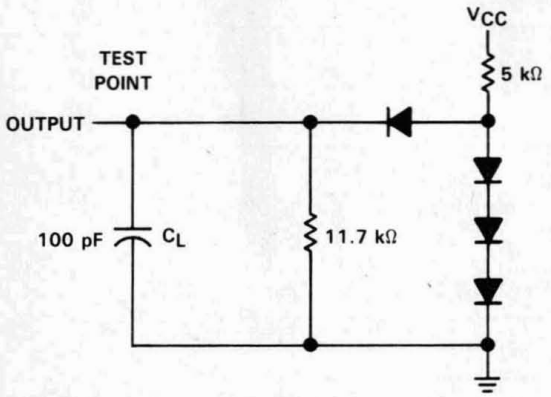


FIGURE 1. TEST CIRCUIT

PRINCIPLES OF OPERATION

The ADC0808M consists of an analog signal multiplexer, an 8-bit successive-approximation converter, and related control and output circuitry.

multiplexer

The analog multiplexer selects 1 of 8 single-ended input channels as determined by the address decoder. Address load control loads the address code into the decoder on a low-to-high transition. The output latch is reset by the positive-going edge of the start pulse. Sampling also starts with the positive-going edge of the start pulse and lasts for 32 clock periods. The conversion process may be interrupted by a new start pulse before the end of 64 clock periods. The previous data will be lost if a new start of conversion occurs before the 64th clock pulse. Continuous conversion may be accomplished by connecting the End-of-Conversion output to the start input. If used in this mode an external pulse should be applied after power up to assure start up.

converter

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (Figure 2). In the first phase of the conversion process, the analog input is sampled by closing switch S_C and all S_T switches, and by simultaneously charging all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference voltage. In the switching sequence, all eight capacitors are examined separately until all 8 bits are identified, and then the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 128). Node 128 of this capacitor is switched to the reference voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF−. If the voltage at the summing node is greater than the trip-point of the threshold detector (approximately one-half the V_{CC} voltage), a bit is placed in the output register, and the 128-weight capacitor is switched to REF−. If the voltage at the summing node is less than the trip point of the threshold detector, this 128-weight capacitor remains connected to REF+ through the remainder of the capacitor-sampling (bit-counting) process. The process is repeated for the 64-weight capacitor, the 32-weight capacitor, and so forth down the line, until all bits are counted.

With each step of the capacitor-sampling process, the initial charge is redistributed among the capacitors. The conversion process is successive approximation, but relies on charge redistribution rather than a successive-approximation register (and reference DAC) to count and weigh the bits from MSB to LSB.

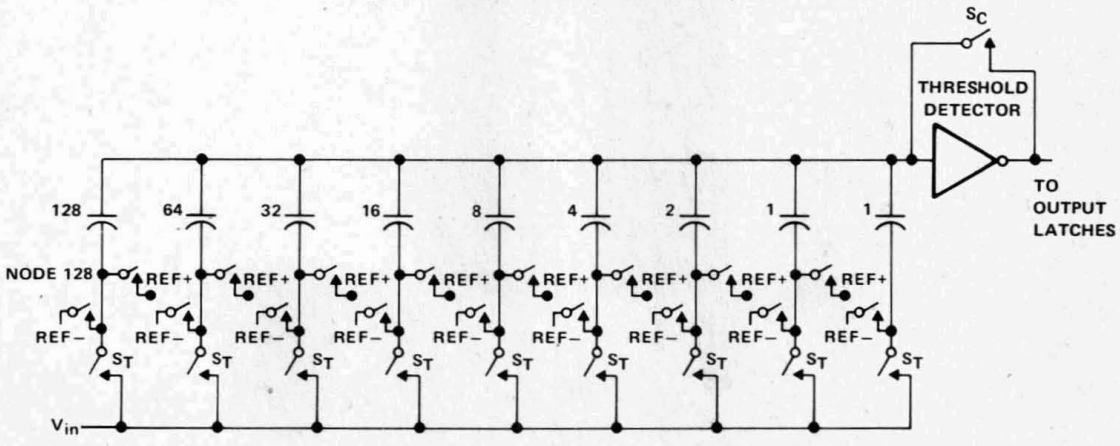


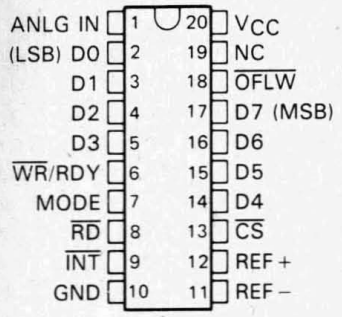
FIGURE 2. SIMPLIFIED MODEL OF THE SUCCESSIVE-APPROXIMATION SYSTEM

TLC0820A, TLC0820B, ADC0820B, ADC0820C
Advanced LinCMOS™ HIGH-SPEED 8-BIT ANALOG-TO-DIGITAL CONVERTERS USING MODIFIED "FLASH" TECHNIQUES

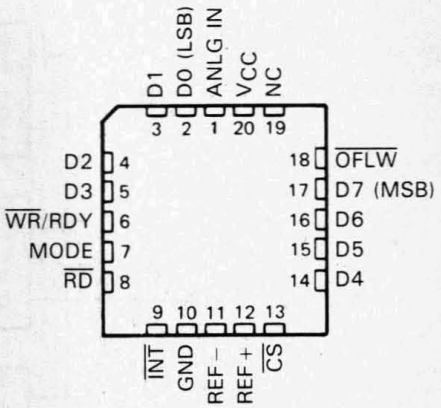
D2873, SEPTEMBER 1986—REVISED FEBRUARY 1989

- **Advanced LinCMOS™ Silicon-Gate Technology**
- **8-Bit Resolution**
- **Differential Reference Inputs**
- **Parallel Microprocessor Interface**
- **Conversion and Access Time Over Temperature Range**
  Write-Read Mode . . . 1.18 μs and 1.92 μs
  Read Mode . . . 2.5 μs Max
- **No External Clock or Oscillator Components Required**
- **On-Chip Track-and-Hold**
- **Low Power Consumption . . . 50 mW Typ**
- **Single 5-V Supply**
- **TLC0820B is Direct Replacement for National Semiconductor ADC0820B/BC and Analog Devices AD7820L/C/U; TLC0820A is Direct Replacement for National Semiconductor ADC0820C/CC and Analog Devices AD7820K/B/T**

ALL TYPES . . . DW OR N PACKAGE
TLC0820_M . . . J PACKAGE
(TOP VIEW)



TLC0820_M . . . FK PACKAGE
TLC0820_I, TLC0820_C . . . FN PACKAGE
ADC0820_CI, ADC0820_C . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

The TLC0820A, TLC0820B, ADC0820B, and ADC0820C are Advanced LinCMOS™ 8-bit analog-to-digital converters each consisting of two 4-bit "flash" converters, a 4-bit digital-to-analog converter, a summing (error) amplifier, control logic, and a result latch circuit. The modified "flash" technique allows low-power integrated circuitry to complete an 8-bit conversion in 1.18 μs over temperature. The on-chip track-and-hold circuit has a 100 ns sample window and allows these devices to convert continuous analog signals having slew rates of up to 100 mV/μs without external sampling components. TTL-compatible three-state output drivers and two modes of operation allow interfacing to a variety of microprocessors. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The C-suffix devices are characterized for operation from 0°C to 70°C. See Available Options.

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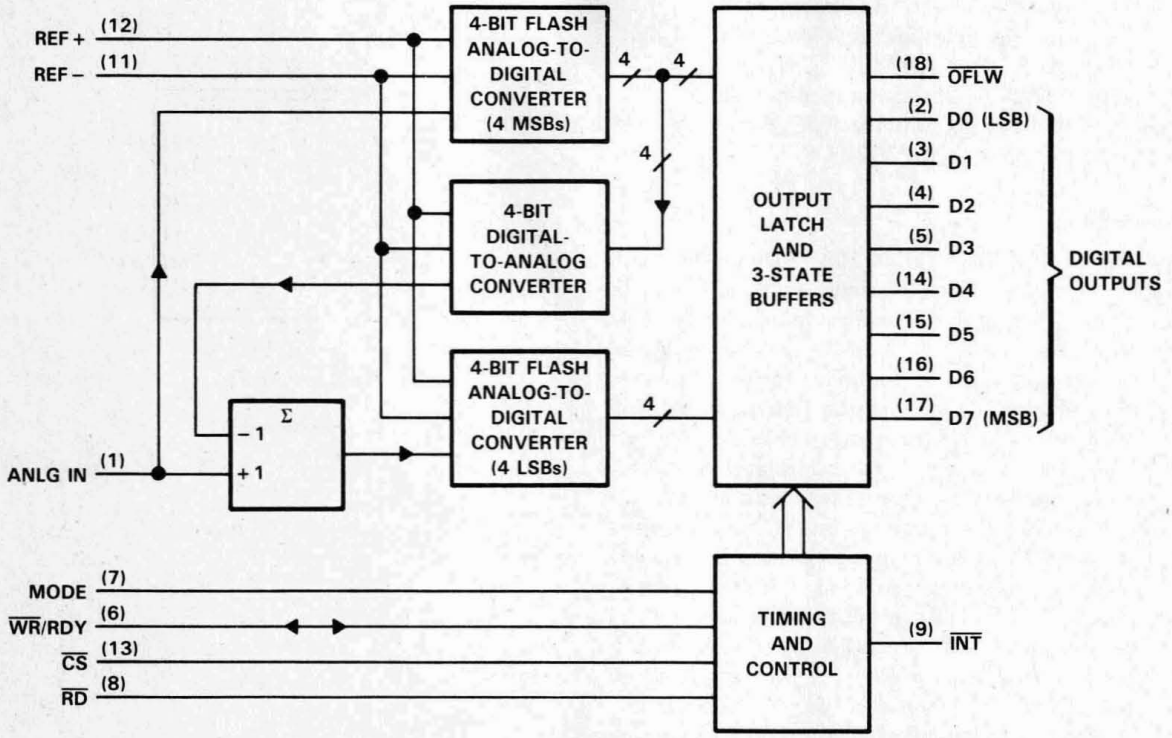
AVAILABLE OPTIONS

SYMBOLIZATION†		OPERATING TEMPERATURE RANGE	TOTAL UNADJUSTED ERROR
DEVICE	PACKAGE SUFFIX		
TLC0820AC	DW, FN, N	0°C to 70°C	±1 LSB
TLC0820AI	DW, FN, N	−40°C to 85°C	±1 LSB
TLC0820AM	DW, FK, J, N	−55°C to 125°C	±1 LSB
TLC0820BC	DW, FN, N	0°C to 70°C	±0.5 LSB
TLC0820BI	DW, FN, N	−40°C to 85°C	±0.5 LSB
TLC0820BM	DW, FK, J, N	−55°C to 125°C	±0.5 LSB
ADC0820BC	DW, FN, N	0°C to 70°C	±0.5 LSB
ADC0820BCI	DW, FN, N	−40°C to 85°C	±0.5 LSB
ADC0820CC	DW, FN, N	0°C to 70°C	±1 LSB
ADC0820CCI	DW, FN, N	−40°C to 85°C	±1 LSB

†In many instances, these ICs may have both TLC0820 and ADC0820 labeling on the package.

functional block diagram



PIN NAME	PIN NUMBER	DESCRIPTION
ANLG IN	1	Analog input
$\overline{CS}$	13	This input must be low in order for $\overline{RD}$ or $\overline{WR}$ to be recognized by the ADC.
D0	2	Three-state data output, bit 1 (LSB)
D1	3	Three-state data output, bit 2
D2	4	Three-state data output, bit 3
D3	5	Three-state data output, bit 4
D4	14	Three-state data output, bit 5
D5	15	Three-state data output, bit 6
D6	16	Three-state data output, bit 7
D7	17	Three-state data output, bit 8 (MSB)
GND	10	Ground
$\overline{INT}$	9	In the WRITE-READ mode, the interrupt output, $\overline{INT}$, going low indicates that the internal count-down delay time, $t_{d(int)}$, is complete and the data result is in the output latch. $t_{d(int)}$ is typically 800 ns starting after the rising edge of the $\overline{WR}$ input (see operating characteristics and Figure 3). If $\overline{RD}$ goes low prior to the end of $t_{d(int)}$, $\overline{INT}$ goes low at the end of t_{dRIL} and the conversion results are available sooner (see Figure 2). $\overline{INT}$ is reset by the rising edge of either $\overline{RD}$ or $\overline{CS}$.
MODE	7	Mode-selection input. It is internally tied to GND through a 50-μA current source, which acts like a pull-down resistor. READ mode: Occurs when this input is low. WRITE-READ mode: Occurs when this input is high.
NC	19	No internal connection
$\overline{OFLW}$	18	Normally the $\overline{OFLW}$ output is a logical high. However, if the analog input is higher than the V_{REF+}, $\overline{OFLW}$ will be low at the end of conversion. It can be used to cascade 2 or more devices to improve resolution (9 or 10-bits).
$\overline{RD}$	8	In the WRITE-READ mode with $\overline{CS}$ low, the 3-state data outputs D0 through D7 are activated when $\overline{RD}$ goes low. $\overline{RD}$ can also be used to increase the conversion speed by reading data prior to the end of the internal count-down delay time. As a result, the data transferred to the output latch is latched after the falling edge of $\overline{RD}$. In the READ mode with $\overline{CS}$ low, the conversion starts with $\overline{RD}$ going low. $\overline{RD}$ also enables the three-state data outputs upon completion of the conversion. The RDY output going into the high-impedance state and $\overline{INT}$ going low indicates completion of the conversion.
REF−	11	This input voltage is placed on the bottom of the resistor ladder.
REF+	12	This input voltage is placed on the top of the resistor ladder.
V_{CC}	20	Power supply voltage
$\overline{WR}$/RDY	6	In the WRITE-READ mode with $\overline{CS}$ low, the conversion is started on the falling edge of the $\overline{WR}$ input signal. The result of the conversion is strobed into the output latch after the internal count-down delay time, $t_{d(int)}$, provided that the $\overline{RD}$ input does not go low prior to this time. $t_{d(int)}$ is approximately 800 ns. In the READ mode, RDY (an open-drain output) will go low after the falling edge of $\overline{CS}$, and will go into the high-impedance state when the conversion is strobed into the output latch. It is used to simplify the interface to a microprocessor system.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	TLC0820_M	TLC0820_I ADC0820_CI	TLC0820_C ADC0820_C	UNIT
Supply voltage, V_{CC} (see Note 1)	10	10	10	V
Input voltage range, all inputs (see Note 1)	−0.2 to V_{CC}+0.2	−0.2 to V_{CC}+0.2	−0.2 to V_{CC}+0.2	V
Output voltage range, all outputs (see Note 1)	−0.2 to V_{CC}+0.2	−0.2 to V_{CC}+0.2	−0.2 to V_{CC}+0.2	V
Operating free-air temperature range	−55 to 125	−40 to 85	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds: FK package	260			°C
Case temperature for 10 seconds: FN package		260	260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300			°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package	260	260	260	°C

NOTE 1: All voltages are with respect to network ground terminal, pin 10.

recommended operating conditions

			TLC0820_M			TLC0820_I ADC0820_CI			TLC0820_C ADC0820_C			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.5	5	8	4.5	5	8	4.5	5	8	V
Analog input voltage			−0.1		V_{CC}+0.1	−0.1		V_{CC}+0.1	−0.1		V_{CC}+0.1	V
Positive reference voltage, V_{REF+}			V_{REF-}		V_{CC}	V_{REF-}		V_{CC}	V_{REF-}		V_{CC}	V
Negative reference voltage, V_{REF-}			GND		V_{REF+}	GND		V_{REF+}	GND		V_{REF+}	V
High-level input voltage, V_{IH}	V_{CC} = 4.75 V to 5.25 V	$\overline{CS}$, $\overline{WR}$/RDY, $\overline{RD}$	2			2			2			V
		MODE	3.5			3.5			3.5			
Low-level input voltage, V_{IL}	V_{CC} = 4.75 V to 5.25 V	$\overline{CS}$, $\overline{WR}$/RDY, $\overline{RD}$			0.8			0.8			0.8	V
		MODE			1.5			1.5			1.5	
Delay to next conversion, $t_{d(NC)}$ (see Figures 1, 2, 3, and 4)			500			500			500			ns
Delay time from $\overline{WR}$ to $\overline{RD}$ in write-read mode, t_{dWR} (see Figure 2)			0.4			0.4			0.4			μs
Write-pulse duration in write-read mode, t_{wW} (see Figures 2, 3, and 4)			0.5		50	0.5		50	0.5		50	μs
Operating free-air temperature, T_A			−55		125	−40		85	0		70	°C

electrical characteristics at specified operating free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	Any D, $\overline{INT}$, or $\overline{OFLW}$	V_{CC} = 4.75 V, I_{OH} = −360 μA	Full range	2.4			V
			V_{CC} = 4.75 V, I_{OH} = −10 μA	Full range	4.5			
				25°C	4.6			
V_{OL}	Low-level output voltage	Any D, $\overline{OFLW}$, $\overline{INT}$, or $\overline{WR}$/RDY	V_{CC} = 5.25 V, I_{OL} = 1.6 mA	Full range			0.4	V
				25°C			0.34	
I_{IH}	High-level input current	$\overline{CS}$ or $\overline{RD}$	V_{IH} = 5 V	Full range		0.005	1	μA
		$\overline{WR}$/RDY		Full range			3	
				25°C		0.1	0.3	
		MODE		Full range			200	
				25°C		50	170	
I_{IL}	Low-level input current	$\overline{CS}$, $\overline{WR}$/RDY, $\overline{RD}$, or MODE	V_{IL} = 0	Full range		−0.005	−1	μA
I_{OZ}	Off-state (high-impedance state) output current	Any D or $\overline{WR}$/RDY	V_O = 5 V	Full range			3	μA
				25°C		0.1	0.3	
			V_O = 0	Full range			−3	
				25°C		−0.1	−0.3	
I_I	Analog input current		$\overline{CS}$ at 5 V, V_I = 5 V	Full range			3	μA
				25°C			0.3	
			$\overline{CS}$ at 5 V, V_I = 0	Full range			−3	
				25°C			−0.3	
I_{OS}	Short-circuit output current	Any D, $\overline{OFLW}$, $\overline{INT}$, or $\overline{WR}$/RDY	V_O = 5 V	Full range	7			mA
				25°C	8.4	14		
		Any D or $\overline{OFLW}$	V_O = 0	Full range	−6			
				25°C	−7.2	−12		
		$\overline{INT}$		Full range	−4.5			
				25°C	−5.3	−9		
R_{ref}	Reference resistance			Full range	1.25		6	kΩ
				25°C	1.4	2.3	5.3	
I_{CC}	Supply current		$\overline{CS}$, $\overline{WR}$/RDY, and $\overline{RD}$ at 0 V	Full range			15	mA
				25°C		7.5	13	
C_i	Input capacitance	Any digital		Full range		5		pF
		ANLG IN				45		
C_o	Output capacitance	Any digital		Full range			5	pF

†All typical values are at T_A = 25°C.

operating characteristics, V_{CC} = 5 V, V_{REF+} = 5 V, V_{REF-} = 0, $t_r = t_f$ = 20 ns, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC0820B ADC0820B			TLC0820A ADC0820C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
k_{SVS}	Supply voltage sensitivity	V_{CC} = 5 V ± 5%, T_A = MIN to MAX			±1/16	±1/4		±1/16	±1/4	LSB
	Total unadjusted error†	MODE pin at 0 V, T_A = MIN to MAX				1/2			1	LSB
t_{convR}	Read mode conversion time	MODE pin at 0 V, See Figure 1			1.6	2.5		1.6	2.5	μs
$t_{d(int)}$	Internal count-down delay time	MODE pin at 5 V, See Figures 3 and 4	C_L = 50 pF,		800	1300		800	1300	ns
t_{aR}	Access time from $\overline{RD}$↓	MODE pin at 0 V, See Figure 1			t_{convR} +20	t_{convR} +50		t_{convR} +20	t_{convR} +50	ns
t_{aR1}	Access time from $\overline{RD}$↓	MODE pin at 5 V, $t_{dWR} < t_{d(int)}$, See Figure 2	C_L = 15 pF		190	280		190	280	ns
			C_L = 100 pF		210	320		210	320	
t_{aR2}	Access time from $\overline{RD}$↓	MODE pin at 5 V, $t_{dWR} > t_{d(int)}$ See Figure 3	C_L = 15 pF		70	120		70	120	ns
			C_L = 100 pF		90	150		90	150	
t_{aINT}	Access time from $\overline{INT}$↓	MODE pin at 5 V, See Figure 4			20	50		20	50	ns
t_{dis}	Disable time from $\overline{RD}$↑	R_L = 1 kΩ, See Figures 1, 2, 3, and 5	C_L = 10 pF,		70	95		70	95	ns
t_{dRDY}	Delay time from $\overline{CS}$↓ to RDY↓	MODE pin at 0 V, See Figure 1	C_L = 50 pF,		50	100		50	100	ns
t_{dRIH}	Delay time from $\overline{RD}$↑ to $\overline{INT}$↑	C_L = 50 pF, See Figures 1, 2, and 3			125	225		125	225	ns
t_{dRIL}	Delay time from $\overline{RD}$↓ to $\overline{INT}$↓	MODE pin at 5 V, See Figure 2	$t_{dWR} < t_{d(int)}$,		200	290		200	290	ns
t_{dWIH}	Delay time from $\overline{WR}$↑ to $\overline{INT}$↑	MODE pin at 5 V, See Figure 4	C_L = 50 pF,		175	270		175	270	ns
	Slew rate tracking				0.1			0.1		V/μs

† Total unadjusted error includes offset, full-scale, and linearity errors.

PARAMETER MEASUREMENT INFORMATION

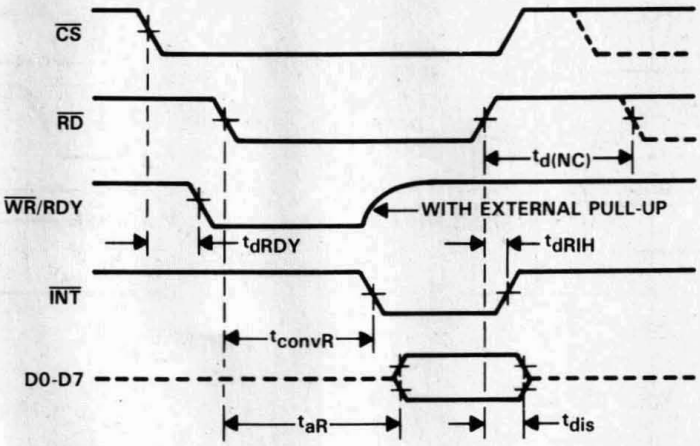


FIGURE 1. READ MODE WAVEFORMS (MODE PIN LOW)

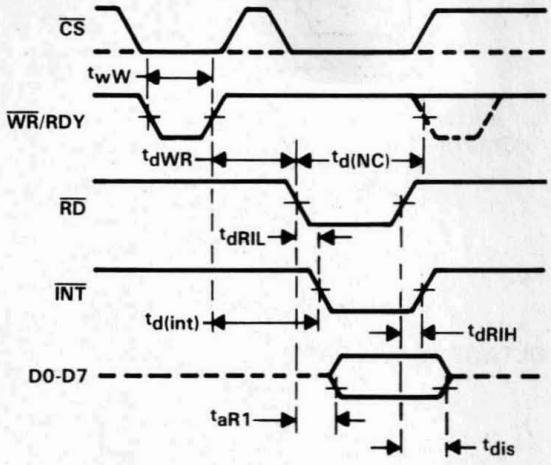


FIGURE 2. WRITE-READ MODE WAVEFORMS
[MODE PIN HIGH AND $t_{dWR} < t_{d(int)}$]

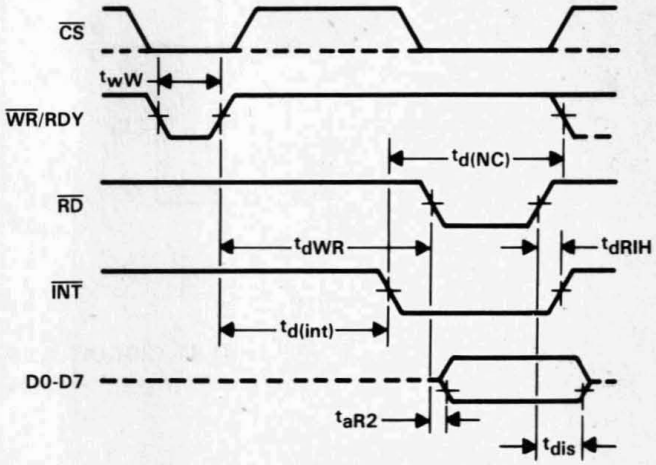


FIGURE 3. WRITE-READ WAVEFORMS
[MODE PIN HIGH AND $t_{dWR} > t_{d(int)}$]

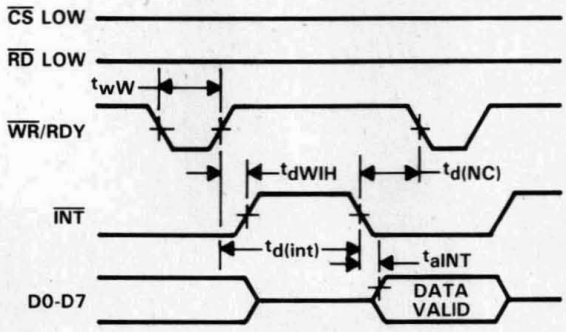
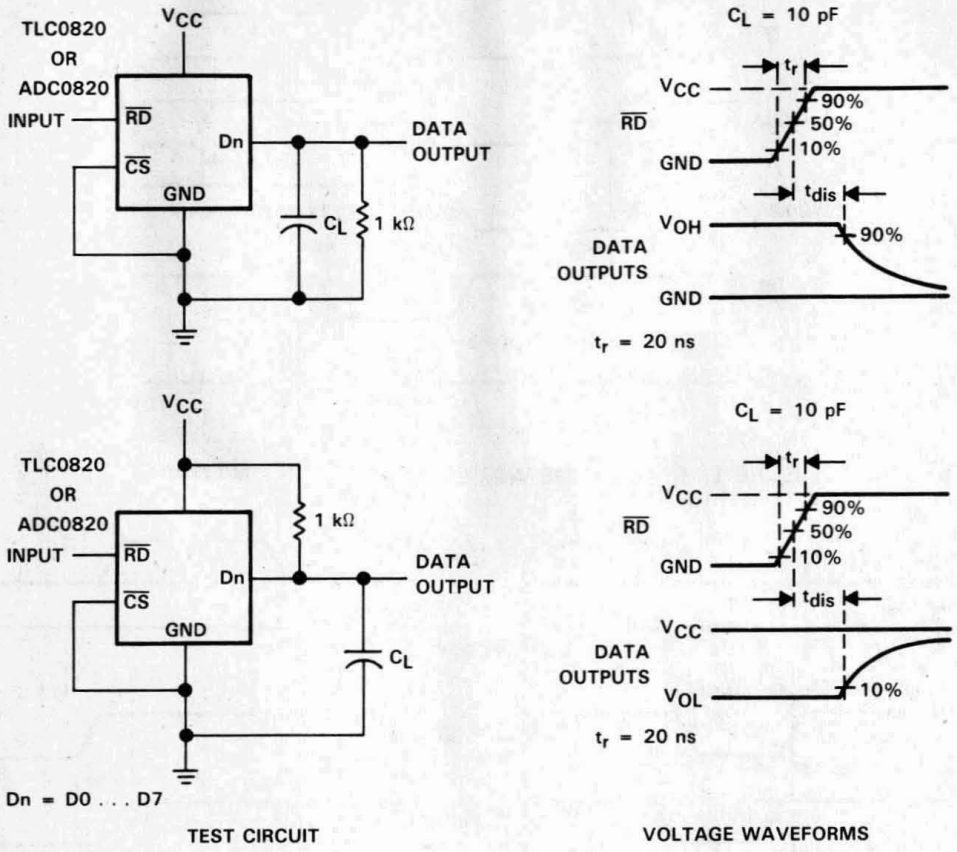


FIGURE 4. WRITE-READ MODE WAVEFORMS
(STAND-ALONE OPERATION, MODE PIN HIGH, AND RD LOW)

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 5. TEST CIRCUIT AND VOLTAGE WAVEFORMS

PRINCIPLES OF OPERATION

The TLC0820A, TLC0820B, ADC0820B and ADC0820C each employ a combination of "sampled-data" comparator techniques and "flash" techniques common to many high-speed converters. Two 4-bit "flash" analog-to-digital conversions are used to give a full 8-bit output.

The recommended analog input voltage range for conversion is -0.1 V to $V_{CC}+0.1$ V. Analog input signals that are less than V_{REF-} + ½ LSB or greater than V_{REF+} − ½ LSB convert to 00000000 or 11111111 respectively. The reference inputs are fully differential with common-mode limits defined by the supply rails. The reference input values define the full-scale range of the analog input. This allows the gain of the ADC to be varied for ratiometric conversion by changing the V_{REF+} and V_{REF-} voltages.

The device operates in two modes, read (only) and write-read, which are selected by the MODE pin (pin 7). The converter is set to the read (only) mode when pin 7 is low. In the read mode, the $\overline{WR}$/RDY pin is used as an output and is referred to as the "ready" pin. In this mode, a low on the "ready" pin while $\overline{CS}$ is low indicates that the device is busy. Conversion starts on the falling edge of $\overline{RD}$ and is completed no more than 2.5 μs later when $\overline{INT}$ falls and the "ready" pin returns to a high-impedance state. Data outputs also change from high-impedance to active states at this time. After the data is read, $\overline{RD}$ is taken high, $\overline{INT}$ returns high, and the data outputs return to their high-impedance states.

The converter is set to the write-read mode when pin 7 is high and $\overline{WR}$/RDY is referred to as the "write" pin. Taking $\overline{CS}$ and the "write" pin low selects the converter and initiates measurement of the input signal. Approximately 600 ns after the "write" pin returns high, the conversion is completed. Conversion starts on the rising edge of $\overline{WR}$/RDY in the write-read mode.

The high-order 4-bit "flash" ADC measures the input by means of 16 comparators operating simultaneously. A high precision 4-bit DAC then generates a discrete analog voltage from the result of that conversion. After a time delay, a second bank of comparators does a low-order conversion on the analog difference between the input level and the high-order DAC output. The results from each of these conversions enter an 8-bit latch and are output to the three-state buffers on the falling edge of $\overline{RD}$.

TYPICAL APPLICATION DATA

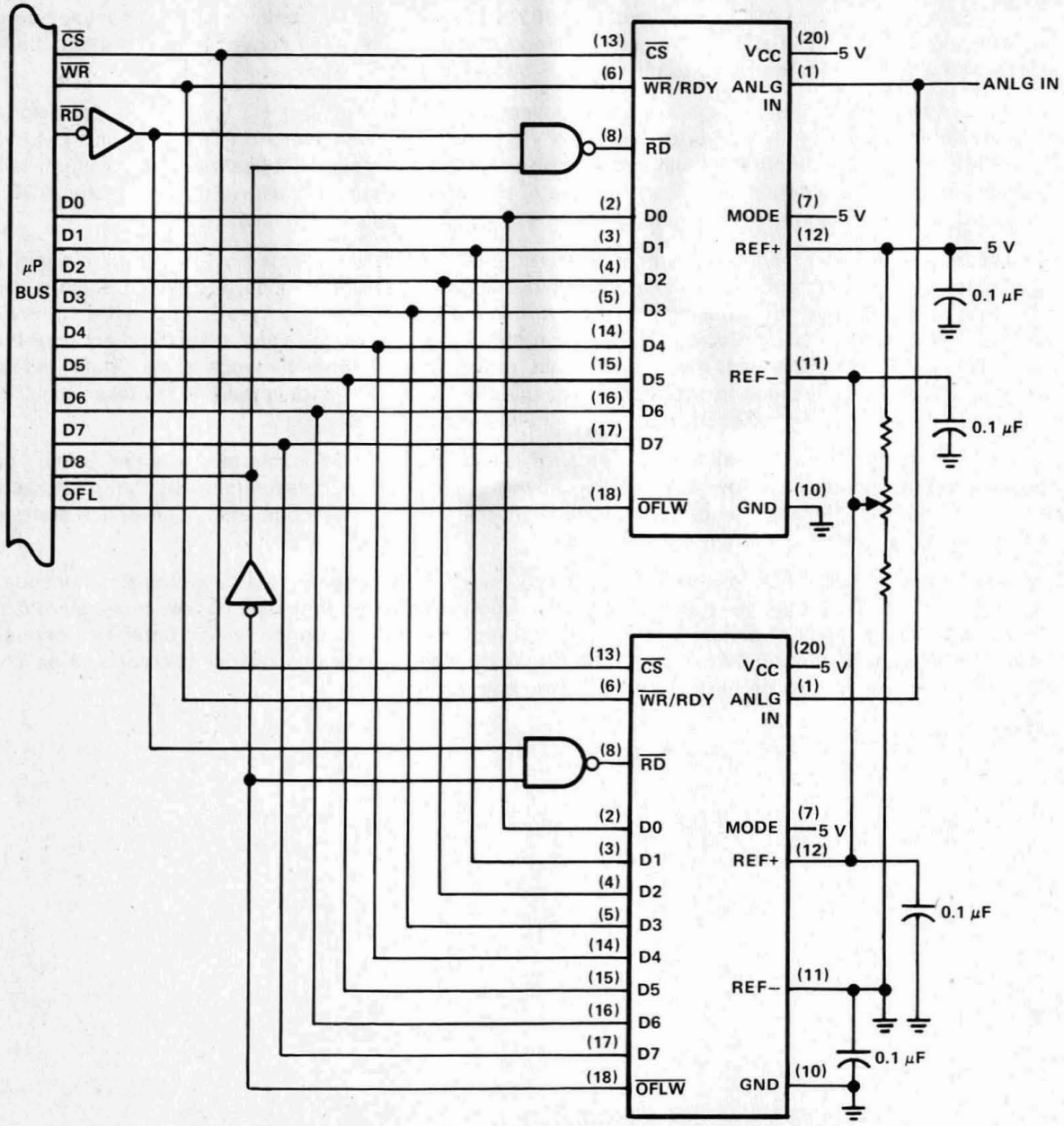


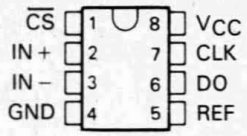
FIGURE 6. CONFIGURATION FOR 9-BIT RESOLUTION

D2795, AUGUST 1985—REVISED JUNE 1986

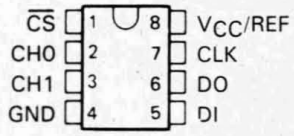
- **8-Bit Resolution**
- **Easy Microprocessor Interface or Stand-Alone Operation**
- **Operates Ratiometrically or with 5-V Reference**
- **Single Channel or Multiplexed Twin Channels with Single-Ended or Differential Input Options**
- **Input Range 0 to 5 V with Single 5-V Supply**
- **Inputs and Outputs are Compatible with TTL and MOS**
- **Conversion Time of 32 μs at CLK = 250 kHz**
- **Designed to be Interchangeable with National Semiconductor ADC0831 and ADC0832**

DEVICE	TOTAL UNADJUSTED ERROR	
	A-SUFFIX	B-SUFFIX
ADC0831	±1 LSB	± ½ LSB
ADC0832	±1 LSB	± ½ LSB

ADC0831 . . . P DUAL-IN-LINE PACKAGE
(TOP VIEW)



ADC0832 . . . P DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

These devices are 8-bit successive-approximation analog-to-digital converters. The ADC0831A and ADC0831B have single input channels; the ADC0832A and ADC0832B have multiplexed twin input channels. The serial output is configured to interface with standard shift registers or microprocessors. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The ADC0832 multiplexer is software configured for single-ended or differential inputs. The differential analog voltage input allows for common-mode rejection or offset of the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

The operation of the ADC0831 and ADC0832 devices is very similar to the more complex ADC0834 and ADC0838 devices. Ratiometric conversion can be attained by setting the REF input equal to the maximum analog input signal value, which gives the highest possible conversion resolution. Typically, REF is set equal to V_{CC} (done internally on the ADC0832). For more detail on the operation of the ADC0831 and ADC0832 devices, refer to the ADC0834/ADC0838 data sheet.

The ADC0831AI, ADC0831BI, ADC0832AI, and ADC0832BI are characterized for operation from −40°C to 85°C. The ADC0831AC, ADC0831BC, ADC0832AC, and ADC0832BC are characterized for operation from 0°C to 70°C.

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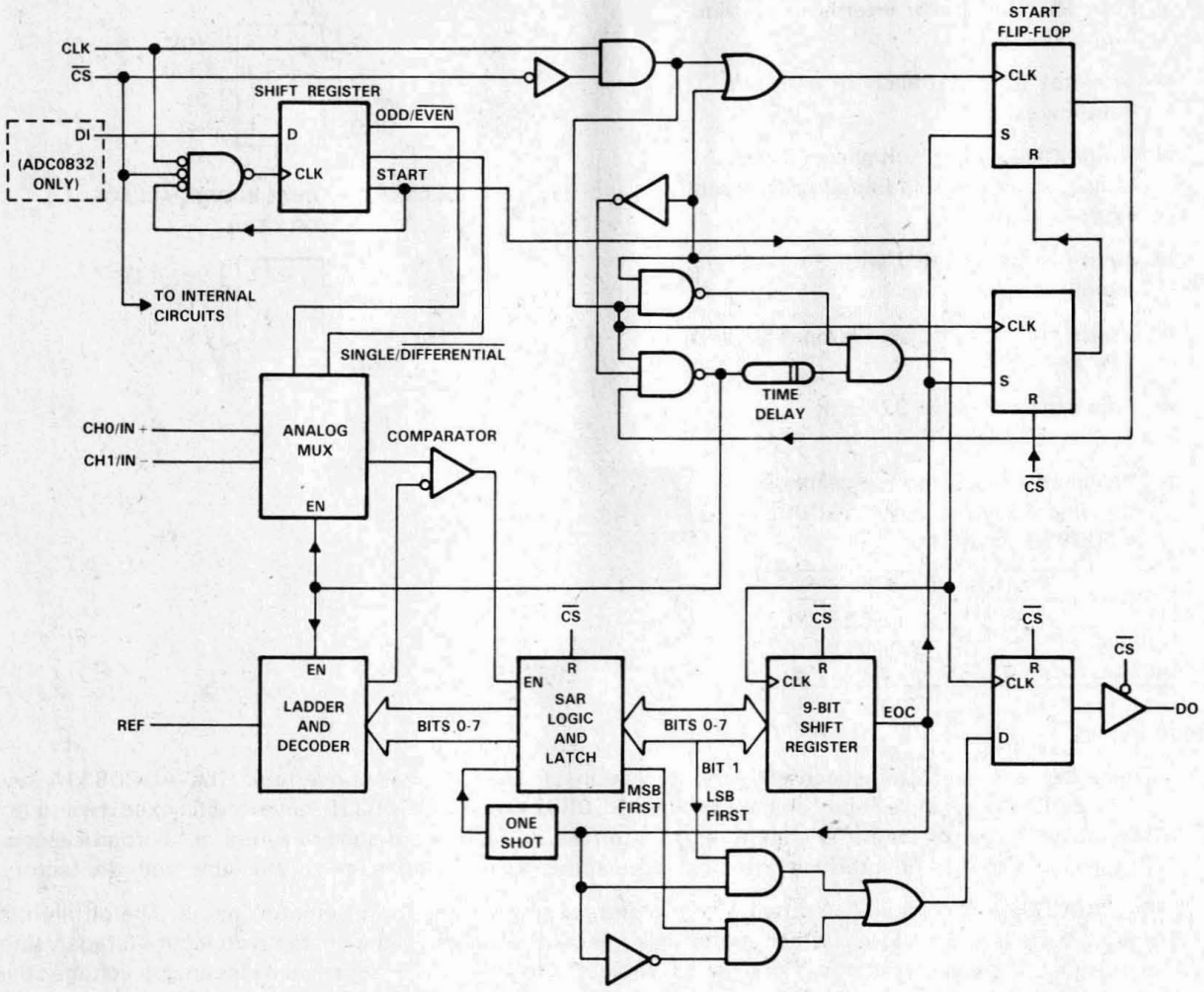
functional block diagram



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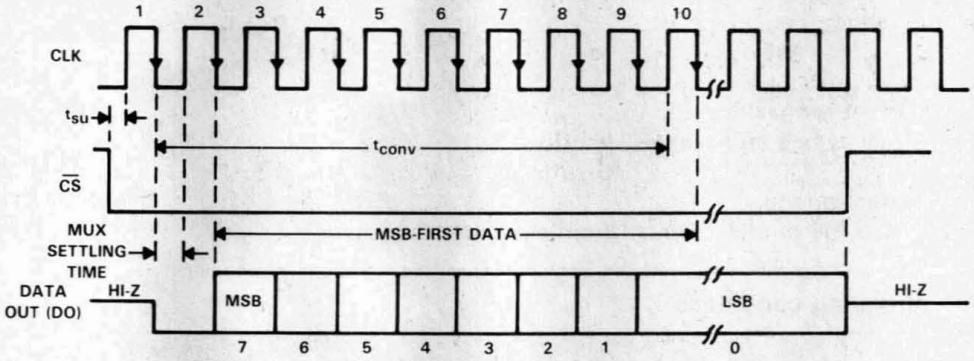
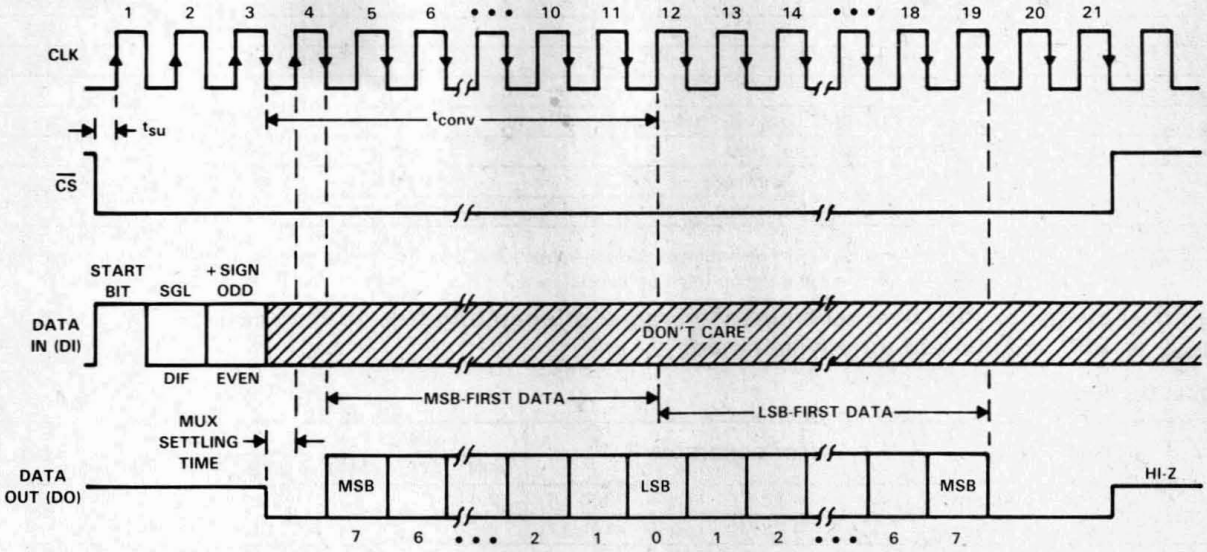
sequence of operation

ADC0831



ADC0832



ADC0832 MUX ADDRESS CONTROL LOGIC TABLE

MUX ADDRESS		CHANNEL NUMBER	
SGL/$\overline{DIF}$	ODD/$\overline{EVEN}$	0	1
L	L	+	−
L	H	−	+
H	L	+	
H	H		+

H = high level, L = low level, − or + = polarity of selected input pin

absolute maximum ratings over recommended operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range: Logic . . . . . −0.3 V to 15 V
Analog . . . . . −0.3 V to V_{CC} +0.3 V
Input current . . . . . ±5 mA
Total input current for package . . . . . ±20 mA
Operating free-air temperature range: I-suffix . . . . . −40°C to 85°C
C-suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values, except differential voltages, are with respect to the network ground terminal.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	6.3	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
f_{clock}	Clock frequency		10		400	kHz
	Clock duty cycle (see Note 2)		40		60	%
$t_{wH(CS)}$	Pulse duration, $\overline{CS}$ high		220			ns
t_{su}	Setup time, $\overline{CS}$ low or ADC0832 data valid before clock↑		350			ns
t_h	Hold time, ADC0832 data valid after clock↑		90			ns
T_A	Operating free-air temperature	I-suffix	−40		85	°C
		C-suffix	0		70	

NOTE 2: The clock duty cycle range ensures proper operation at all clock frequencies. If a clock frequency is used outside the recommended duty cycle range, the minimum pulse duration (high or low) is 1 μs.

electrical characteristics over recommended range of operating free-air temperature, V_{CC} = 5 V, f_{clock} = 250 kHz (unless otherwise noted)

digital section

PARAMETER		TEST CONDITIONS†		I SUFFIX			C SUFFIX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{OH}	High-level output voltage	V_{CC} = 4.75 V,	I_{OH} = −360 μA	2.4			2.8			V
		V_{CC} = 4.75 V,	I_{OH} = −10 μA	4.5			4.6			
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V,	I_{OL} = 1.6 mA	0.4			0.34			V
I_{IH}	High-level input current	V_{IH} = 5 V			0.005	1		0.005	1	μA
I_{IL}	Low-level input current	V_{IL} = 0			−0.005	−1		−0.005	−1	μA
I_{OH}	High-level output (source) current	V_{OH} = V_O,	T_A = 25°C	−6.5	−14		−6.5	−14		mA
I_{OL}	Low-level output (sink) current	V_{OL} = V_{CC},	T_A = 25°C	8	16		8	16		mA
I_{OZ}	High-impedance-state output current (DO)	V_O = 5 V,	T_A = 25°C		0.01	3		0.01	3	μA
		V_O = 0,	T_A = 25°C		−0.01	−3		−0.01	−3	
C_i	Input capacitance				5			5		pF
C_o	Output capacitance				5			5		pF

† All parameters are measured under open-loop conditions with zero common-mode input voltage.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics over recommended range of operating free-air temperature, V_{CC} = 5 V, f_{clock} = 250 kHz (unless otherwise noted)

analog and converter section

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{ICR}	Common-mode input voltage range		See Note 3	−0.05 to V_{CC}+0.05			V
$I_{I(stdby)}$	Standby input current (see Note 4)	On-channel	V_I = 5 V at on-channel,			1	μA
		Off-channel	V_I = 0 at off-channel			−1	
		On-channel	V_I = 0 at on-channel,			−1	
		Off-channel	V_I = 5 V at off-channel			1	
$r_{i(REF)}$	Input resistance to reference ladder			1.3	2.4	5.9	kΩ

total device

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
I_{CC}	Supply current	ADC0831			1	2.5	mA
		ADC0832			3	5.2	

†All parameters are measured under open-loop conditions with zero common-mode input voltage.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 3. If channel IN− is more positive than channel IN+, the digital output code will be 0000 0000. Connected to each analog input are two on-chip diodes that will conduct forward current for analog input voltages one diode drop above V_{CC}. Care must be taken during testing at low V_{CC} levels (4.5 V) because high-level analog input voltage (5 V) can, especially at high temperatures, cause this input diode to conduct and cause errors for analog inputs that are near full-scale. As long as the analog voltage does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V to 5 V input voltage range requires a minimum V_{CC} of 4.95 V for all variations of temperature and load.

4. Standby input currents are currents going into or out of the on or off channels when the A/D converter is not performing conversion and the clock is in a high or low steady-state condition.

operating characteristics V_{CC} = REF = 5 V, f_{clock} = 250 kHz, t_r = t_f = 20 ns, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS§	BI, BC SUFFIX			AI, AC SUFFIX			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
	Supply-voltage variation error		V_{CC} = 4.75 V to 5.25 V		±1/16	±1/4		±1/16	±1/4	LSB
	Total unadjusted error (see Note 5)		V_{ref} = 5 V, T_A = MIN to MAX			±1/2			±1	LSB
	Common-mode error		Differential mode		±1/16	±1/4		±1/16	±1/4	LSB
t_{pd}	Propagation delay time, output data after CLK↓ (see Note 6)	MSB-first data	C_L = 100 pF		650	1500		650	1500	ns
		LSB-first data			250	600		250	600	
t_{dis}	Output disable time, DO after $\overline{CS}$↑		C_L = 10 pF, R_L = 10 kΩ		125	250		125	250	ns
			C_L = 100 pF, R_L = 2 kΩ			500			500	
t_{conv}	Conversion time (multiplexer addressing time not included)					8			8	clock periods

§ All parameters are measured under open-loop conditions with zero common-mode input voltage. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 5. Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors.

6. The most significant-bit-first data is output directly from the comparator and therefore requires additional delay to allow for comparator response time. Least-significant-bit-first data applies only to ADC0832.

PARAMETER MEASUREMENT INFORMATION

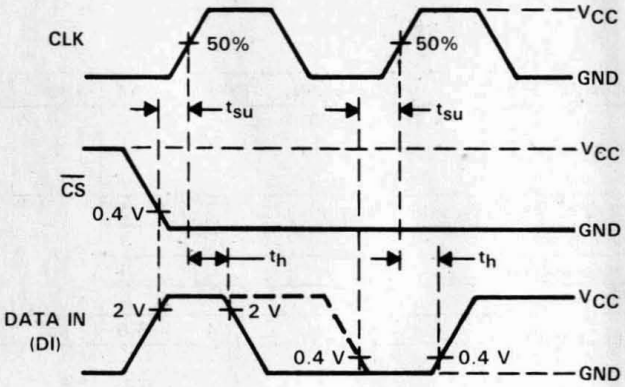


FIGURE 1. ADC0832 DATA INPUT TIMING

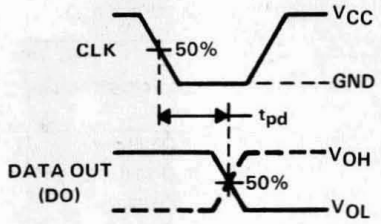
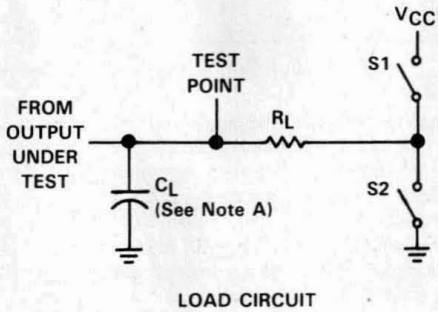
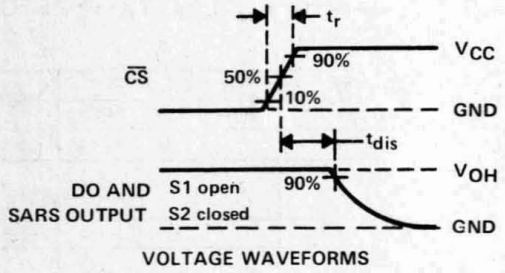


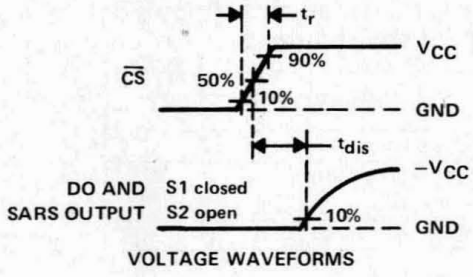
FIGURE 2. DATA OUTPUT TIMING



LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

FIGURE 3. OUTPUT DISABLE TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS

UNADJUSTED OFFSET ERROR
vs
REFERENCE VOLTAGE

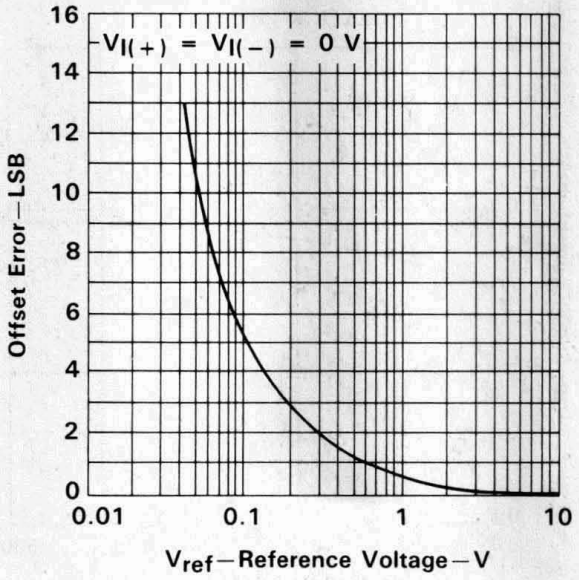


FIGURE 4

LINEARITY ERROR
vs
REFERENCE VOLTAGE

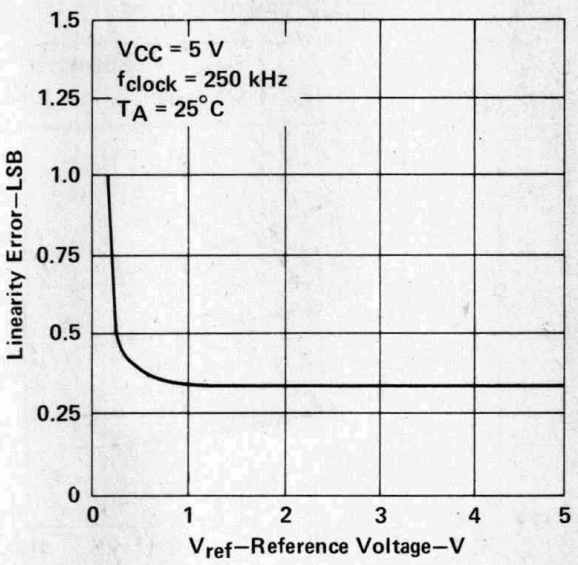


FIGURE 5

LINEARITY ERROR
vs
FREE-AIR TEMPERATURE

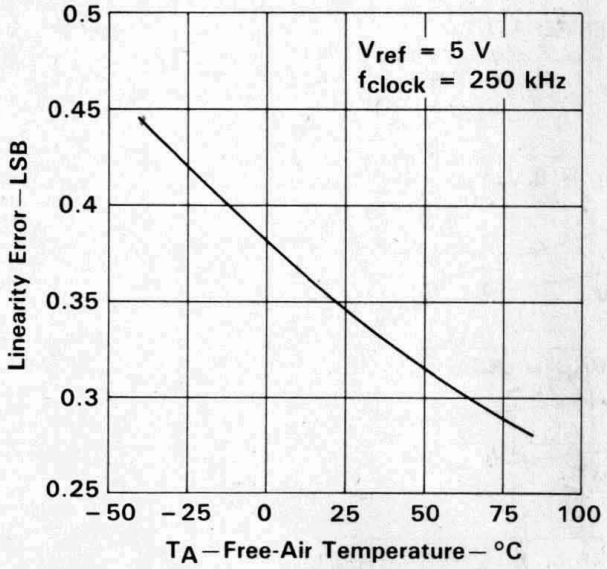


FIGURE 6

LINEARITY ERROR
vs
CLOCK FREQUENCY

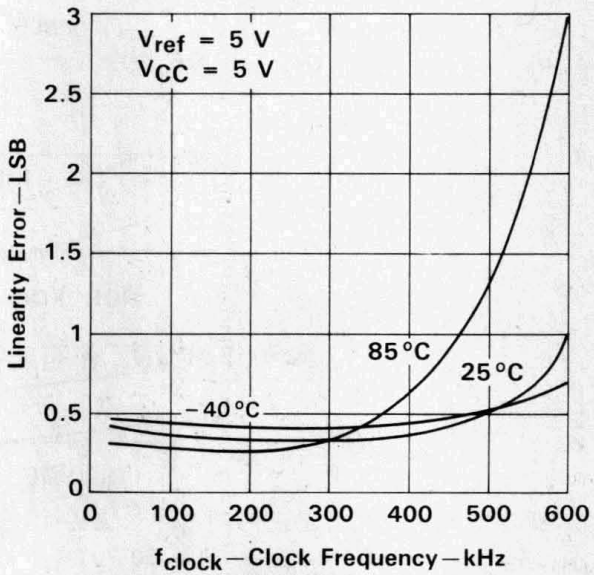


FIGURE 7

TYPICAL CHARACTERISTICS

ADC0831
SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

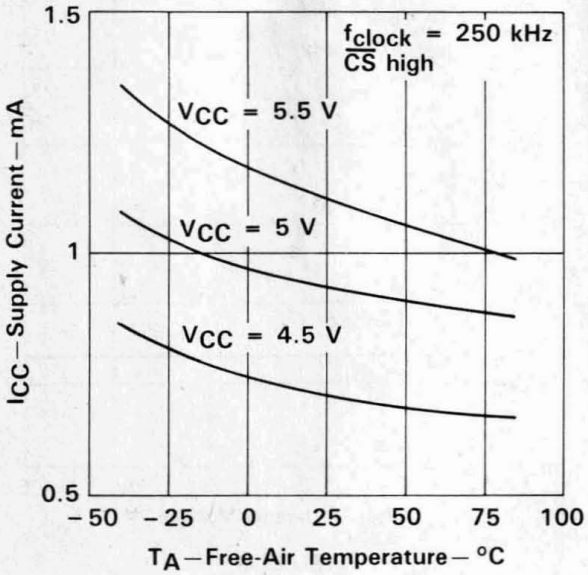


FIGURE 8

ADC0831
SUPPLY CURRENT
vs
CLOCK FREQUENCY

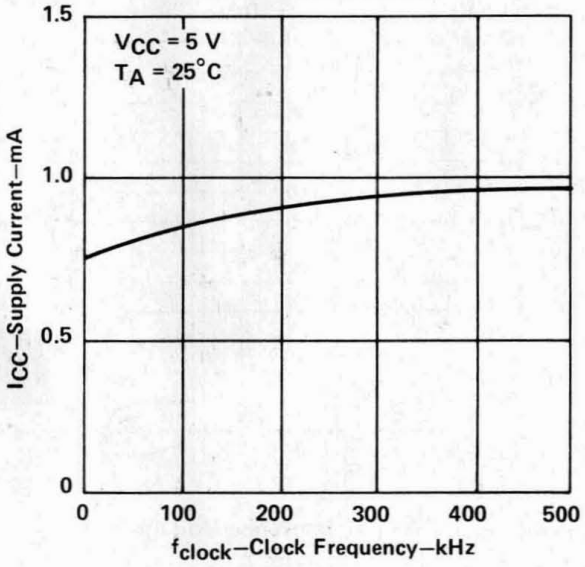


FIGURE 9

OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

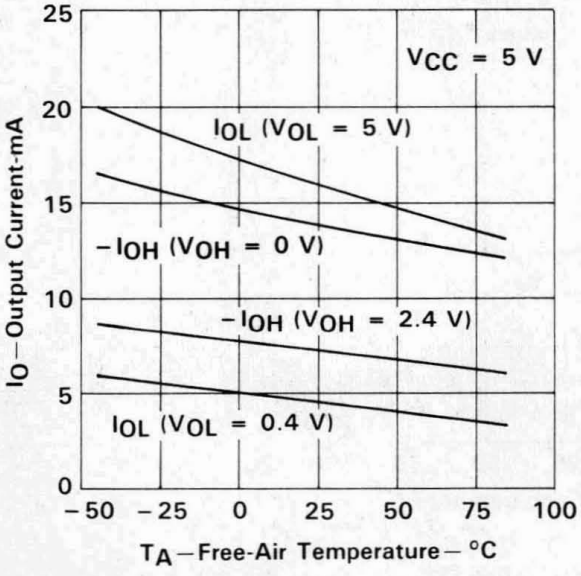


FIGURE 10

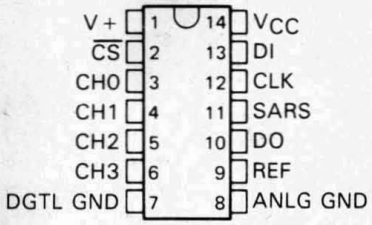
ADC0834A, ADC0838A, ADC0834B, ADC0838B
A/D PERIPHERALS WITH SERIAL CONTROL

D2795, AUGUST 1985—REVISED OCTOBER 1986

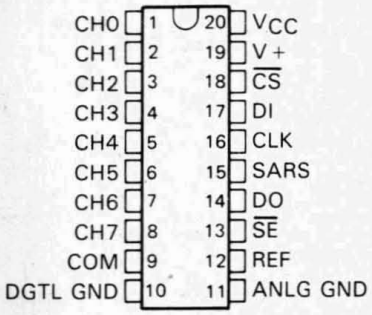
- **8-Bit Resolution**
- **Easy Microprocessor Interface or Stand-Alone Operation**
- **Operates Ratiometrically or with 5-V Reference**
- **4- or 8-Channel Multiplexer Options with Address Logic**
- **Shunt Regulator Allows Operation with High-Voltage Supplies**
- **Input Range 0 to 5 V with Single 5-V Supply**
- **Remote Operation with Serial Data Link**
- **Inputs and Outputs are Compatible with TTL and MOS**
- **Conversion Time of 32 μs at f_{clock} = 250 kHz**
- **Designed to be Interchangeable with National Semiconductor ADC0834 and ADC0838**

DEVICE	TOTAL UNADJUSTED ERROR	
	A SUFFIX	B SUFFIX
ADC0834	±1 LSB	±1/2 LSB
ADC0838	±1 LSB	±1/2 LSB

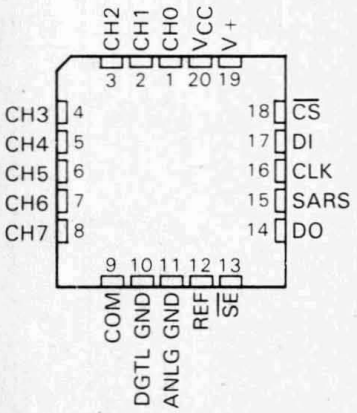
ADC0834 . . . N PACKAGE
(TOP VIEW)



ADC0838 . . . N PACKAGE
(TOP VIEW)



ADC0838 . . . FN PACKAGE
(TOP VIEW)



description

These devices are 8-bit successive-approximation analog-to-digital converters, each with an input-configurable multichannel multiplexer and serial input/output. The serial input/output is configured to interface with standard shift registers or microprocessors. Detailed information on interfacing with most popular microprocessors is readily available from the factory.

The ADC0834 (4-channel) and ADC0838 (8-channel) multiplexer is software configured for single-ended or differential inputs as well as pseudo-differential input assignments. The differential analog voltage input allows for common-mode rejection or offset of the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

The ADC0834AI, ADC0834BI, ADC0838AI, and ADC0838BI are characterized for operation from −40°C to 85°C. The ADC0834AC, ADC0834BC, ADC0838AC, and ADC0838BC are characterized for operation from 0°C to 70°C.

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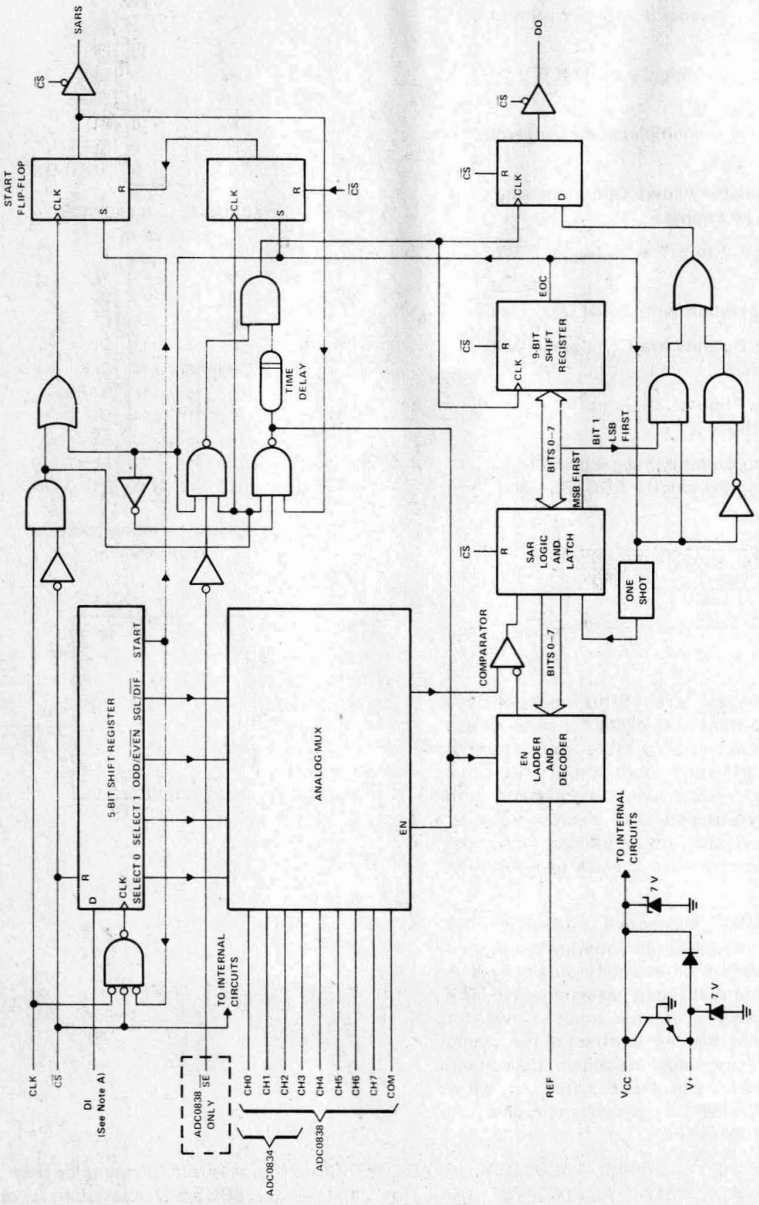
functional block diagram



NOTE A: For the ADC0834, DI is input directly to the D input of SELECT 1; SELECT 0 is forced to a high.

functional description

The ADC0834 and ADC0838 use a sample data comparator structure that converts differential analog inputs by a successive-approximation routine. Operation of both devices is similar with the exception of a select enable ($\overline{SE}$) input, an analog common input, and multiplexer addressing. The input voltage to be converted is applied to a channel terminal and is compared to ground (single-ended), to an adjacent input (differential), or to a common terminal (pseudo-differential) that can be an arbitrary voltage. The input terminals are assigned a positive (+) or negative (−) polarity. If the signal input applied to the assigned positive terminal is less than the signal on the negative terminal, the converter output is all zeros.

Channel selection and input configuration are under software control using a serial data link from the controlling processor. A serial communication format allows more functions to be included in a converter package with no increase in size. In addition, it eliminates the transmission of low-level analog signals by locating the converter at the analog sensor and communicating serially with the controlling processor. This process returns noise-free digital data to the processor.

A particular input configuration is assigned during the multiplexer addressing sequence. The multiplexer address is shifted into the converter through the data input (DI) line. The multiplexer address selects the analog inputs to be enabled and determines whether the input is single-ended or differential. When the input is differential, the polarity of the channel input is assigned. Differential inputs are assigned to adjacent channel pairs. For example, channel 0 and channel 1 may be selected as a differential pair. These channels cannot act differentially with any other channel. In addition to selecting the differential mode, the polarity may also be selected. Either channel of the channel pair may be designated as the negative or positive input.

The common input on the ADC0838 can be used for a pseudo-differential input. In this mode, the voltage on the common input is considered to be the negative differential input for all channel inputs. This voltage can be any reference potential common to all channel inputs. Each channel input can then be selected as the positive differential input. This feature is useful when all analog circuits are biased to a potential other than ground.

A conversion is initiated by setting the chip select ($\overline{CS}$) input low, which enables all logic circuits. The $\overline{CS}$ input must be held low for the complete conversion process. A clock input is then received from the processor. On each low-to-high transition of the clock input, the data on the DI input is clocked into the multiplexer address shift register. The first logic high on the input is the start bit. A 3- to 4-bit assignment word follows the start bit. On each successive low-to-high transition of the clock input, the start bit and assignment word are shifted through the shift register. When the start bit is shifted into the start location of the multiplexer register, the input channel is selected and conversion starts. The SAR Status output (SARS) goes high to indicate that a conversion is in progress, and the DI input to the multiplexer shift register is disabled the duration of the conversion.

An interval of one clock period is automatically inserted to allow the selected multiplexed channel to settle. The data output DO comes out of the high-impedance state and provides a leading low for this one clock period of multiplexer settling time. The SAR comparator compares successive outputs from the resistive ladder with the incoming analog signal. The comparator output indicates whether the analog input is greater than or less than the resistive ladder output. As the conversion proceeds, conversion data is simultaneously output from the DO output pin, with the most significant bit (MSB) first.

After eight clock periods the conversion is complete and the SAR Status (SARS) output goes low.

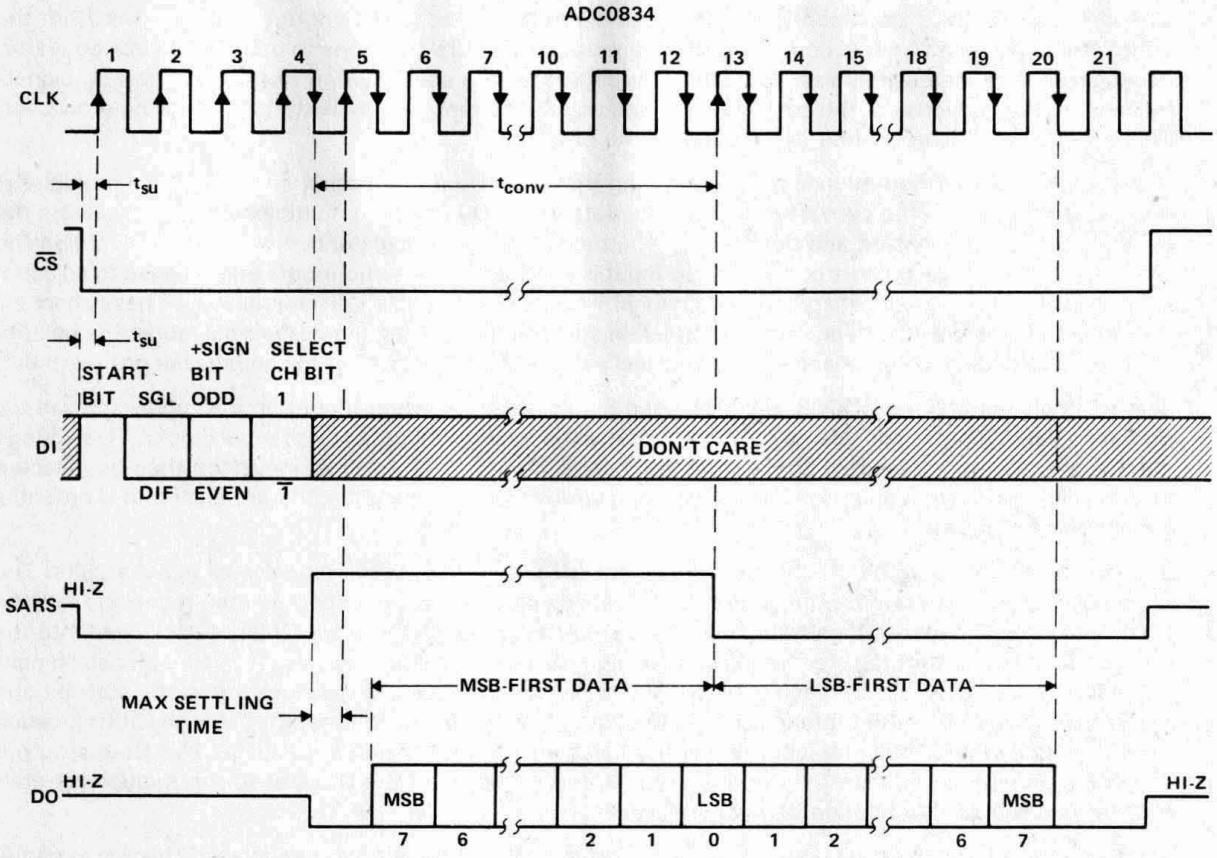
The ADC0834 outputs the least-significant-bit-first data after the MSB-first data stream. If the shift enable ($\overline{SE}$) line is held high on the ADC0838, the value of the least significant bit (LSB) will remain on the data line. When $\overline{SE}$ is forced low, the data is then clocked out as LSB-first data. (To output LSB first, the $\overline{SE}$ control input must first go low, then the data stored in the 9-bit shift register outputs LSB first.) When $\overline{CS}$ goes high, all internal registers are cleared. At this time the output circuits go to the high-impedance state. If another conversion is desired, the $\overline{CS}$ line must make a high-to-low transition followed by address information.

functional description (continued)

The DI and DO pins can be tied together and controlled by a bidirectional processor I/O bit received on a single wire. This is possible because the DI input is only examined during the multiplexer addressing interval and the DO output is still in a high-impedance state.

Detailed information on interfacing to most popular microprocessors is readily available from the factory.

sequence of operation

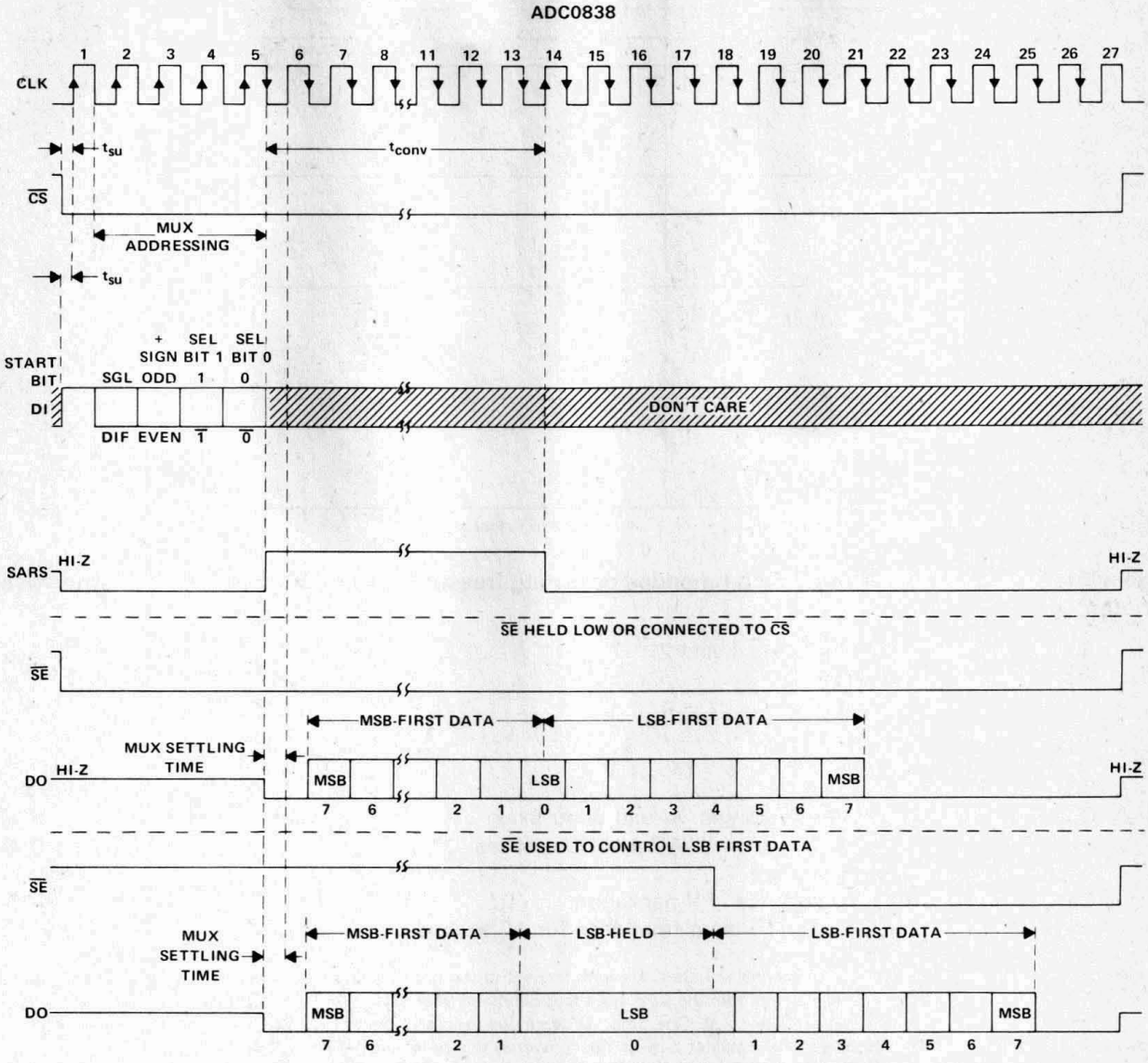


ADC0834 MUX ADDRESS CONTROL LOGIC TABLE

MUX ADDRESS			CHANNEL NUMBER			
SGL/$\overline{DIF}$	ODD/$\overline{EVEN}$	SELECT BIT 1	0	1	2	3
L	L	L	+	−		
L	L	H			+	−
L	H	L	−	+		
L	H	H			−	+
H	L	L	+			
H	L	H			+	
H	H	L		+		
H	H	H				+

H = high level, L = low level, − or + = polarity of selected input pin

sequence of operation



ADC0838 MUX ADDRESS CONTROL LOGIC TABLE

MUX ADDRESS				SELECTED CHANNEL NUMBER								COM
SGL/$\overline{\text{DIF}}$	ODD/$\overline{\text{EVEN}}$	SELECT		0		1		2		3		
		1	0	0	1	2	3	4	5	6	7	
L	L	L	L	+	−							
L	L	L	H			+	−					
L	L	H	L					+	−			
L	L	H	H							+	−	
L	H	L	L	−	+							
L	H	L	H			−	+					
L	H	H	L					+	−			
L	H	H	H							−	+	
H	L	L	L	+								−
H	L	L	H			+						−
H	L	H	L					+				−
H	L	H	H							+		−
H	H	L	L		+							−
H	H	L	H				+					−
H	H	H	L						+			−
H	H	H	H								+	−

H = high level, L = low level, − or + = polarity of selected input

absolute maximum ratings over recommended operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Notes 1 and 2) . . . . . 6.5 V
Input voltage range: Logic . . . . . −0.3 V to 15 V
Analog . . . . . −0.3 V to V_{CC} +0.3 V
Input current: V+ input . . . . . 15 mA
Any other input . . . . . ±5 mA
Total input current for package . . . . . ±20 mA
Operating free-air temperature range: AI and BI suffixes . . . . . −40°C to 85°C
AC and BC suffixes . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Internal zener diodes are connected from the V_{CC} input to ground and from the V+ input to ground. The breakdown voltage of each zener diode is approximately 7 V. One zener diode can be used as a shunt regulator and connects to V_{CC} through a regular diode. When the voltage regulator powers the converter, this zener and regular diode combination ensures that the V_{CC} input (6.4 V) is less than the zener breakdown voltage. A series resistor is recommended to limit current into the V+ input.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	6.3	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
f_{clock}	Clock frequency		10		400	kHz
	Clock duty cycle (see Note 3)		40		60	%
$t_{wH(CS)}$	Pulse duration, $\overline{CS}$ high		220			ns
t_{su}	Setup time, $\overline{CS}$ low, $\overline{SE}$ low, or data valid before clock↑		350			ns
t_h	Hold time, data valid after clock↑		90			ns
T_A	Operating free-air temperature	AI and BI suffixes	−40		85	°C
		AC and BC suffixes	0		70	

NOTE 3: The clock duty cycle range ensures proper operation at all clock frequencies. If a clock frequency is used outside the recommended duty cycle range, the minimum pulse duration (high or low) is 1 μs.

electrical characteristics over recommended range of operating free-air temperature, V_{CC} = V+ = 5 V, f_{clock} = 250 kHz (unless otherwise noted)

digital section

PARAMETER		TEST CONDITIONS†		AI, BI SUFFIX			AC, BC SUFFIX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{OH}	High-level output voltage	V_{CC} = 4.75 V,	I_{OH} = −360 μA	2.4			2.8			V
		V_{CC} = 4.75 V,	I_{OH} = −10 μA	4.5			4.6			
V_{OL}	Low-level output voltage	V_{CC} = 5.25 V,	I_{OL} = 1.6 mA			0.4			0.34	V
I_{IH}	High-level input current	V_{IH} = 5 V			0.005	1		0.005	1	μA
I_{IL}	Low-level input current	V_{IL} = 0			−0.005	−1		−0.005	−1	μA
I_{OH}	High-level output (source) current	V_{OH} = 0,	T_A = 25°C	−6.5	−14		−6.5	−14		mA
I_{OL}	Low-level output (sink) current	V_{OL} = V_{CC},	T_A = 25°C	8	16		8	16		mA
I_{OZ}	High-impedance-state output current (DO or SARS)	V_O = 5 V,	T_A = 25°C		0.01	3		0.01	3	μA
		V_O = 0,	T_A = 25°C		−0.01	−3		−0.01	−3	
C_i	Input capacitance				5			5		pF
C_o	Output capacitance				5			5		pF

†All parameters are measured under open-loop conditions with zero common-mode input voltage (unless otherwise specified).
‡All typical values are at V_{CC} = V+ = 5 V, T_A = 25°C.

electrical characteristics over recommended range of operating free-air temperature, V_{CC} = V+ = 5 V, f_{clock} = 250 kHz (unless otherwise noted)

analog and converter section

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{ICR}	Common-mode input voltage range		See Note 4	−0.05 to V_{CC}+0.05			V
$I_{I(stdby)}$	Standby input current (see Note 5)	On-channel	V_I = 5 V at on-channel, V_I = 0 at off-channel			1	μA
		Off-channel				−1	
		On-channel	V_I = 0 at on-channel, V_I = 5 V at off-channel			−1	
		Off-channel				1	
$r_{i(ref)}$	Input resistance to reference ladder			1.3	2.4	5.9	kΩ

total device

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_Z	Internal zener diode breakdown voltage	I_I = 15 mA at V+ pin, See Note 2	6.3	7	8.5	V
I_{CC}	Supply current			1	2.5	mA

†All parameters are measured under open-loop conditions with zero common-mode input voltage.

‡All typical values are at V_{CC} = 5 V, V+ = 5 V, T_A = 25°C.

NOTES: 2. Internal zener diodes are connected from the V_{CC} input to ground and from the V+ input to ground. The breakdown voltage of each zener diode is approximately 7 V. One zener diode can be used as a shunt regulator and connects to V_{CC} through a regular diode. When the voltage regulator powers the converter, this zener and regular diode combination ensures that the V_{CC} input (6.4 V) is less than the zener breakdown voltage. A series resistor is recommended to limit current into the V+ input.

4. If channel IN− is more positive than channel IN+, the digital output code will be 0000 0000. Connected to each analog input are two on-chip diodes that conduct forward current for analog input voltages one diode drop above V_{CC}. Care must be taken during testing at low V_{CC} levels (4.5 V) because high-level analog input voltage (5 V) can, especially at high temperatures, cause this input diode to conduct and cause errors for analog inputs that are near full-scale. As long as the analog voltage does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V to 5 V input voltage range requires a minimum V_{CC} of 4.950 V for all variations of temperature and load.

5. Standby input currents are currents going into or out of the on or off channels when the A/D converter is not performing conversion and the clock is in a high or low steady-state condition.

operating characteristics V+ = V_{CC} = 5 V, f_{clock} = 250 kHz, t_r = t_f = 20 ns, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	BI, BC SUFFIX			AI, AC SUFFIX			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
	Supply-voltage variation error		V_{CC} = 4.75 V to 5.25 V		±1/16	±1/4		±1/16	±1/4	LSB
	Total unadjusted error (see Note 6)		V_{ref} = 5 V, T_A = MIN to MAX			±1/2			±1	LSB
	Common-mode error		Differential mode		±1/16	±1/4		±1/16	±1/4	LSB
	Change in zero-error from V_{CC} = 5 V to internal zener diode operation (see Note 2)		I_I = 15 mA at V+ pin, V_{ref} = 5 V, V_{CC} open			1			1	LSB
t_{pd}	Propagation delay time, output data after CLK↓ (see Note 7)	MSB-first data	C_L = 100 pF		650	1500		650	1500	ns
		LSB-first data			250	600		250	600	
t_{dis}	Output disable time, DO or SARS after CS↑		C_L = 10 pF, R_L = 10 kΩ		125	250		125	250	ns
			C_L = 100 pF, R_L = 2 kΩ			500			500	
t_{conv}	Conversion time (multiplexer addressing time not included)					8			8	clock periods

†All parameters are measured under open-loop conditions with zero common-mode input voltage. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 2. Internal zener diodes are connected from the V_{CC} input to ground and from the V+ input to ground. The breakdown voltage of each zener diode is approximately 7 V. One zener diode can be used as a shunt regulator and connects to V_{CC} through a regular diode. When the voltage regulator powers the converter, this zener and regular diode combination ensures that the V_{CC} input (6.4 V) is less than the zener breakdown voltage. A series resistor is recommended to limit current into the V+ input.

6. Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors.
7. The most significant bit (MSB) data is output directly from the comparator and therefore requires additional delay to allow for comparator response time.

PARAMETER MEASUREMENT INFORMATION

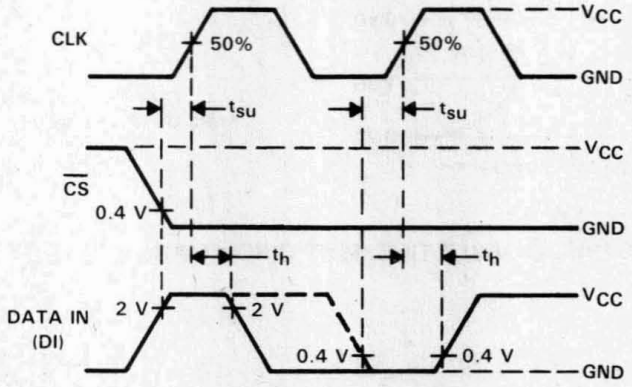


FIGURE 1. DATA INPUT TIMING

PARAMETER MEASUREMENT INFORMATION

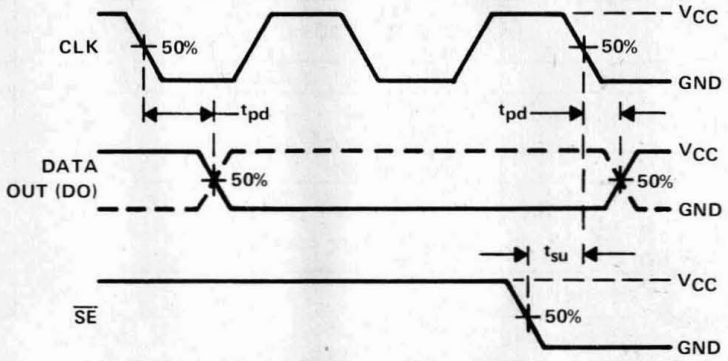
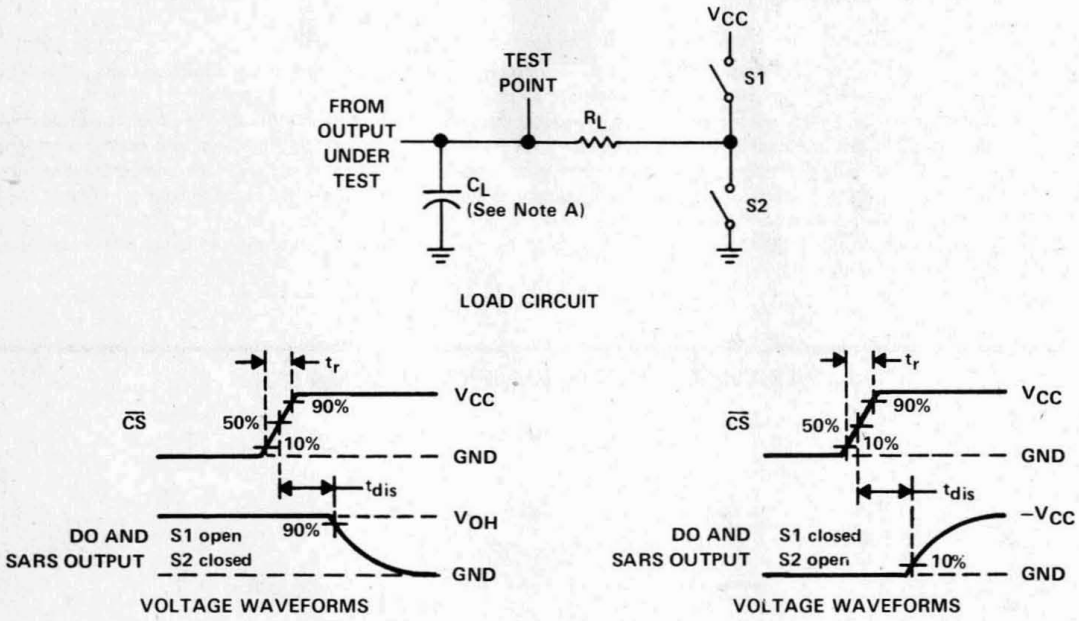


FIGURE 2. DATA OUTPUT TIMING



NOTE A: C_L includes probe and jig capacitance.

FIGURE 3. OUTPUT DISABLE TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS

UNADJUSTED OFFSET ERROR
vs
REFERENCE VOLTAGE

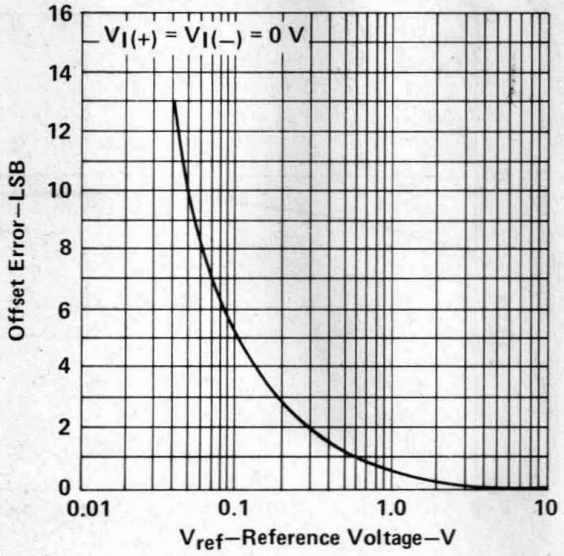


FIGURE 4

LINEARITY ERROR
vs
REFERENCE VOLTAGE

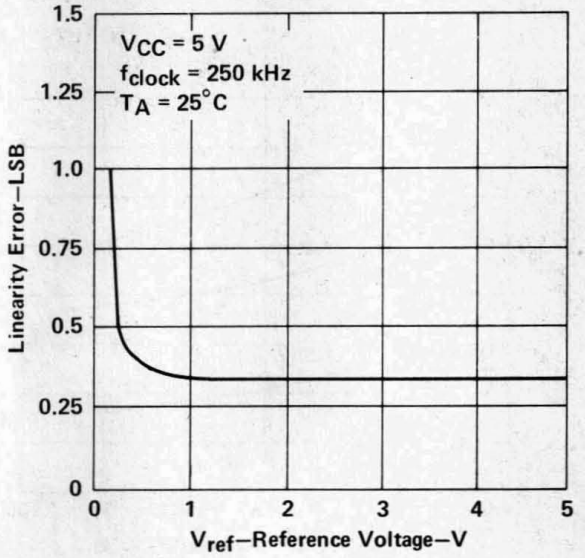


FIGURE 5

LINEARITY ERROR
vs
FREE-AIR TEMPERATURE

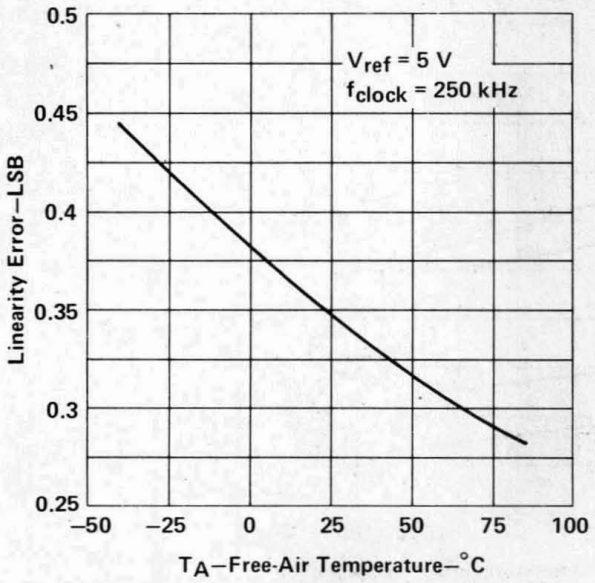


FIGURE 6

LINEARITY ERROR
vs
CLOCK FREQUENCY

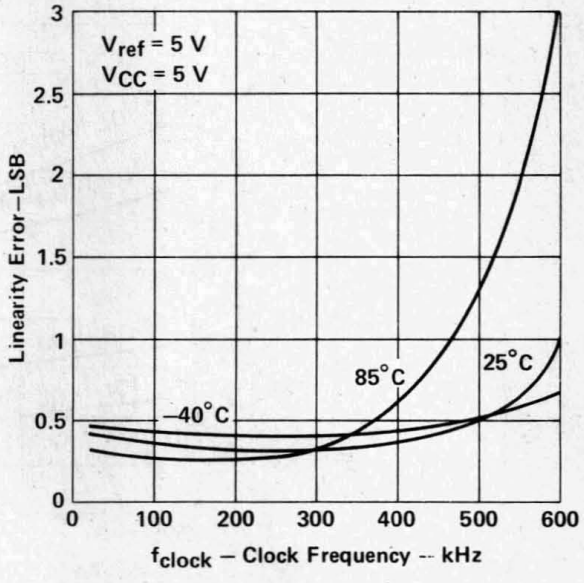


FIGURE 7

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

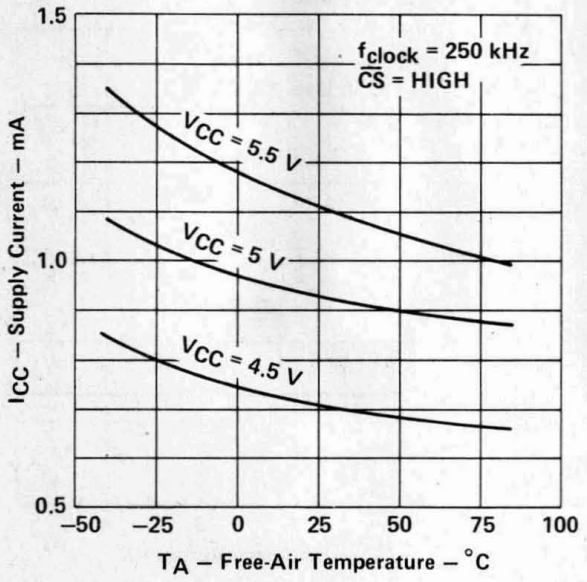


FIGURE 8

SUPPLY CURRENT
vs
CLOCK FREQUENCY

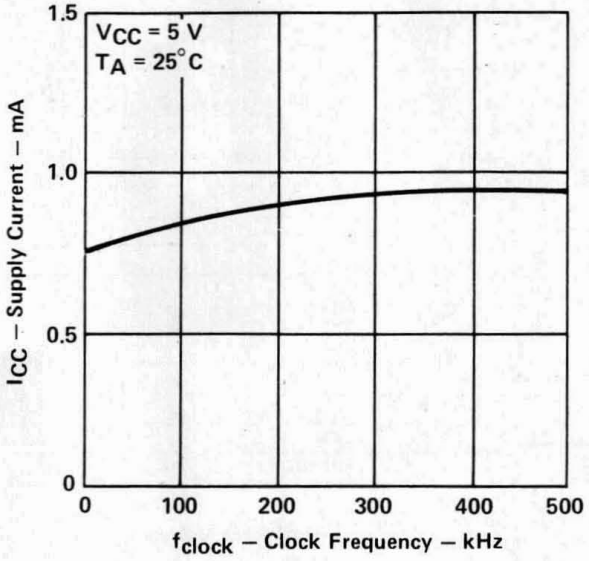


FIGURE 9

OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

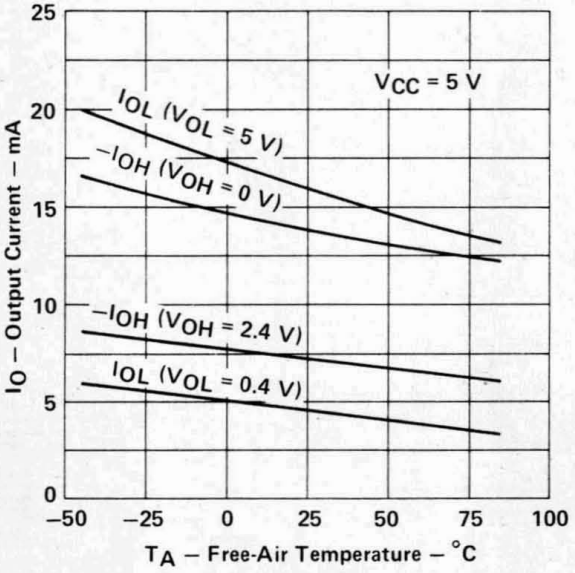
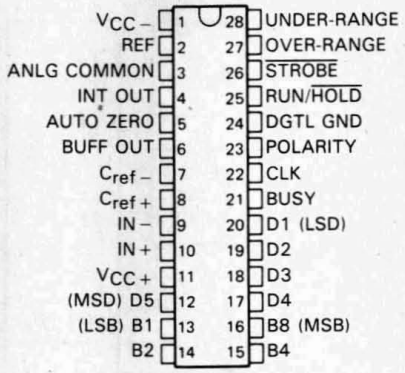


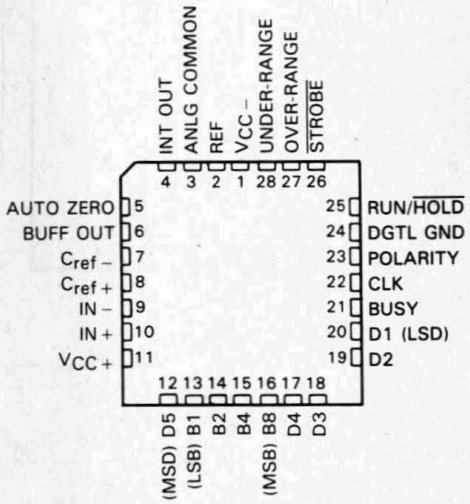
FIGURE 10

- **Advanced LinCMOS™ Technology**
- **Zero Reading for 0-V Input**
- **Precision Null Detection with True Polarity at Zero**
- **1-pA Typical Input Current**
- **True Differential Input**
- **Multiplexed Binary-Coded-Decimal Output**
- **Low Rollover Error: ±1 Count Maximum**
- **Control Signals Allow Interfacing with UARTs or Microprocessors**
- **Autoranging Capability with Over- and Under-Range Signals**
- **TTL-Compatible Outputs**
- **Direct Replacement for Teledyne TSC7135, Intersil ICL7135, Maxim ICL7135, and Siliconix Si7135**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The ICL7135C and TLC7135C converters are manufactured with Texas Instruments highly efficient Advanced LinCMOS™ technology. This 4 1/2-digit dual-slope-integrating analog-to-digital converter is designed to provide interfaces to both a microprocessor and a visual display. The digit-drive outputs D1 through D4 and multiplexed binary-coded-decimal outputs, B1 through B4, provide an interface for LED or LCD decoder/drivers as well as microprocessors.

The ICL7135C and TLC7135C offer 50-ppm (one part in 20,000) resolution with a maximum linearity error of one count. The zero error is less than 10 μV and zero drift is less than 0.5 μV/°C. Source-impedance errors are minimized by low input current (less than 10 pA). Rollover error is limited to ±1 count.

The BUSY, $\overline{\text{STROBE}}$, RUN/$\overline{\text{HOLD}}$, OVER-RANGE, and UNDER-RANGE control signals support microprocessor-based measurement systems. The control signals also can support remote data acquisition systems with data transfer via universal asynchronous receiver transmitters (UARTs).

The ICL7135C and TLC7135C are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS†

SYMBOLIZATION		OPERATING
DEVICE	PACKAGE SUFFIX	TEMPERATURE RANGE
ICL7135C	FN, N	0°C to 70°C
TLC7135C	FN, N	0°C to 70°C

† In many instances, these ICs may have ICL7135C and TLC7135C symbolization on the package.

Caution. This device has limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage.

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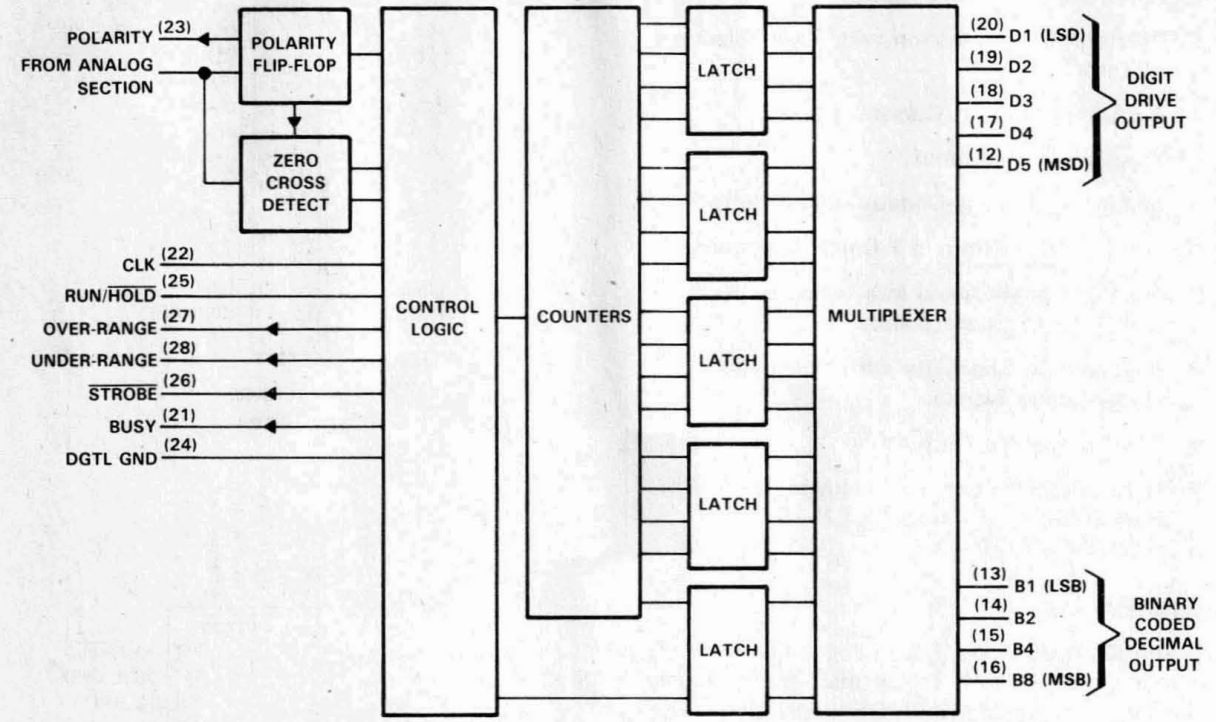
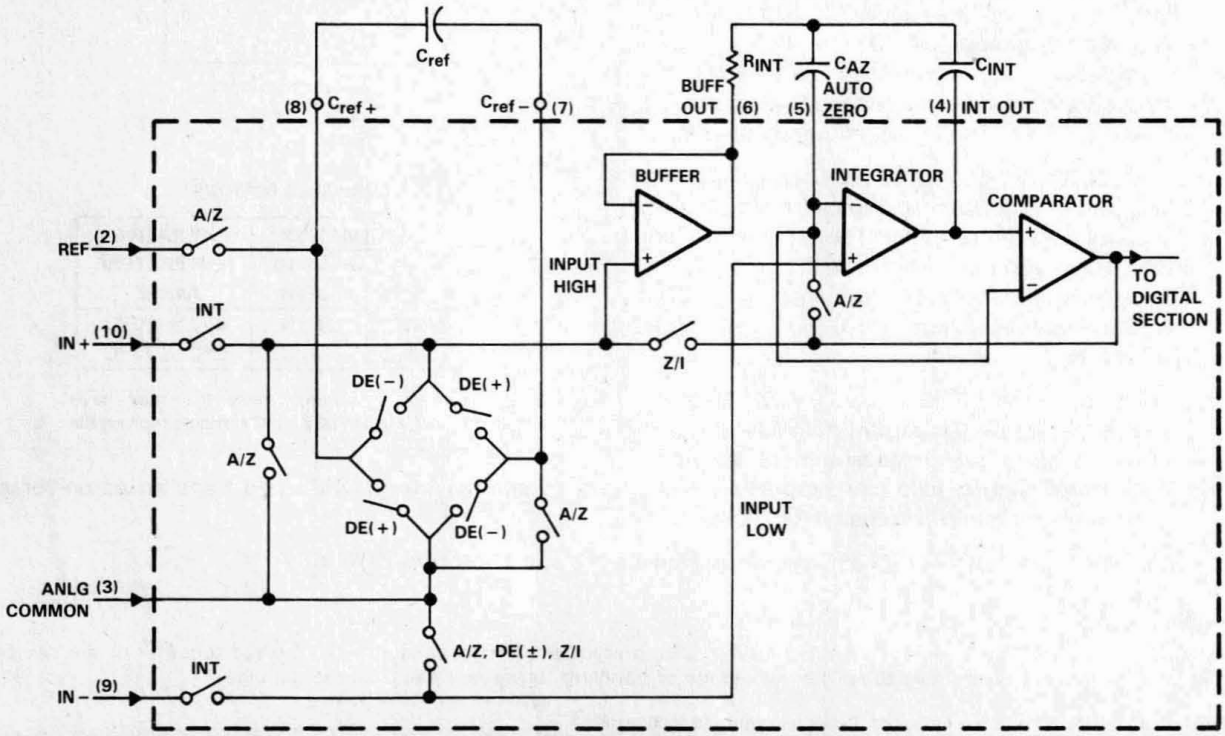
functional block diagram



ANALOG SECTION



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (V_{CC+} with respect to V_{CC-}) . . . . . 15 V
Analog input voltage (pin 9 or pin 10) . . . . . V_{CC-} to V_{CC+}
Reference voltage range . . . . . V_{CC-} to V_{CC+}
Clock input voltage range . . . . . 0 V to V_{CC+}
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C
Case temperature for 10 seconds: FN package . . . . . 260°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	4	5	6	V
Supply voltage, V_{CC-}	−3	−5	−8	V
Reference voltage, V_{ref}		1		V
High-level input voltage, CLK, RUN/$\overline{HOLD}$, V_{IH}	2.8			V
Low-level input voltage, CLK, RUN/$\overline{HOLD}$, V_{IL}			0.8	V
Differential input voltage, V_{ID}	V_{CC-} +1		V_{CC+} −0.5	V
Maximum operating frequency, f_{clock} (see Note 1)	1.2	2		MHz
Operating free-air temperature range, T_A	0		70	°C

NOTE 1: Clock frequency range extends down to 0 Hz.

electrical characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{ref} = 1 V, f_{clock} = 120 kHz, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	D1-D5,B1,B2,B4,B8	I_O = −1 mA		2.4		5	V
		Other outputs	I_O = −10 μA		4.9		5	
V_{OL}	Low-level output voltage		I_O = 1.6 mA				0.4	V
	Peak-to-peak output noise voltage (see Note 2)		V_{ID} = 0,	Full Scale = 2 V		15		μV
α_{VO}	Zero-reading temperature coefficient of output voltage		V_{ID} = 0,	0°C ≤ T_A ≤ 70°C		0.5	2	μV/°C
I_{IH}	High-level input current		V_I = 5 V,	0°C ≤ T_A ≤ 70°C		0.1	10	μA
I_{IL}	Low-level input current		V_I = 0 V,	0°C ≤ T_A ≤ 70°C		−0.02	−0.1	mA
I_I	Input leakage current, pins 9 and 10		V_{ID} = 0	T_A = 25°C		1	10	pA
				0°C ≤ T_A ≤ 70°C			250	
I_{CC+}	Positive supply current		f_{clock} = 0	T_A = 25°C		1	2	mA
				0°C ≤ T_A ≤ 70°C			3	
I_{CC-}	Negative supply current		f_{clock} = 0	T_A = 25°C		−0.8	−2	mA
				0°C ≤ T_A ≤ 70°C			−3	
C_{pd}	Power dissipation capacitance		See Note 3			40		pF

NOTES: 2. This is the peak-to-peak value that is not exceeded 95% of the time.
3. Factor relating clock-frequency to increase in supply current. At V_{CC+} = 5 V

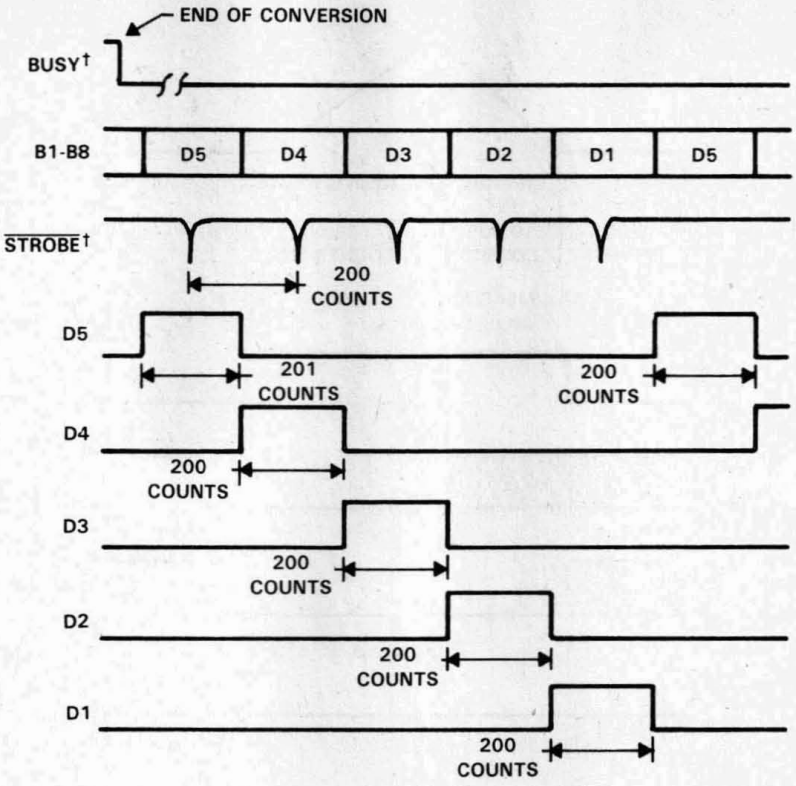
$$I_{CC+} = I_{CC+(f_{clock} = 0)} + C_{pd} \times 5\ V \times f_{clock}$$

operating characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{ref} = 1 V, f_{clock} = 120 kHz, T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
α_{FS}	Full-scale temperature coefficient (see Note 4)	V_{ID} = 2 V, 0°C ≤ T_A ≤ 70°C			5	ppm/°C
	Linearity error	−2 V ≤ V_{ID} ≤ 2 V		0.5	1	count
	Differential linearity error (see Note 5)	−2 V ≤ V_{ID} ≤ 2 V		0.01		LSB
	± Full-scale symmetry error (see Note 6) (rollover error)	V_{ID} = ±2 V		0.5	1	count
	Display reading with 0-V input	V_{ID} = 0, 0°C ≤ T_A ≤ 70°C	−0.0000	±0.0000	+0.0000	Digital Reading
	Display reading in ratiometric operation	V_{ID} = V_{ref}, T_A = 25°C	+0.9998	+0.9999	+1.0000	Digital
		0°C ≤ T_A ≤ 70°C	+0.9995	+0.9999	+1.0005	Reading

NOTES: 4. This parameter is measured with an external reference having a temperature coefficient of less than 0.01 ppm/°C.
5. The magnitude of the difference between the worst case step of adjacent counts and the ideal step.
6. Rollover error is the difference between the absolute values of the conversion for 2 V and −2 V.

timing diagrams



† Delay between BUSY going low and the first $\overline{\text{STROBE}}$ pulse is dependent upon the analog input.

FIGURE 1

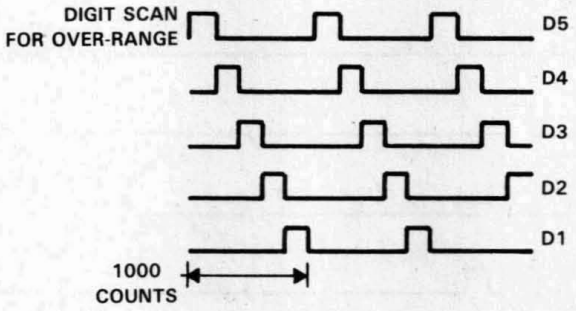


FIGURE 2

timing diagrams (continued)

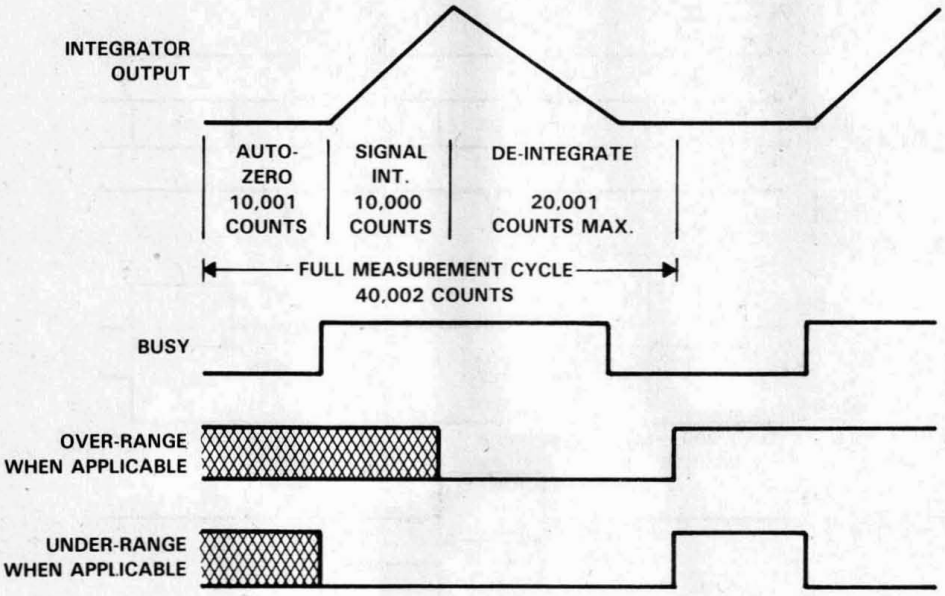
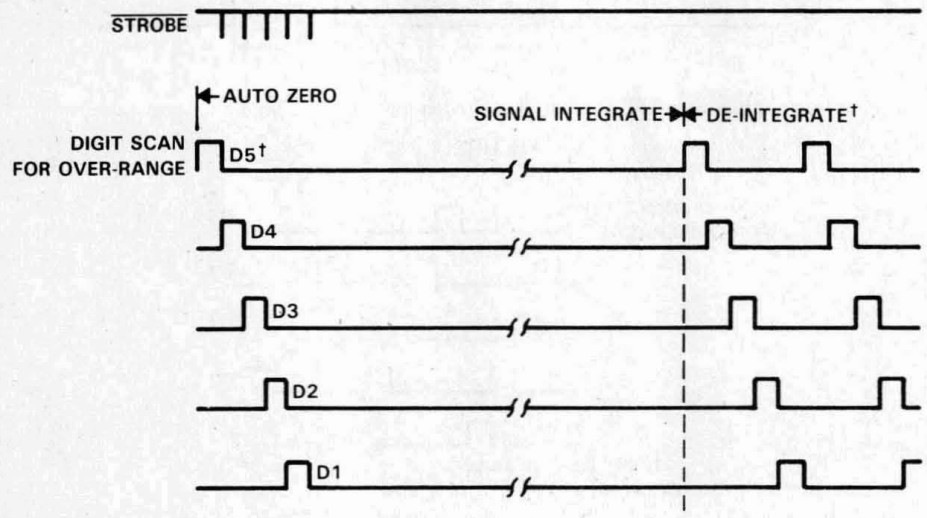


FIGURE 3



†First D5 of AUTO ZERO and DE-INTEGRATE is one count longer.

FIGURE 4

PRINCIPLES OF OPERATION

A measurement cycle for the ICL7135C and TLC7135C consists of the following four phases.

1. Auto-Zero Phase. The internal IN+ and IN− inputs are disconnected from the pins and internally connected to ANLG COMMON. The reference capacitor is charged to the reference voltage. The system is configured in a closed loop and the auto-zero capacitor is charged to compensate for offset voltages in the buffer amplifier, integrator, and comparator. The auto-zero accuracy is limited only by the system noise, and the overall offset, as referred to the input, is less than 10 μV.
2. Signal Integrate Phase. The auto-zero loop is opened and the internal IN+ and IN− inputs are connected to the external pins. The differential voltage between these inputs is integrated for a fixed period of time. If the input signal has no return with respect to the converter power supply, IN− can be tied to ANLG COMMON to establish the correct common-mode voltage. Upon completion of this phase, the polarity of the input signal is recorded.
3. De-integrate Phase. The reference is used to perform the de-integrate task. The internal IN− is internally connected to ANLG COMMON and IN+ is connected across the previously charged reference capacitor. The recorded polarity of the input signal is used to ensure that the capacitor will be connected with the correct polarity so that the integrator output polarity will return to zero. The time, which is required for the output to return to zero, is proportional to the amplitude of the input signal. The return time is displayed as a digital reading and is determined by the equation 10,000 x (V_{ID}/V_{ref}). The maximum or full-scale conversion occurs when V_{ID} is two times V_{ref}.
4. Zero Integrator Phase. The internal IN− is connected to ANLG COMMON. The system is configured in a closed loop to cause the integrator output to return to zero. Typically this phase requires 100 to 200 clock pulses. However, after an over-range conversion, 6200 pulses are required.

description of analog circuits

input signal range

The common mode range of the input amplifier extends from 1 V above the negative supply to 1 V below the positive supply. Within this range, the common mode rejection ratio (CMRR) is typically 86 dB. Both differential and common mode voltages cause the integrator output to swing. Therefore, care must be exercised to assure the integrator output does not saturate.

analog common

Analog common (ANLG COMMON) is connected to the internal IN− during the auto-zero, de-integrate, and zero integrator phases. If IN− is connected to a voltage which is different than analog common during the signal integrate phase, the resulting common mode voltage will be rejected by the amplifier. However, in most applications, IN LO will be set at a known fixed voltage (power supply common for instance). In this application, analog common should be tied to the same point, thus removing the common mode voltage from the converter. Removing the common mode voltage in this manner will slightly increase conversion accuracy.

reference

The reference voltage is positive with respect to analog common. The accuracy of the conversion result is dependent upon the quality of the reference. Therefore, to obtain a high accuracy conversion, a high quality reference should be used.

description of digital circuits

RUN/$\overline{\text{HOLD}}$ input

When the RUN/$\overline{\text{HOLD}}$ input is high or open, the device will continuously perform measurement cycles every 40,002 clock pulses. If this input is taken low, the IC will continue to perform the ongoing measurement cycle and then hold the conversion reading for as long as the pin is held low. If the pin is held low after completion of a measurement cycle, a short positive pulse (greater than 300 ns) will initiate a new measurement cycle. If this positive pulse occurs before the completion of a measurement cycle, it will not be recognized. The first STROBE pulse, which occurs 101 counts after the end of a measurement cycle, is an indication of the completion of a measurement cycle. Thus, the positive pulse could be used to trigger the start of a new measurment after the first STROBE pulse.

$\overline{\text{STROBE}}$ input

Negative going pulses from this input are used to transfer the BCD conversion data to external latches, UARTS, or microprocesors. At the end of the measurement cycle, the digit-drive (D5) input goes high and remains high for 201 counts. The most significant digit (MSD) BCD bits are placed on the BCD pins. After the first 101 counts, halfway through the duration of output D1-D5 going high, the $\overline{\text{STROBE}}$ pin goes low for 1/2 clock pulse width. The placement of the $\overline{\text{STROBE}}$ pulse at the midpoint of the D5 high pulse allows the information to be latched into an external device on either a low-level or an edge. Such placement of the $\overline{\text{STROBE}}$ pulse also ensures that the BCD bits for the second MSD will not yet be competing for the BCD lines and latching of the correct bits is assured. The above process is repeated for the second MSD and the D4 output. Similarly, the process is repeated through the least significant digit (LSD). Subsequently, inputs D5 through D1 and the BCD lines will continue scanning without the inclusion of $\overline{\text{STROBE}}$ pulses. This subsequent continuous scanning causes the conversion results to be continuously displayed. Such subsequent scanning does not occur when an over-range condition occurs.

BUSY output

The BUSY output goes high at the beginning of the signal integrate phase and remains high until the first clock pulse after zero-crossing or at the end of the measurement cycle if an over-range condition occurs. It is possible to use the BUSY pin to serially transmit the conversion result. Serial transmission can be accomplished by ANDing the BUSY and CLOCK signals and transmitting the ANDed output. The transmitted output consists of 10,001 clock pulses, which occur during the signal integrate phase, and the number of clock pulses, which occur during the de-integrate phase. The conversion result can be obtained by subtracting 10,001 from the total number of clock pulses.

OVER-RANGE output

When an over-range condition occurs, this pin goes high after the BUSY signal goes low at the end of the measurement cycle. As previously noted, the BUSY signal remains high until the end of the measurement cycle when an over-range condition occurs. The OVER-RANGE output goes high at end of BUSY and goes low at the beginning of the de-integrate phase in the next measurement cycle.

UNDER-RANGE output

At the end of the BUSY signal, this pin goes high if the conversion result is less than or equal to 9% (count of 1800) of the full-scale range. The UNDER-RANGE output is brought low at the beginning of the signal integrate phase of the next measurement cycle.

PRINCIPLES OF OPERATION

POLARITY output

The POLARITY output is high for a positive input signal and is updated at the beginning of each de-integrate phase. The polarity output is valid for all inputs including ±0 and over-range signals.

digit-drive (D5, D4, D2 and D1) outputs

Each digit-drive output (D1 through D5) sequentially goes high for 200 clock pulses. This sequential process is continuous unless an over-range occurs. When an over-range occurs, all of the digit drive outputs are blanked from the end of the strobe sequence until the beginning of the de-integrate phase (when the sequential digit drive activation begins again). The blanking activity, during an over-range condition, may be used to cause the display to flash and indicate the over-range condition.

BCD outputs

The BCD bits (B8, B4, B2 and B1) for a given digit are sequentially activated on these outputs. Simultaneously, the appropriate Digit-drive line for the given digit is activated.

system aspects

integrating resistor

The value of the integrating resistor (R_{INT}) is determined by the full scale input voltage and the output current of the integrating amplifier. The integrating amplifier can supply 20 μA of current with negligible non-linearity. The equation for determining the value of this resistor is as follows:

$$R_{INT} = \frac{\text{FULL-SCALE VOLTAGE}}{I_{INT}}$$

Integrating amplifier current, I_{INT}, from 5 to 40 μA will yield good results. However, the nominal and recommended current is 20 μA.

integrating capacitor

The product of the integrating resistor and capacitor should be selected to give the maximum voltage swing without causing the integrating amplifier output to saturate and get too close to the power supply voltages. If the amplifier output is within 0.3 V of either supply, saturation will occur. With ±5-V supplies and ANLG COMMON connected to ground, the designer should design for a ±3.5-V to ±4-V integrating amplifier swing. A nominal capacitor value is 0.47 μF. The equation for determining the value of the integrating capacitor (C_{INT}) is as follows:

$$C_{INT} = \frac{10{,}000 \times \text{CLOCK PERIOD} \times I_{INT}}{\text{INTEGRATOR OUTPUT VOLTAGE SWING}}$$

where: I_{INT} is nominally 20 μA.

Capacitors with large tolerances and high dielectric absorption can induce conversion inaccuracies. A capacitor, which is too small could cause the integrating amplifier to saturate. High dielectric absorption causes the effective capacitor value to be different during the signal integrate and de-integrate phases. Polypropylene capacitors have very low dielectric absorption. Polystyrene and Polycarbonate capacitors have higher dielectric absorption, but also work well.

PRINCIPLES OF OPERATION

auto-zero and reference capacitor

Large capacitors will tend to reduce noise in the system. Dielectric absorption is unimportant except during power-up or overload recovery. Typical values are 1 μF.

reference voltage

For high-accuracy absolute measurements, a high quality reference should be used.

rollover resistor and diode

The ICL7135C and TLC7135C have a small rollover error, however it can be corrected. The correction is to connect the cathode of any silicon diode to the INT OUT pin and the anode to a resistor. The other end of the resistor is connected to ANLG COMMON or ground. For the recommended operating conditions the resistor value is 100 kΩ. This value may be changed to correct any rollover error which has not been corrected. In many non-critical applications, the resistor and diode are not needed.

maximum clock frequency

For most dual-slope A/D converters, the maximum conversion rate is limited by the frequency response of the comparator. In this circuit, the comparator follows the integrator ramp with a 3 μs delay. Therefore, with a 160-kHz clock frequency (6 μs period), half of the first reference integrate clock period is lost in delay. Hence, the meter reading will change from 0 to 1 with a 50-μV input, 1 to 2 with a 150-μV input, 2 to 3 with a 250-μV input, etc. This transition at midpoint is desirable; however, if the clock frequency is increased appreciably above 160 kHz, the instrument will flash "1" on noise peaks even when the input is shorted. The above transition points assume a 2-V input range is equivalent to 20,000 clock cycles.

If the input signal is always of one polarity, comparator delay need not be a limitation. Clock rates of 1 MHz are possible since non-linearity and noise do not increase substantially with frequency. For a fixed clock frequency, the extra count or counts caused by comparator delay will be a constant and can be subtracted out digitally.

For signals with both polarities, the clock frequency can be extended above 160 kHz without error by using a low value resistor in series with the integrating capacitor. This resistor causes the integrator to jump slightly towards the zero-crossing level at the beginning of the de-integrate phase and thus, compensates for the comparator delay. This series resistor should be 10 Ω to 50 Ω. This approach allows clock frequencies up to 480 kHz.

minimum clock frequency

The minimum clock frequency limitations result from capacitor leakage from the auto-zero and reference capacitors. Measurement cycles as high as 10 s are not influenced by leakage error.

rejection of 50 Hz or 60 Hz pickup

To maximize the rejection of 50 Hz or 60 Hz pickup, the clock frequency should be chosen so that an integral multiple of 50 Hz or 60 Hz periods occur during the signal integrate phase. To achieve rejection of these signals, some clock frequencies which could be used are as follows:

50 Hz: 250, 166.66, 125, 100 kHz, etc.
60 Hz: 300, 200, 150, 120, 100, 40, 33.33 kHz, etc.

PRINCIPLES OF OPERATION

zero-crossing flip-flop

This flip-flop interrogates the comparator's zero-crossing status. The interrogation is performed after the previous clock cycle and the positive half of the ongoing clock cycle have occurred so that any comparator transients which result from the clock pulses do not affect the detection of a zero-crossing. This procedure delays the zero-crossing detection by one clock cycle. To eliminate the inaccuracy, which is caused by this delay, the counter is disabled for one clock cycle at the beginning of the de-integrate phase. Therefore, when the zero-crossing is detected one clock cycle later than the zero-crossing actually occurs, the correct number of counts is displayed.

noise

The peak-to-peak noise around zero is approximately 15 μV (peak-to-peak value not exceeded 95% of the time). Near full scale, this value increases to approximately 30 μV. Much of the noise originates in the auto-zero loop, and is proportional to the ratio of the input signal to the reference.

analog and digital grounds

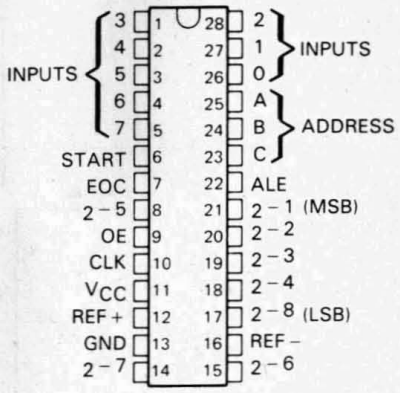
For high-accuracy applications, ground loops must be avoided. Return currents from digital circuits must not be sent to the analog ground line.

power supplies

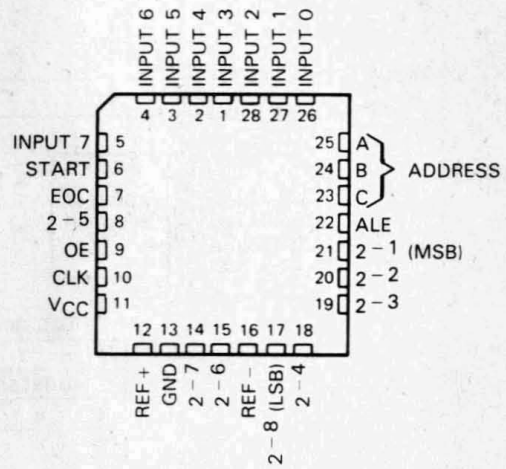
The ICL7135C and TLC7135C are designed to work with $\pm$5-V power supplies. However, 5-V operation is possible if the input signal does not vary more than $\pm$1.5 V from mid-supply.

- Total Unadjusted Error . . . ±0.75 LSB Max for TL0808 and ±1.25 LSB Max for TL0809 Over Temperature Range
- Ideal for Battery Operated, Portable Instrumentation Applications
- Resolution of 8 Bits
- 100 μs Conversion Time
- Ratiometric Conversion
- Monotonic Over the Entire A/D Conversion Range
- No Missing Codes
- Easy Interface with Microprocessors
- Latched 3-State Outputs
- Latched Address Inputs
- Single 2.75-V to 5.5-V Supply
- Extremely Low Power Consumption . . . 0.3 mW Typ
- Improved Direct Replacements for ADC0808, ADC0809

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The TL0808 and TL0809 are monolithic CMOS devices with an 8-channel multiplexer, an 8-bit analog-to-digital (A/D) converter, and microprocessor-compatible control logic. The 8-channel multiplexer can be controlled by a microprocessor through a 3-bit address decoder with address load to select any one of eight single-ended analog switches connected directly to the comparator. The 8-bit A/D converter uses the successive-approximation conversion technique featuring a high-impedance threshold detector, a switched-capacitor array, a sample-and-hold, and a successive-approximation register (SAR). Detailed information on interfacing to most popular microprocessors is readily available from the factory. These devices are designed to operate from common microprocessor control buses, with three-state output latches driving the data bus. The devices can be made to appear to the microprocessor as a memory location or an I/O port.

The comparison and converting methods used eliminate the possibility of missing codes, nonmonotonicity, and the need for zero or full-scale adjustment. Also featured are latched 3-state outputs from the SAR and latched inputs to the multiplexer address decoder. The single 2.75-V to 5.5-V supply and extremely low power requirements make the TL0808 and TL0809 especially useful for a wide variety of applications including portable battery and LCD applications. Ratiometric conversion is made possible by access to the reference voltage input terminals.

The TL0808 and TL0809 are characterized for operation from −40°C to 85°C.

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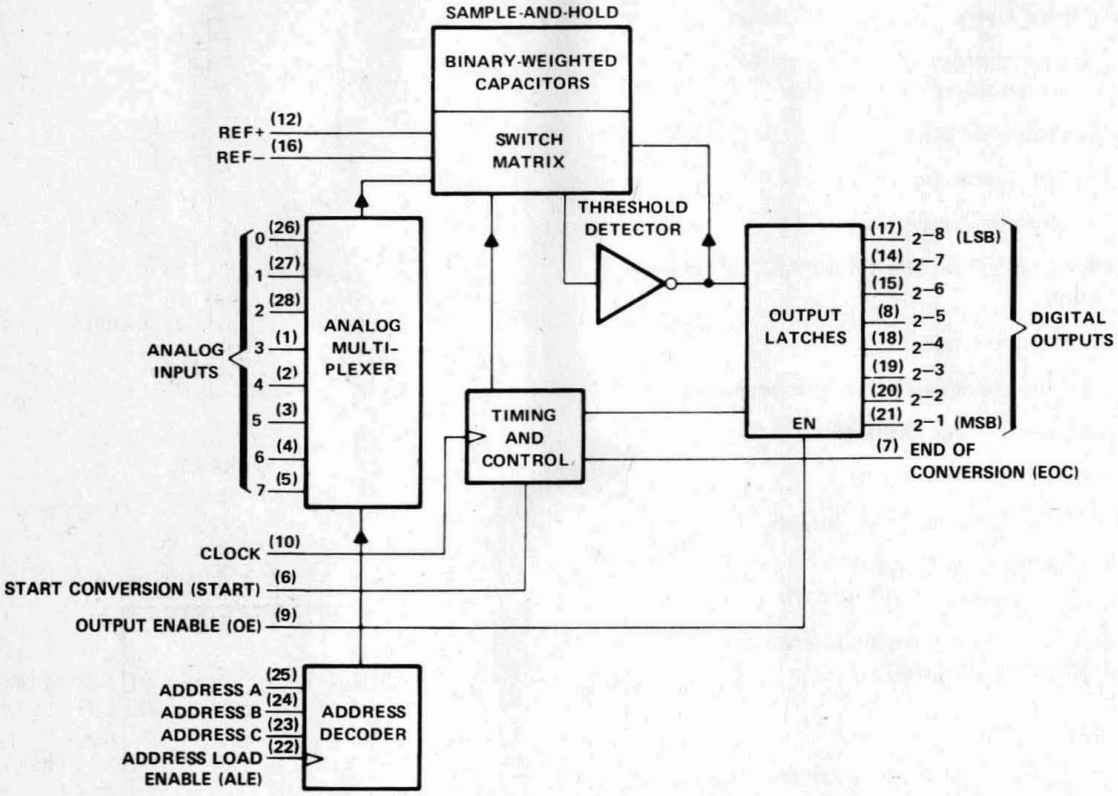
functional block diagram (positive logic)

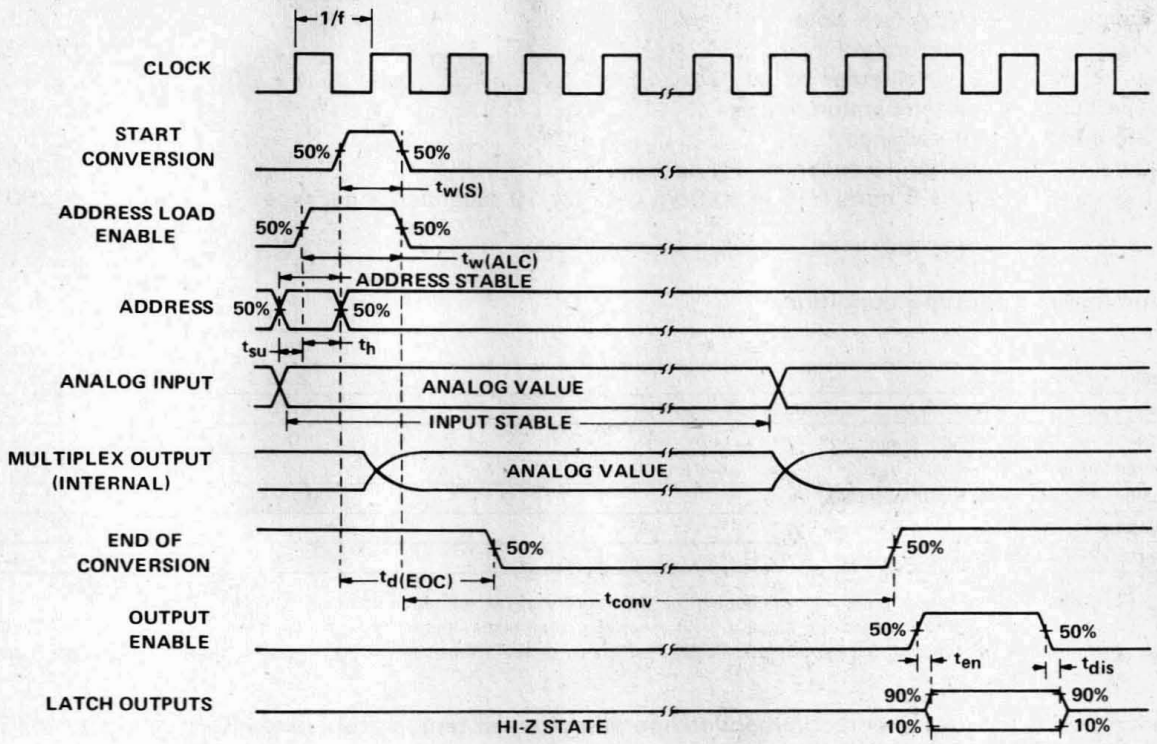


MULTIPLEXER FUNCTION TABLE

INPUTS				SELECTED
ADDRESS			ADDRESS	ANALOG
C	B	A	STROBE	CHANNEL
L	L	L	↑	0
L	L	H	↑	1
L	H	L	↑	2
L	H	H	↑	3
H	L	L	↑	4
H	L	H	↑	5
H	H	L	↑	6
H	H	H	↑	7

H = high level, L = low level
↑ = low-to-high transition

operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range: control inputs . . . . . −0.3 to 15 V
all other inputs . . . . . −0.3 V to V_{CC} + 0.3 V
Operating free-air temperature range . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	2.75		5.5	V
Positive reference voltage, V_{ref+} (see Notes 2, 3, and 4)	2.75	V_{CC}	V_{CC}+0.1	V
Negative reference voltage, V_{ref-} (see Notes 2, 3, and 4)	−0.1	0		V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 4)		3		V
High-level input voltage, control inputs, V_{IH}	0.7 V_{CC}			V
Low-level input voltage, control inputs, V_{IL}			0.3 V_{CC}	V
Operating free-air temperature, T_A (see Note 4)	−40		85	°C

NOTES: 2. The accuracy of the conversion will depend on the stability of the reference voltages applied.
3. Analog voltages greater than or equal to V_{ref+} convert to all highs, and all voltages less than V_{ref-} convert to all lows.
4. For proper operation of the TL0808 and TL0809 at free-air temperatures below 0°C, V_{CC} and ($V_{ref+} - V_{ref-}$) should not be less than 3 V.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 3 V to 5.25 V (unless otherwise noted)

total device

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_O = −360 μA	V_{CC}−0.6			V
V_{OL}	Low-level output voltage	Data outputs	I_O = 1.6 mA			0.45	V
		End of conversion	I_O = 1.2 mA			0.45	
I_{OZ}	Off-state (high-impedance-state) output current		V_O = V_{CC}			1	μA
			V_O = 0			−1	
I_I	Control input current at maximum input voltage		V_I = 15 V			1	μA
I_{IL}	Low-level control input current		V_I = 0			−1	μA
I_{CC}	Supply current		V_{CC} = 3 V, f_{clock} = 640 kHz		100	500	μA
			V_{CC} = 5 V, f_{clock} = 640 kHz		0.3	3	mA
C_i	Input capacitance, control inputs		T_A = 25°C		10	15	pF
C_o	Output capacitance, data outputs		T_A = 25°C		10	15	pF
	Resistance from pin 12 to pin 16			1	1000		kΩ

†Typical values are at V_{CC} = 3 V and T_A = 25°C.

analog multiplexer

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{on}	Channel on-state current (see Note 5)	V_I = 3 V,	f_{clock} = 640 kHz			2	μA
		V_I = 0,	f_{clock} = 640 kHz			−2	
I_{off}	Channel off-state current	V_{CC} = 3 V, T_A = 25°C	V_I = 3 V		10	200	nA
			V_I = 0		−10	−200	
		V_{CC} = 3 V	V_I = 3 V			1	μA
			V_I = 0			−1	

†Typical values are at V_{CC} = 3 V and T_A = 25°C.

NOTE 5: Channel on-state current is primarily due to the bias current into or out of the threshold detector, and it varies directly with clock frequency.

timing requirements, T_A = 25°C, V_{CC} = V_{ref+} = 3 V, V_{ref-} = 0 (unless otherwise noted)

			MIN	NOM	MAX	UNIT
t_{conv}	Conversion time (see Note 6)		90	100	116	μs
f_{clock}	Clock frequency	V_{CC} = 2.75 V to 4 V	10		640	kHz
		V_{CC} = 4 V to 5.5 V	10		1280	
$t_{w(s)}$	Start pulse duration		200			ns
$t_{w(ALC)}$	Address load control pulse duration		200			ns
t_{su}	Address setup time		50			ns
t_h	Address hold time		50			ns
$t_{d(EOC)}$	Delay time, end of conversion output (see Notes 6 and 7)		0		14.5	μs

operating characteristics, T_A = 25°C, V_{CC} = V_{ref+} = 3 V, V_{ref-} = 0, f_{clock} = 640 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TL0808			TL0809			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
k_{SVS}	Supply voltage sensitivity	V_{CC} = V_{ref+} = 3 V to 5.25 V, T_A = −40°C to 85°C, See Note 8			±0.05			±0.05		%/V
	Linearity error (see Note 9)				±0.5			±1		LSB
	Zero error (see Note 10)				±0.5			±0.5		LSB
	Total unadjusted error (See Note 11)	f_{clock} = 125 kHz	T_A = 25°C		±0.25	±0.5		±0.5	±1	LSB
			T_A = −40°C to 85°C			±0.75			±1.25	
t_{en}	Output enable time	C_L = 50 pF, R_L = 10 kΩ			80	250		80	250	ns
t_{dis}	Output disable time	C_L = 10 pF, R_L = 10 kΩ			105	300		105	300	ns

†Typical values for all except supply voltage sensitivity are at V_{CC} = 3 V.

NOTES:
6. Refer to the operating sequence diagram.
7. For clock frequencies other than 640 kHz, $t_{d(EOC)}$ maximum is 8 clock periods plus 2 μs.
8. Supply voltage sensitivity relates to the ability of an analog-to-digital converter to maintain accuracy as the supply voltage varies. The supply and V_{ref+} are varied together and the change in accuracy is measured with respect to full-scale.
9. Linearity error is the maximum deviation from a straight line through the end points of the A/D transfer characteristic.
10. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
11. Total unadjusted error is the maximum sum of linearity error, zero error, and full-scale error.

PRINCIPLES OF OPERATION

The TL0808 and TL0809 each consists of an analog signal multiplexer, an 8-bit successive-approximation converter, and related control and output circuitry.

multiplexer

The analog multiplexer selects 1 of 8 single-ended input channels as determined by the address decoder. Address load control loads the address code into the decoder on a low-to-high transition. The output latch is reset by the positive-going edge of the start pulse. Sampling also starts with the positive-going edge of the start pulse and lasts for 32 clock periods. The conversion process may be interrupted by a new start pulse before the end of 64 clock periods. The previous data will be lost if a new start of conversion occurs before the 64th clock pulse. Continuous conversion may be accomplished by connecting the End-of-Conversion output to the start input. If used in this mode an external pulse should be applied after power up to assure start up.

converter

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (Figure 1). In the first phase of the conversion process, the analog input is sampled by closing switch S_C and all S_T switches, and by simultaneously charging all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference voltage. In the switching sequence, all eight capacitors are examined separately until all 8 bits are identified, and then the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 128). Node 128 of this capacitor is switched to the reference voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF−. If the voltage at the summing node is greater than the trip-point of the threshold detector (approximately one-half the V_{CC} voltage), a bit is placed in the output register, and the 128-weight capacitor is switched to REF−. If the voltage at the summing node is less than the trip point of the threshold detector, this 128-weight capacitor remains connected to REF+ through the remainder of the capacitor-sampling (bit-counting) process. The process is repeated for the 64-weight capacitor, the 32-weight capacitor, and so forth down the line, until all bits are counted.

With each step of the capacitor-sampling process, the initial charge is redistributed among the capacitors. The conversion process is successive approximation, but relies on charge redistribution rather than a successive-approximation register (and reference DAC) to count and weigh the bits from MSB to LSB.

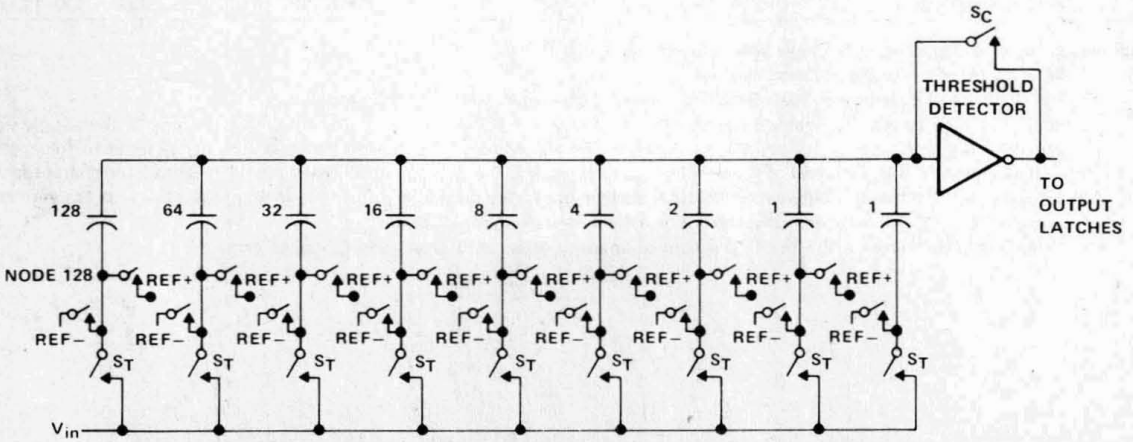


FIGURE 1. SIMPLIFIED MODEL OF THE SUCCESSIVE-APPROXIMATION SYSTEM

TL500I, TL500C, TL501I, TL501C, TL502C, TL503C
ANALOG-TO-DIGITAL-CONVERTER BUILDING BLOCKS

D2477 DECEMBER 1979—REVISED JANUARY 1989

TL500I, TL500C, TL501I, TL501C
ANALOG PROCESSORS

- True Differential Inputs
- Automatic Zero
- Automatic Polarity
- High Input Impedance . . . 10^9 Ohms Typically

TL500I, TL500C CAPABILITIES

- Resolution . . .14 Bits (with TL502C)
- Linearity Error . . . 0.001%
- 4 1/2-Digit Readout Accuracy with External Precision Reference

TL502C/TL503C
DIGITAL PROCESSORS

- Fast Display Scan Rates
- Internal Oscillator May Be Driven or Free-Running
- Interdigit Blanking
- Over-Range Blanking
- 4 1/2-Digit Display Circuitry
- High-Sink-Current Digit Driver for Large Displays

TL501I, TL501C CAPABILITIES

- Resolution . . . 10-13 Bits (with TL502C)
- Linearity Error . . . 0.01%
- 3 1/2-Digit Readout Accuracy

TL502C CAPABILITIES

- Compatible with Popular Seven-Segment Common-Anode Displays
- High-Sink-Current Segment Driver for Large Displays

TL503C CAPABILITIES

- Multiplexed BCD Outputs
- High-Sink-Current BCD Outputs

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

description

The TL500I, TL500C, TL501I, and TL501C analog processors and TL502C and TL503C digital processors provide the basic functions for a dual-slope-integrating analog-to-digital converter.

The TL500 and TL501 contain the necessary analog switches and decoding circuits, reference voltage generator, buffer, integrator, and comparator. These devices may be controlled by the TL502C, TL503C, by discrete logic, or by a software routine in a microprocessor.

The TL502C and TL503C each includes oscillator, counter, control logic, and digit enable circuits. The TL502C provides multiplexed outputs for seven-segment displays, while the TL503C has multiplexed BCD outputs.

When used in complementary fashion, these devices form a system that features automatic zero-offset compensation, true differential inputs, high input impedance, and capability for 4 1/2-digit accuracy. Applications include the conversion of analog data from high-impedance sensors of pressure, temperature, light, moisture, and position. Analog-to-digital-logic conversion provides display and control signals for weight scales, industrial controllers, thermometers, light-level indicators, and many other applications.

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TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

principles of operation

The basic principle of dual-slope-integrating converters is relatively simple. A capacitor, C_X, is charged through the integrator from V_{CT} for a fixed period of time at a rate determined by the value of the unknown voltage input. Then the capacitor is discharged at a fixed rate (determined by the reference voltage) back to V_{CT} where the discharge time is measured precisely. The relationship of the charge and discharge values are shown below (see Figure 1).

$$V_{CX} = V_{CT} - \frac{V_I t_1}{R_X C_X} \qquad \text{Charge} \qquad (1)$$

$$V_{CT} = V_{CX} - \frac{V_{ref}\, t_2}{R_X C_X} \qquad \text{Discharge} \qquad (2)$$

Combining equations 1 and 2 results in:

$$\frac{V_I}{V_{ref}} = -\frac{t_2}{t_1} \qquad (3)$$

where:

V_{CT} = Comparator (offset) threshold voltage
V_{CX} = Voltage change across C_X during t_1 and during t_2 (equal in magnitude)
V_I = Average value of input voltage during t_1
t_1 = Time period over which unknown voltage is integrated
t_2 = Unknown time period over which a known reference voltage is integrated.

Equation (3) illustrates the major advantages of a dual-slope converter:

a. Accuracy is not dependent on absolute values of t_1 and t_2, but is dependent on their ratios. Long-term clock frequency variations will not affect the accuracy.
b. Offset values, V_{CT}, are not important.

The BCD counter in the digital processor (see Figure 2) and the control logic divide each measurement cycle into three phases. The BCD counter changes at a rate equal to one-half the oscillator frequency.

auto-zero phase

The cycle begins at the end of the integrate-reference phase when the digital processor applies low levels to inputs A and B of the analog processor. If the trigger input is at a high level, a free-running condition exists and continuous conversions are made. However, if the trigger input is low, the digital processor stops the counter at 20,000, entering a hold mode. In this mode, the processor samples the trigger input every 4000 oscillator pulses until a high level is detected. When this occurs, the counter is started again and is carried to completion at 30,000. The reference voltage is stored on reference capacitor C_{ref}, comparator offset voltage is stored on integration capacitor C_X, and the sum of the buffer and integrator offset voltages is stored on zero capacitor C_Z. During the auto-zero phase, the comparator output is characterized by an oscillation (limit cycle) of indeterminate waveform and frequency that is filtered and d-c shifted by the level shifter.

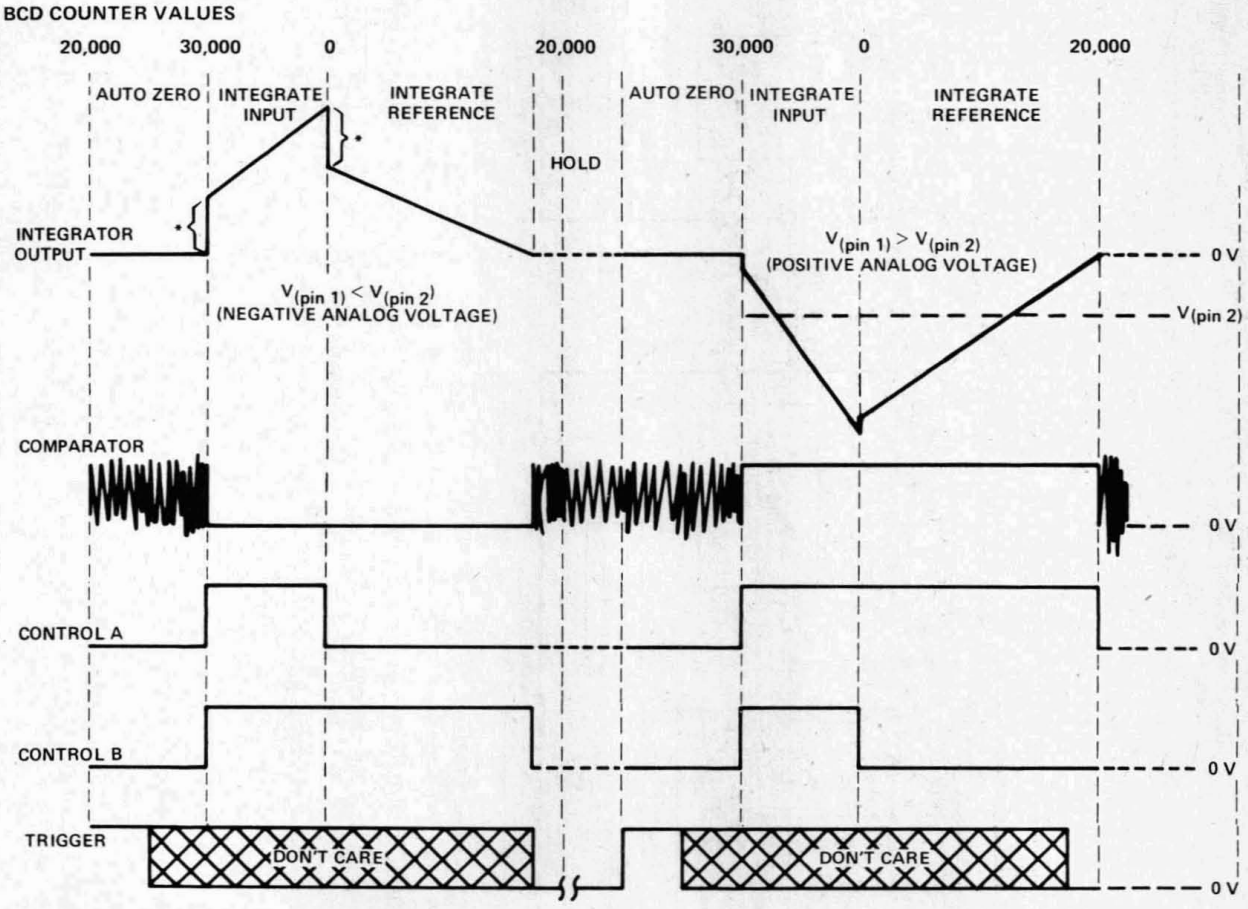
integrate-input phase

The auto-zero phase is completed at a BCD count of 30,000, and high levels are applied to both control inputs to initiate the integrate-input phase. The integrator charges C_X for a fixed time of 10,000 BCD counts at a rate determined by the input voltage. Note that during this phase, the analog inputs see only the high impedance of the noninverting operational amplifier input. Therefore, the integrator responds only to the difference between the analog input terminals, thus providing true differential inputs.

integrate-reference phase

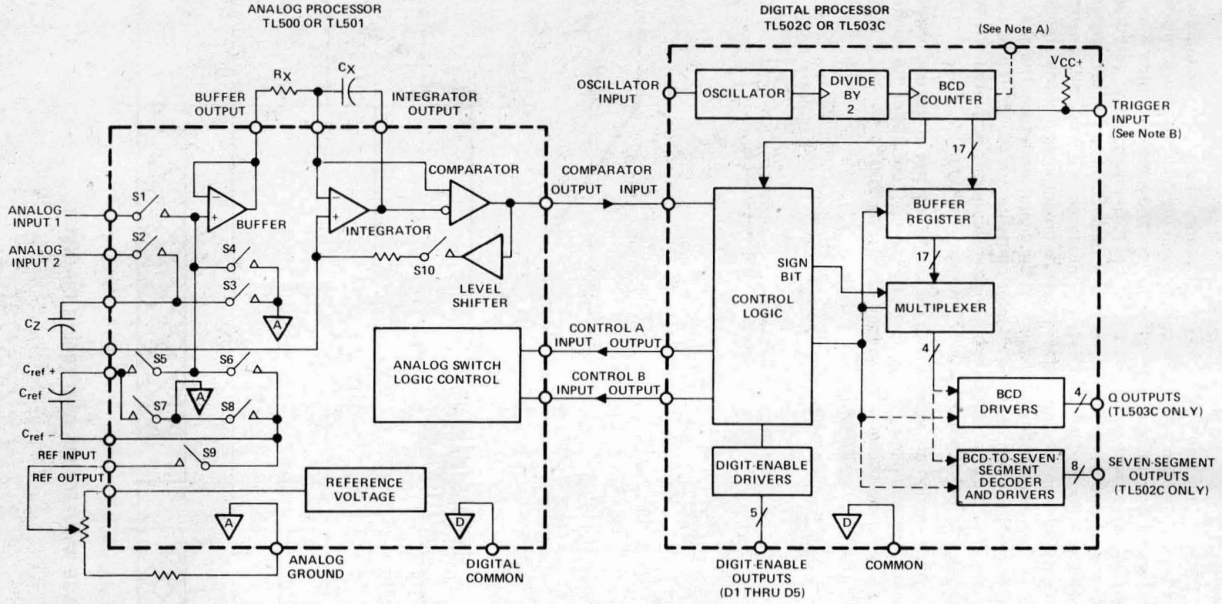
At a BCD count of 39,999 + 1 = 40,000 or 0, the integrate-input phase is terminated and the integrate-reference phase is begun by sampling the comparator output. If the comparator output is low corresponding to a negative average analog input voltage, the digital processor applies a low and a high to inputs A and B, respectively, to apply the reference voltage stored on C_{ref} to the buffer. If the comparator output is high corresponding to a positive input, inputs A and B are made high and low, respectively, and the negative of the stored reference voltage is applied to the buffer. In either case, the processor automatically selects the proper logic state to cause the integrator to ramp back toward zero at a rate proportional to the reference voltage. The time required to return to zero is measured by the counter in the digital processor. The phase is terminated when the integrator output crosses zero and the counter contents are transferred to the register, or when the BCD counter reaches 20,000 and the over-range indication is activated. When activated, the over-range indication blanks all but the most significant digit and sign.

Seventeen parallel bits (4-1/2 digits) of information are strobed into the buffer register at the end of the integration phase. Information for each digit is multiplexed out to the BCD outputs (TL503C) or the seven-segment drivers (TL502C) at a rate equal to the oscillator frequency divided by 200.



*This step is the voltage at pin 2 with respect to analog ground.

FIGURE 1. VOLTAGE WAVEFORMS AND TIMING DIAGRAM



NOTES: A. Pin 18 of the TL502C provides an output of f_{osc} (oscillator frequency) ÷ 20,000.
B. The trigger input assumes a high level if not externally connected.

FIGURE 2. BLOCK DIAGRAM OF BASIC ANALOG-TO-DIGITAL CONVERTER USING TL500 OR TL501 AND TL502C OR TL503C

MODE	ANALOG INPUT	COMPARATOR	CONTROLS A AND B	ANALOG SWITCHES CLOSED
Auto Zero	X	Oscillation	L L	S3, S4, S7, S9, S10
Hold†				
Integrate Input	Positive	H	H H	S1, S2
	Negative	L		
Integrate Reference	X	L‡	L H	S3, S6, S7
		H‡	H L	S3, S5, S8

H ≡ High, L ≡ low, X ≡ Irrelevant

† If the trigger input is low at the beginning of the auto-zero cycle, the system will enter the hold mode. A high level (or open circuit) will signal the digital processor to continue or resume normal operation.

‡ This is the state of the comparator output as determined by the polarity of the analog input during the integrate input phase.

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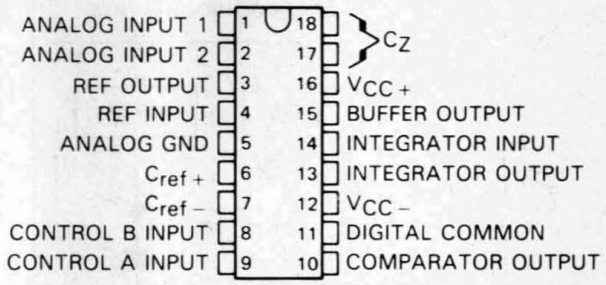
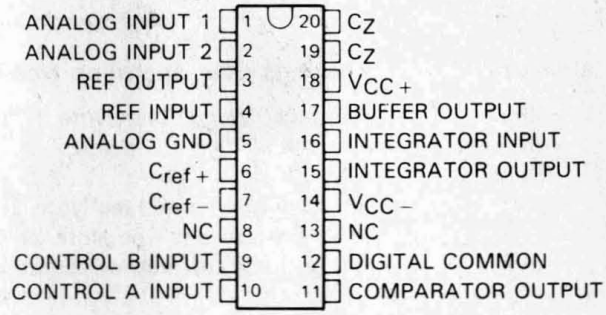
description of analog processors

The TL500 and TL501 analog processors are designed to automatically compensate for internal zero offsets, integrate a differential voltage at the analog inputs, integrate a voltage at the reference input in the opposite direction, and provide an indication of zero-voltage crossing. The external control mechanism may be a microcomputer and software routing, discrete logic, or a TL502C or TL503C controller. The TL500 and TL501 are designed primarily for simple, cost-effective, dual-slope analog-to-digital converters. Both devices feature true differential analog inputs, high input impedance, and an internal reference-voltage source. The TL500 provides 4-1/2-digit readout accuracy when used with a precision external reference voltage. The TL501 provides 100-ppm linearity error and 3-1/2-digit accuracy capability. These devices are manufactured using TI's advanced technology to produce JFET, MOSFET, and bipolar devices on the same chip. The TL500C and TL501C are characterized for operation over the temperature range of 0°C to 70°C. The TL500I and TL501I are characterized for operation from −40°C to 85°C.

J PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)

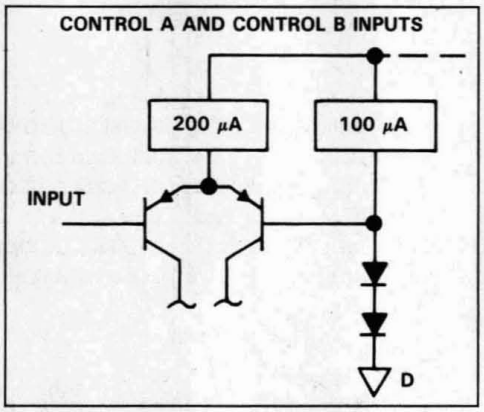


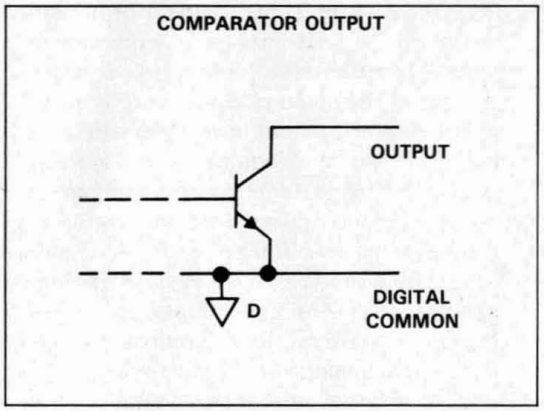
NC – No internal connection

AVAILABLE OPTIONS

T_A	LINEARITY ERROR	PACKAGE	
		CERAMIC DIP (J)	WIDE-BODY SO (DW)
0°C to 70°C	0.005% FS	TL500CJ	TL500CDW
	0.05% FS	TL501CJ	TL501CDW
−40°C to 85°C	0.005% FS	TL500IJ	TL500IDW
	0.05% FS	TL501IJ	TL501IDW

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Positive supply voltage, V_{CC+} (see Note 1) . . . . . +18 V
Negative supply voltage, V_{CC-} . . . . . −18 V
Input voltage, V_I . . . . . $\pm V_{CC}$
Comparator output voltage range (see Note 2) . . . . . 0 V to V_{CC+}
Comparator output sink current (see Note 2) . . . . . 20 mA
Buffer, reference, or integrator output source current (see Note 2) . . . . . 10 mA
Total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: TL500I, TL501I . . . . . −40 to 85°C
TL500C, TL501C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTES: 1. Voltage values, except differential voltages, are with respect to the analog ground common pin tied together.
2. Buffer, integrator, and comparator outputs are not short-circuit protected.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1125 mW	9 mW/°C	720 mW	585 mW
J	1025 mW	8.2 mW/°C	656 mW	533 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Positive supply voltage, V_{CC+}		7	12	15	V
Negative supply voltage, V_{CC-}		−9	−12	−15	V
Reference input voltage, $V_{ref(I)}$		0.1		5	V
Analog input voltage, V_I				±5	V
Differential analog input voltage, V_{ID}				10	V
High-level input voltage, V_{IH}	Control inputs	2			V
Low-level input voltage, V_{IL}	Control inputs			0.8	V
Peak positive integrator output voltage, V_{OM+}		+9			V
Peak negative integrator output voltage, V_{OM-}		−5			V
Full scale input voltage				2 V_{ref}	
Autozero and reference capacitors, C_Z and C_{ref}		0.2			μF
Integrator capacitor, C_X		0.2			μF
Integrator resistor, R_X		15		100	kΩ
Integrator time constant, R_XC_X		See Note 3			
Free-air operating temperature, T_A	TL500I, TL501I	−40		85	°C
	TL500C, TL501C	0		70	
Maximum conversion rate with TL502C or TL503C			3	12.5	conv/sec

system electrical characteristics at $V_{CC\pm}$ = ±12 V, V_{ref} = 1.000 ± 0.03 mV, T_A = 25°C (unless otherwise noted) (see Figure 3)

PARAMETER	TEST CONDITIONS	TL501			TL500			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Zero error			50	300		10	30	μV
Linearity error relative to full scale	V_I = 2 V to 2 V		0.005	0.05		0.001	0.005	%FS
Full scale temperature coefficient	T_A = full range		6			6		ppm/°C
Temperature coefficient of zero error			4			1		μV/°C
Rollover error†			200	500		30	100	μV
Equivalent peak-to-peak input noise voltage			20			20		μV
Analog input resistance	Pin 1 or 2		10^9			10^9		Ω
Common-mode rejection ratio	V_{IC} = −1 V to +1 V		86			90		dB
Current into analog input	V_I = ±5 V		50			50		pA
Supply voltage rejection ratio			90			90		dB

†Rollover error is the voltage difference between the conversion results of the full-scale positive 2 V and the full-scale negative 2 V.

NOTE 3. The minimum integrator time constant may be found by use of the following formula:

$$\text{Minimum } R_XC_X = \frac{V_{ID}\ (\text{full scale})\ t_1}{|V_{OM-}| - V_I(\text{pin 2})}$$

where

V_{ID} = voltage at pin with respect to pin 2
V_I(pin 2) = voltage at pin 2 with respect to analog ground
t_1 = input integration time seconds

electrical characteristics at $V_{CC\pm}$ = ±12 V, V_{ref} = 1 V, T_A = 25°C (see Figure 3)

integrator and buffer operational amplifiers

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage			15		mV
I_{IB}	Input bias current			50		pA
V_{OM+}	Positive output voltage swing		9	11		V
V_{OM-}	Negative output voltage swing		−5	−7		V
A_{VD}	Voltage amplification			110		dB
B_1	Unity-gain bandwidth			3		MHz
CMRR	Common mode rejection	V_{IC} = −1 V to +1 V		100		dB
SR	Output slew rate			5		V/μs

comparator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage			15		mV
I_{IB}	Input bias current			50		pA
A_{VD}	Voltage amplification			100		dB
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA		200	400	mV
I_{OH}	High-level output current	V_{OH} = 3 V		5	20	nA

voltage reference output

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ref(0)}$	Reference voltage		1.12	1.22	1.32	V
αV_{ref}	Reference-voltage temperature coefficient	T_A = full range		80		ppm/°C
r_o	Reference output resistance			3		Ω

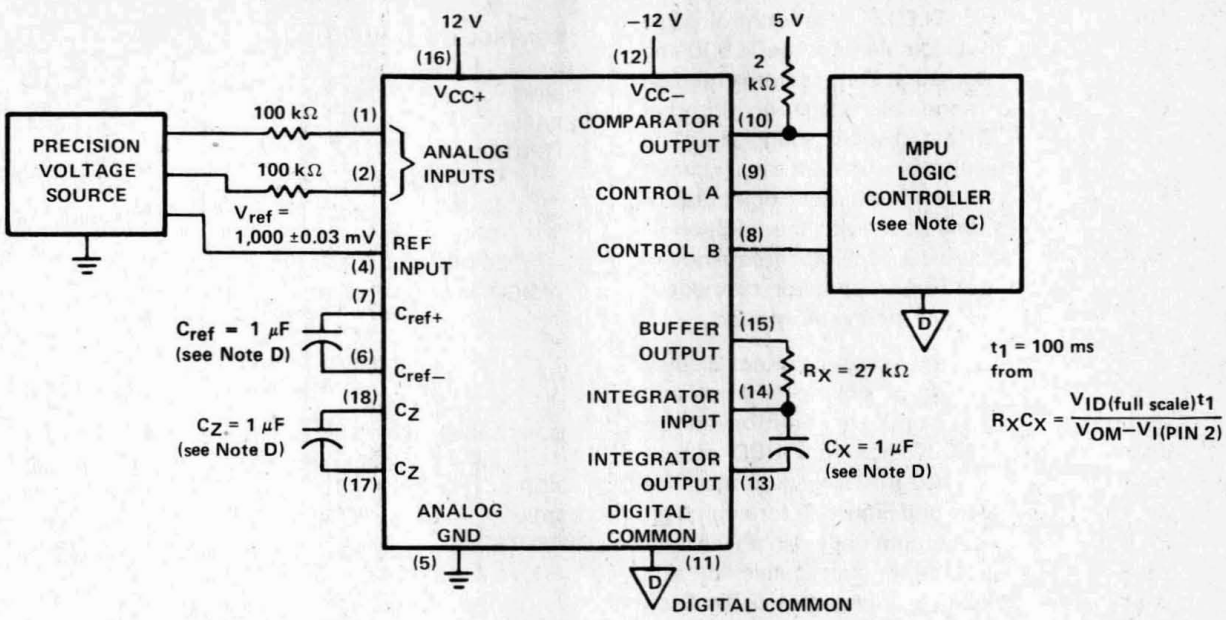
logic control section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level input current	V_{IH} = 2 V		.1	10	μA
I_{IL}	Low-level input current	V_{IL} = 0.8 V		−40	−300	μA

total device

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC+}	Positive supply current			15	20	mA
I_{CC-}	Negative supply current			12	18	mA

PARAMETER MEASUREMENT INFORMATION



NOTES: C. Tests are started approximately 5 seconds after power-on.
D. Capacitors used are TRW's X363UW polypropylene or equivalent for C_X, C_{ref}, and C_Z; however for C_{ref} and C_Z film-dielectric capacitors may be substituted.

FIGURE 3. TEST CIRCUIT CONFIGURATION

external-component selection guide

The autozero capacitor C_Z and reference capacitor C_{ref} should be within the recommended range of operating conditions and should have low-leakage characteristics. Most film-dielectric capacitors and some tantalum capacitors provide acceptable results. Ceramic and aluminum capacitors are not recommended because of their relatively high-leakage characteristics.

The integrator capacitor C_X should also be within the recommended range and must have good voltage linearity and low dielectric absorption. A polypropylene-dielectric capacitor similar to TRW's X363UW is recommended for 4-1/2-digit accuracy. For 3-1/2-digit applications, polyester, polycarbonate, and other film dielectrics are usually suitable. Ceramic and electrolytic capacitors are not recommended.

Stray coupling from the comparator output to any analog pin (in order of importance 17, 18, 14, 7, 6, 13, 1, 2, 15) must be minimized to avoid oscillations. In addition, all power supply pins should be bypassed at the package, for example, by a 0.01-μF ceramic capacitor.

Analog and digital common are internally isolated and may be at different potentials. Digital common can be within 4 V of positive or negative supply with the logic decode still functioning properly.

The time constant R_XC_X should be kept as near the minimum value as possible and is given by the formula:

$$\text{Minimum } R_XC_X = \frac{V_{ID}\ (\text{full scale})\ t_1}{|V_{OM-}| - V_{I(pin2)}}$$

where:

V_{ID}(full scale) = Voltage on pin 1 with respect to pin 2
t_1 = Input integration time in seconds
$V_{I(pin2)}$ = Voltage on pin 2 with respect to analog ground.

description of digital processors

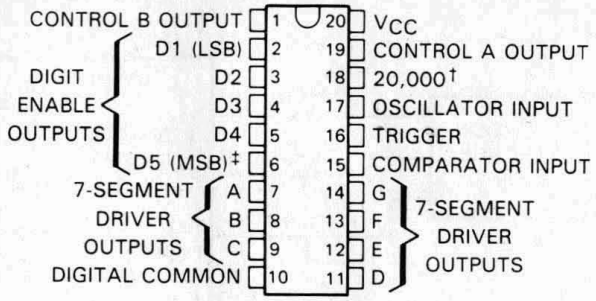
The TL502C and TL503C are control logic devices designed to complement the TL500 and TL501 analog processors. They feature interdigit blanking, over-range blanking, an internal oscillator, and a fast display scan rate. The internal-oscillator input is a Schmitt trigger circuit that can be driven by an external clock pulse or provide its own time base with the addition of a capacitor. The typical oscillator frequency is 120 kHz with a 470-pF capacitor connected between the oscillator input and ground.

The TL502C provides seven-segment-display output drivers capable of sinking 100 mA and compatible with popular common-anode displays. The TL503C has four BCD output drivers capable of 100-mA sink currents. The code (see next page and Figure 4) for each digit is multiplexed to the output drivers in phase with a pulse on the appropriate digit-enable line at a digit rate equal to f_{osc}, divided by 200. Each digit-enable output is capable of sinking 20-mA.

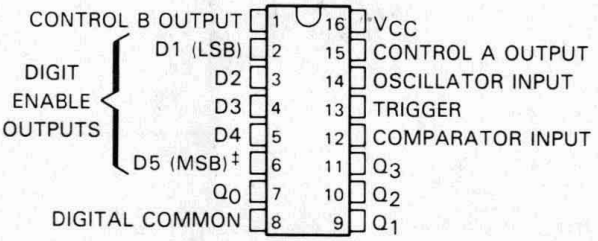
The comparator input of each device, in addition to monitoring the output of the zero-crossing detector in the analog processor, may be used in the display test mode to check for wiring and display faults. A high logic level (2 to 6.5 V) at the trigger input with the comparator input at or below 6.5 V starts the integrate-input phase. Voltage levels equal to or greater than 7.9 V on both the trigger and comparator inputs clear the system and set the BCD counter to 20,000. When normal operation resumes, the conversion cycle is restarted at the auto zero phase.

These devices are manufactured using I^2L and bipolar techniques. The TL502C and TL503C are characterized for operation from 0°C to 70°C.

TL502C . . . N PACKAGE
(TOP VIEW)



TL503C . . . N PACKAGE
(TOP VIEW)



†Pin 18 of TL502C provides an output of f_{osc} (oscillator frequency) ÷ 20,000.
‡D5, the most significant bit, is also the sign bit.

TABLE OF SPECIAL FUNCTIONS
V_{CC} = 5 V ±10%

TRIGGER INPUT	COMPARATOR INPUT	FUNCTION
$V_I \leq 0.8$ V	$V_I \leq 6.5$ V	Hold at auto-zero cycle after completion of conversion
2 V $\leq V_I \leq$ 6.5 V	$V_I \leq 6.5$ V	Normal operation (continuous conversion)
$V_I \leq 6.5$ V	$V_I \geq 7.9$ V	Display Test: All BCD outputs high
$V_I \geq 7.9$ V	$V_I \leq 6.5$ V	Internal Test
Both inputs to go $V_I \geq 7.9$ V simultaneously		System clear: Sets BCD counter to 20,000. When normal operation is resumed, cycle begins with Auto Zero.

DIGIT 5 (MOST SIGNIFICANT DIGIT) CHARACTER CODES

CHARACTER	TL502C SEVEN-SEGMENT LINES							TL503C BCD OUTPUT LINES			
	A	B	C	D	E	F	G	Q3 8	Q2 4	Q1 2	Q0 1
+	H	H	H	H	L	L	L	H	L	H	L
+1	H	L	L	H	L	L	L	H	H	H	L
−	L	H	H	L	H	H	L	H	L	H	H
−1	L	L	L	L	H	H	L	H	H	H	H

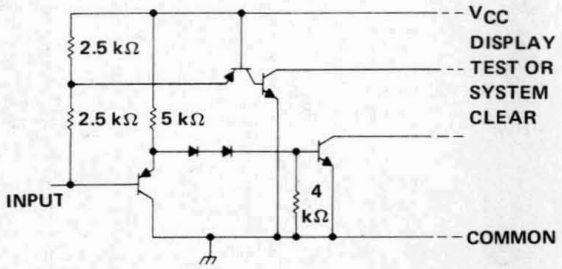
DIGITS 1 THRU 4 NUMERIC CODE (See Figure 4)

NUMBER	TL502C SEVEN-SEGMENT LINES							TL503C BCD OUTPUT LINES			
	A	B	C	D	E	F	G	Q3 8	Q2 4	Q1 2	Q0 1
0	L	L	L	L	L	L	H	L	L	L	L
1	H	L	L	H	H	H	H	L	L	L	H
2	L	L	H	L	L	H	L	L	L	H	L
3	L	L	L	L	H	H	L	L	L	H	H
4	H	L	L	H	H	L	L	L	H	L	L
5	L	H	L	L	H	L	L	L	H	L	H
6	L	H	L	L	L	L	L	L	H	H	L
7	L	L	L	H	H	H	H	L	H	H	H
8	L	L	L	L	L	L	L	H	L	L	L
9	L	L	L	L	H	L	L	H	L	L	H

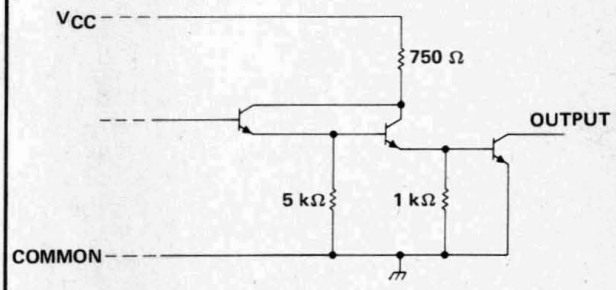
H = high level, L = low level

schematics of inputs and outputs

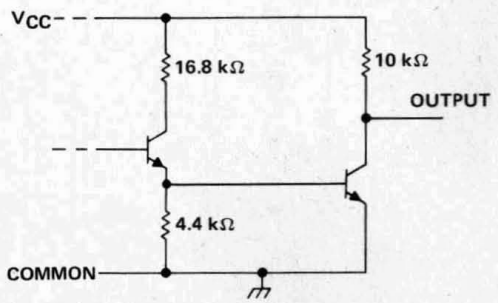
COMPARATOR AND TRIGGER INPUT



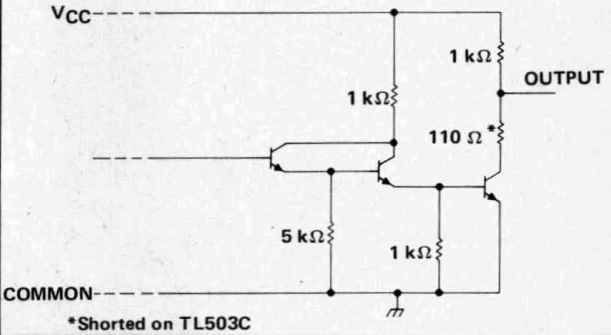
SEGMENT DRIVERS—TL502C
BCD DRIVERS—TL503C



CONTROL A AND B OUTPUTS



DIGIT-ENABLE OUTPUTS



*Shorted on TL503C

absolute maximum ratings

Supply voltage, V_{CC} (see Note 4)		7	V
Input voltage, V_I	Oscillator	5.5	V
	Comparator or Trigger	9	
Output current	BCD or Segment drivers	120	mA
	Digit-enable outputs	40	
	Pin 18 (TL502C only)	20	
Total power dissipation at (or below) 30°C free-air temperature (see Note 5)		1100	mW
Operating free-air temperature range		0 to 70	°C
Storage temperature range		−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C

NOTES: 4. Voltage values are with respect to the network ground terminal.
5. For operation above 30°C free-air temperature, derate linearly to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level input voltage, V_{IH}	Comparator and trigger inputs	2			V
Low-level input voltage, V_{IL}	Comparator and trigger inputs			0.8	V
Operating free-air temperature		0		70	°C

electrical characteristics at 25°C free-air temperature

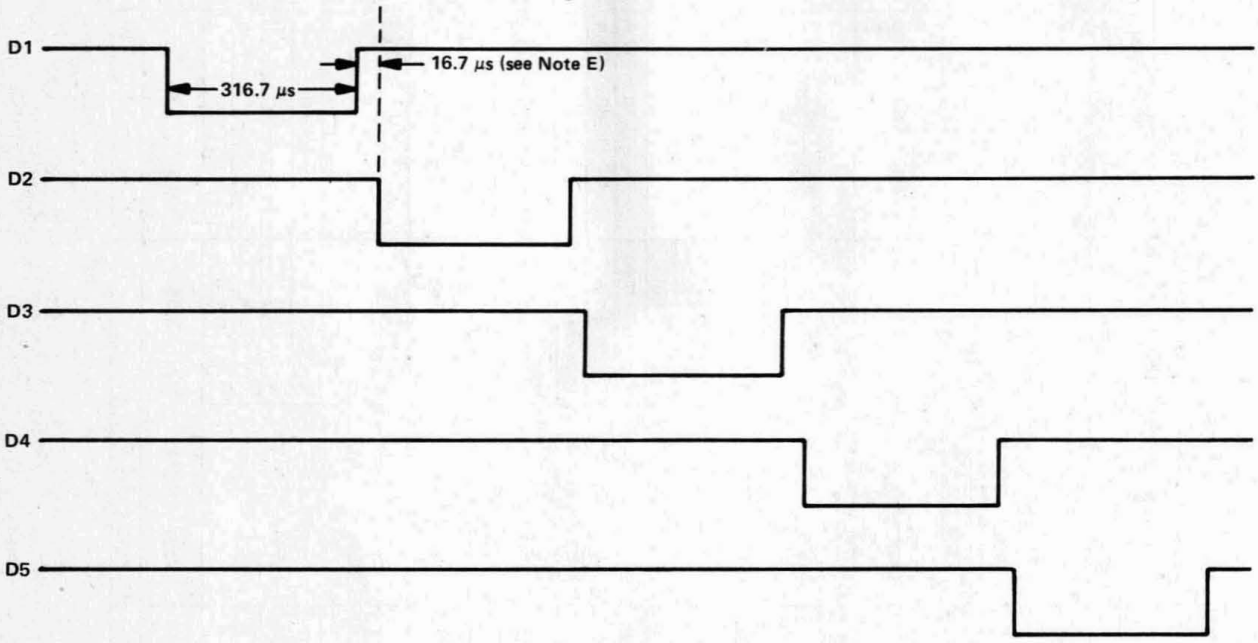
PARAMETER		TERMINAL	TEST CONDITIONS		TL502C			TL503C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IK}	Input clamp voltage	All inputs	V_{CC} = 4.5 V,	I_I = −12 mA		−0.8	−1.5		−0.8	−1.5	V
V_{T+}	Positive-going input threshold voltage	Oscillator	V_{CC} = 5 V			1.5			1.5		V
V_{T-}	Negative-going input threshold voltage	Oscillator	V_{CC} = 5 V			0.9			0.9		V
$V_{T+} - V_{T-}$	Hysteresis	Oscillator	V_{CC} = 5 V		0.4	0.6	0.8	0.4	0.6	0.8	
I_{T+}	Input current at positive-going input threshold voltage	Oscillator	V_{CC} = 5 V		−40	−94	−170	−40	−94	−170	μA
I_{T-}	Input current at negative-going input threshold voltage	Oscillator	V_{CC} = 5 V		40	117	170	40	117	170	μA
V_{OH}	High-level output voltage	Digit enable	V_{CC} = 4.5 V,	I_{OH} = 0	4.15	4.4		4.15	4.4		V
		Pin 18 (TL502C only)			4.25	4.4					
		Control A and B			4.25	4.4		4.25	4.4		
V_{OL}	Low-level output voltage	Digit enable	V_{CC} = 4.5 V	I_{OL} = 20 mA					0.2	0.5	V
		Pin 18 (TL502C only)		I_{OL} = 10 mA		0.15	0.4				
		Control A and B		I_{OL} = 2 mA		0.088	0.4		0.088	0.4	
		Segment drivers		I_{OL} = 100 mA		0.17	0.3				
		BCD drivers		I_{OL} = 100 mA					0.17	0.3	
I_I	Input current	Comparator, Trigger	V_{CC} = 5.5 V,	V_I = 5.5 V		65	100		65	100	μA
		Oscillator					1			1	mA
I_{IH}	High-level input current	Comparator, Trigger	V_{CC} = 5.5 V,	V_I = 2.4 V		−0.6	−1		−0.6	−1	mA
		Oscillator					0.5			0.5	
I_{IL}	Low-level input voltage	Oscillator	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.1	−0.17		−0.1	−0.17	mA
		Comparator, Trigger				−1	−1.6		−1	−1.6	
I_{OH}	High-level output current (Output transistor off)	Digit enable	V_{CC} = 4.5 V	V_O = 0.5 V,	−2.5	−4		−2.5	−4		mA
		Pin 18 (TL502C only)		V_O = 0.5 V	−0.5	−0.9					
		Control A and B		V_O = 0.5 V	−0.25	−0.4		−0.25	−0.4		
		Segment drivers		V_O = 5.5 V			0.25				
		BCD drivers		V_O = 5.5 V						0.25	
I_{OL}	Low-level output current (Output transistor on)	Digit enable	V_{CC} = 4.5 V,	V_O = 3.55 V	18	23					mA
I_{CC}	Supply current	V_{CC}	V_{CC} = 5.5 V			73	110		73	110	mA

special functions† operating characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_I	Input current into comparator or trigger inputs	V_{CC} = 5.5 V, V_I = 8.55 V		1.2	1.8	mA
		V_{CC} = 5.5 V, V_I = 6.25 V			0.5	mA

†The comparator and trigger inputs may be used in the normal mode or to perform special functions. See the Table of Special Functions.

TYPICAL APPLICATION DATA



NOTE E: The BCD or seven-segment driver outputs are present for a particular digit slightly before the falling edge of that digit enable.

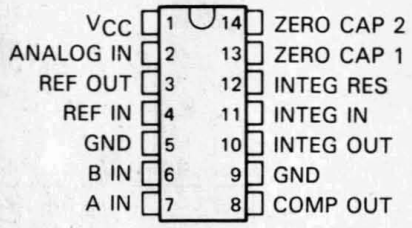
FIGURE 4. TL502C, TL503C DIGIT TIMING WITH 120-kHz CLOCK SIGNAL AT OSCILLATOR INPUT

TL505C
ANALOG-TO-DIGITAL CONVERTER

D2366, OCTOBER 1977 – REVISED FEBRUARY 1989

- 3-Digit Accuracy (0.1%)
- 10-Bit Resolution
- Automatic Zero
- Internal Reference Voltage
- Single-Supply Operation
- High-Impedance MOS Input
- Designed for Use with TMS1000 Type Microprocessors for Cost-Effective High-Volume Applications
- BI-MOS Technology
- Only 40 mW Typical Power Consumption

N PACKAGE
(TOP VIEW)



Caution. This device has limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

description

The TL505C is an analog-to-digital converter building block designed for use with TMS1000 type microprocessors. It contains the analog elements (operational amplifier, comparator, voltage reference, analog switches, and switch drivers) necessary for a unipolar automatic-zeroing dual-slope converter. The logic for the dual-slope conversion can be performed by the associated MPU as a software routine or can be implemented with other components, such as the TL502 logic-control device.

The high-impedance MOS inputs permit the use of less expensive, lower value capacitors for the integration and offset capacitors and permit conversion speeds from 20 per second to 0.05 per second.

The TL505C is a product of TI's BI-MOS process, which incorporates bipolar and MOSFET transistors on the same monolithic circuit. The TL505C is characterized for operation from 0°C to 70°C.

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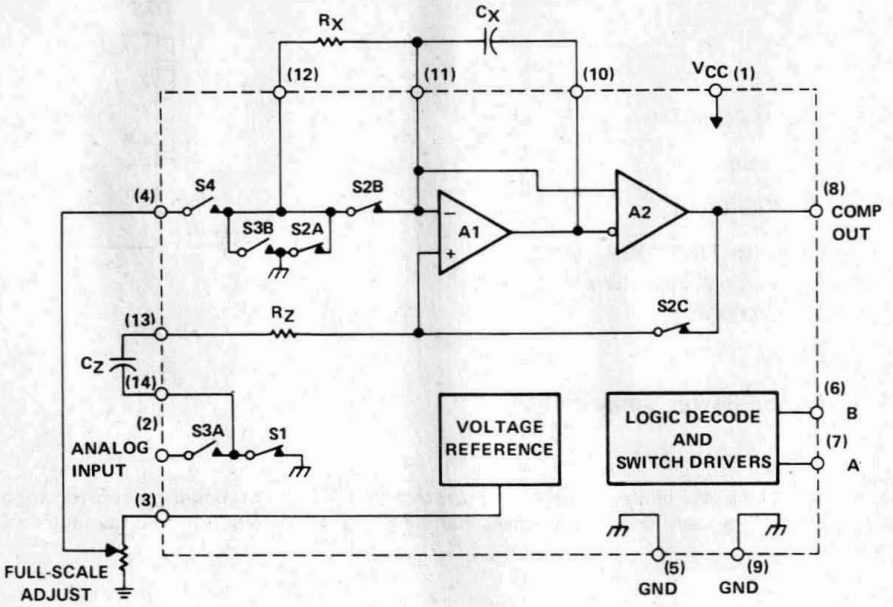
functional block diagram



NOTE: Analog and digital GND are internally connected together.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 18 V
Input voltage, pins 2, 4, 6, and 7 . . . . . V_{CC}
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to the two ground terminals connected together.
2. For operation above 25°C free-air temperature, derate linearly to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	7	9	15	V
Analog input voltage, V_I	0		4	V
Reference input voltage, $V_{ref(I)}$	0.5		3	V
High-level input voltage at A or B, V_{IH}	3.6		$V_{CC}+1$	V
Low-level input voltage at A or B, V_{IL}	0.2		1.8	V
Integrator capacitor, C_X	See "component selection"			
Integrator resistor, R_X	0.5		2	MΩ
Integration time, t_1	16.6		500	ms
Operating free-air temperature, T_A	0		70	°C

electrical characteristics, V_{CC} = 9 V, $V_{ref(I)}$ = 1 V, T_A = 25°C, connected as shown in Figure 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage at pin 8	I_{OH} = 0	7.5	8.5		V
I_{OH}	High-level output current at pin 8	V_{OH} = 7.5 V		−100		μA
V_{OL}	Low-level output voltage at pin 8	I_{OL} = 1.6 mA		200	400	mV
V_{OM}	Maximum peak output voltage swing at integrator output	$R_X \geq 500\ k\Omega$	$V_{CC}-2$	$V_{CC}-1$		V
$V_{ref(O)}$	Reference output voltage	I_{ref} = −100 μA	1.15	1.22	1.35	V
αV_{ref}	Temperature coefficient of reference output voltage	T_A = 0°C to 70°C		±100		ppm/°C
I_{IH}	High-level input current into A or B	V_I = 9 V		1	10	μA
I_{IL}	Low-level input current into A or B	V_I = 1 V		10	200	μA
I_I	Current into analog input	V_I = 0 to 4 V, A input at 0 V		±10	±200	pA
I_{IB}	Total integrator input bias current			±10		pA
I_{CC}	Supply current	No load		4.5	8	mA

system electrical characteristics, V_{CC} = 9 V, $V_{ref(I)}$ = 1 V, T_A = 25°C, connected as shown in Figure 1 (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Zero error	V_I = 0		0.1	0.4	mV
Linearity error	V_I = 0 to 4 V		0.02	0.1	%FS
Ratiometric reading	$V_I = V_{ref(I)} \approx 1$ V	0.998	1.000	1.002	
Temperature coefficient of ratiometric reading	$V_{ref(I)}$ constant and ≈ 1 V, T_A = 0°C to 70°C		±10		ppm/°C

DEFINITION OF TERMS

Zero Error

The intercept (b) of the anolog-to-digital converter system transfer function y = mx + b, where y is the digital output, x is the analog input, and m is the slope of the transfer function, which is approximated by the ratiometric reading.

Linearity Error

The maximum magnitude of the deviation from a straight line between the end points of the transfer function.

Ratiometric Reading

The ratio of negative integration time (t_2) to positive time (t_1).

PRINCIPLES OF OPERATION

A block diagram of an MPU system using the TL505C is shown in Figure 1. The TL505C operates in a modified positive-integration, three-step, dual-slope conversion mode. The A/D converter waveforms during the conversion process are illustrated in Figure 2.

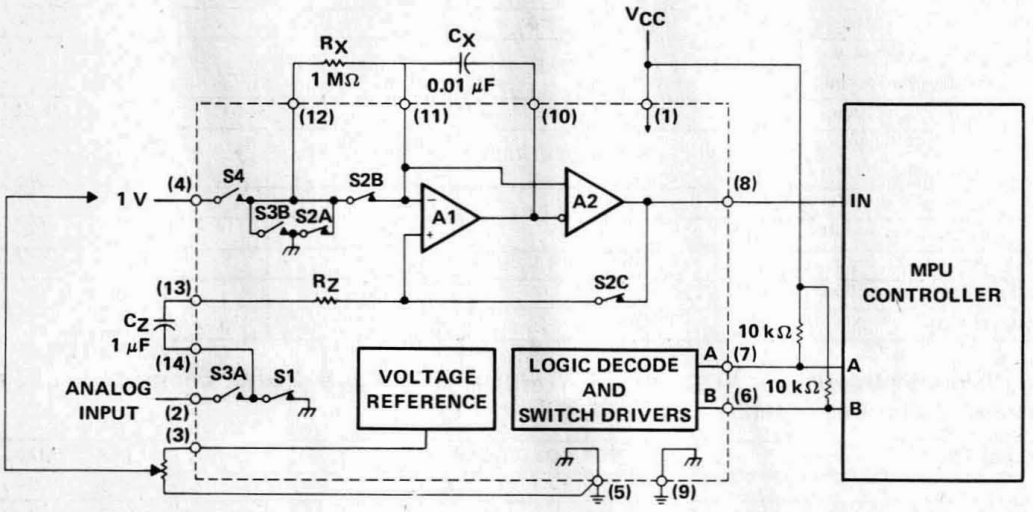
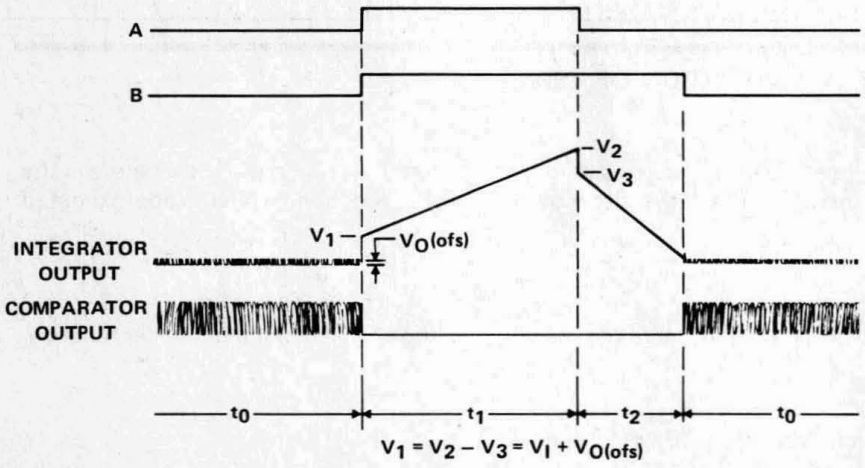


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM OF TL505C INTERFACE WITH A MICROPROCESSOR SYSTEM



FUNCTION TABLE

CONTROLS A	CONTROLS B	ANALOG SWITCHES CLOSED
L	L	S1, S2
H	H	S3
L	H	S1, S4

H = V_{IH}, L = V_{IL}

FIGURE 2. CONVERSION PROCESS TIMING DIAGRAMS

PRINCIPLES OF OPERATION (Continued)

The first step of the conversion process is the auto-zero period t_0. By the end of this period, the integrator offset is stored in the autozero capacitor, and the offset of the comparator is stored in the integrator capacitor. To achieve this end, the MPU takes the A and B inputs low, which closes S1 and S2. The output of the comparator is connected to the input of the integrator through the low-pass filter consisting of R_Z and C_Z. The closed loop of A1 and A2 seeks a null condition in which the offsets of the integrator and comparator are stored in C_Z and C_X, respectively. This null condition is characterized by a high-frequency oscillation at the output of the comparator. The purpose of S2B is to shorten the amount of time required to reach the null condition.

At the conclusion of t_0, the MPU takes the A and B inputs both high, which closes S3 and opens all other switches. The input signal V_I is applied to the noninverting input of A1 through C_Z. V_I is then positively integrated by A1. Since the offset of A1 is stored in C_Z, the change in voltage across C_X is due to only the input voltage. Since the input is integrated in a positive integration during t_1, the output of A1 will be the sum of the input voltage, the integral of the input voltage, and the comparator offset, as shown in Figure 2. The change in voltage across capacitor C_X (V_{CX}) during t_1 is given by

$$\Delta V_{CX(1)} = \frac{V_I t_1}{R_1 C_X} \tag{1}$$

where $R_1 = R_X + R_{S3B}$ and R_{S3B} is the resistance of switch S3B.

At the end of t_1, the MPU takes the A input low and the B input high, which closes S1 and S4 and opens all other switches. In this state, the reference is integrated by A1 in a negative sense until the integrator output reaches the comparator threshold. At this point, the comparator output goes high. This change in state is sensed by the MPU, which terminates t_2 by again taking the A and B inputs both low. During t_2, the change in voltage across C_X is given by

$$\Delta V_{CX(2)} = \frac{V_{ref} t_2}{R_2 C_X} \tag{2}$$

where $R_2 = R_X + R_{S4} + R_{ref}$ and R_{ref} is the equivalent resistance of the reference divider.

Since $\Delta V_{CX1} = -\Delta V_{CX2}$, equations (1) and (2) can be combined to give

$$V_I = V_{ref} \frac{R_1 \cdot t_2}{R_2 \cdot t_1} \tag{3}$$

This equation is a variation on the ideal dual-slope equation, which is

$$V_I = V_{ref} \frac{t_2}{t_1} \tag{4}$$

Ideally then, the ratio of R_1/R_2 would be exactly equal to one. In a typical TL505C system where $R_X = 1\ M\Omega$, the scaling error introduced by the difference in R_1 and R_2 is so small that it can be neglected, and equation (3) reduces to (4).

PRINCIPLES OF OPERATION (Continued)

component selection

The autozero capacitor C_Z should be within the recommended range of operating conditions and should have low leakage characteristics. Most film-dielectric capacitors and some tantalum capacitors provide acceptable results. Ceramic and aluminum capacitors are not recommended because of their relatively high leakage characteristics.

The integrator capacitor C_X should also be within the recommended range and must have good voltage linearity and low dielectric absorption. For 10-bit applications, polyster, polycarbonate, and other film dielectrics are usually suitable. If greater precision or stability is required, a polypropylene-dielectric capacitor similar to TRW's X363UW might be appropriate.

Stray coupling from the comparator output to any analog pin (in order of importance, 13, 11, 10, 2, 4) must be minimized to avoid oscillations. In addition, all power supply pins should be bypassed at the package, for example, by a 0.01-μF ceramic capacitor.

The time constant R_XC_X should be kept as near the minimum value as possible and is given by the formula:

$$\text{Minimum } R_XC_X = \frac{V_{I(max)}\, t_1}{(V_{CC} - 2\text{ V} - V_{I(max)})}$$

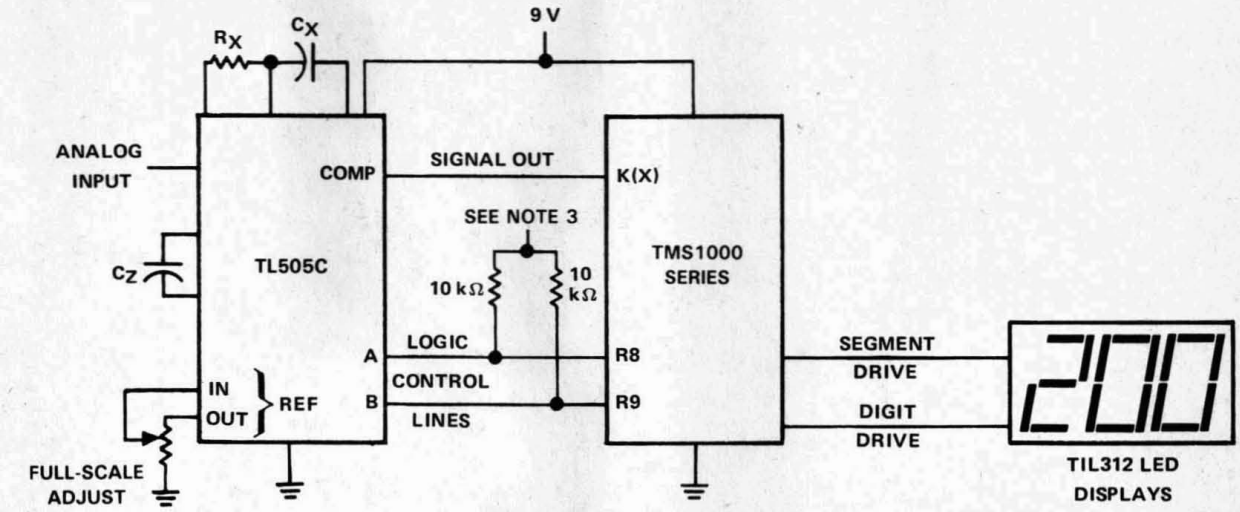
where:

t_1 = Input integration time in seconds,

$V_{I(max)}$ = the maximum value of the analog input voltage,

$V_{CC} - 2$ V = the maximum voltage swing of the integrator input.

TYPICAL APPLICATION DATA



NOTE 3: Connect to either 9 V or 0 V depending on which device in the TMS1000 series is used and how it is programmed.

FIGURE 3. TL505C IN CONJUNCTION WITH A TMS1000 SERIES MICROPROCESSOR FOR A 3-DIGITAL PANEL METER APPLICATION

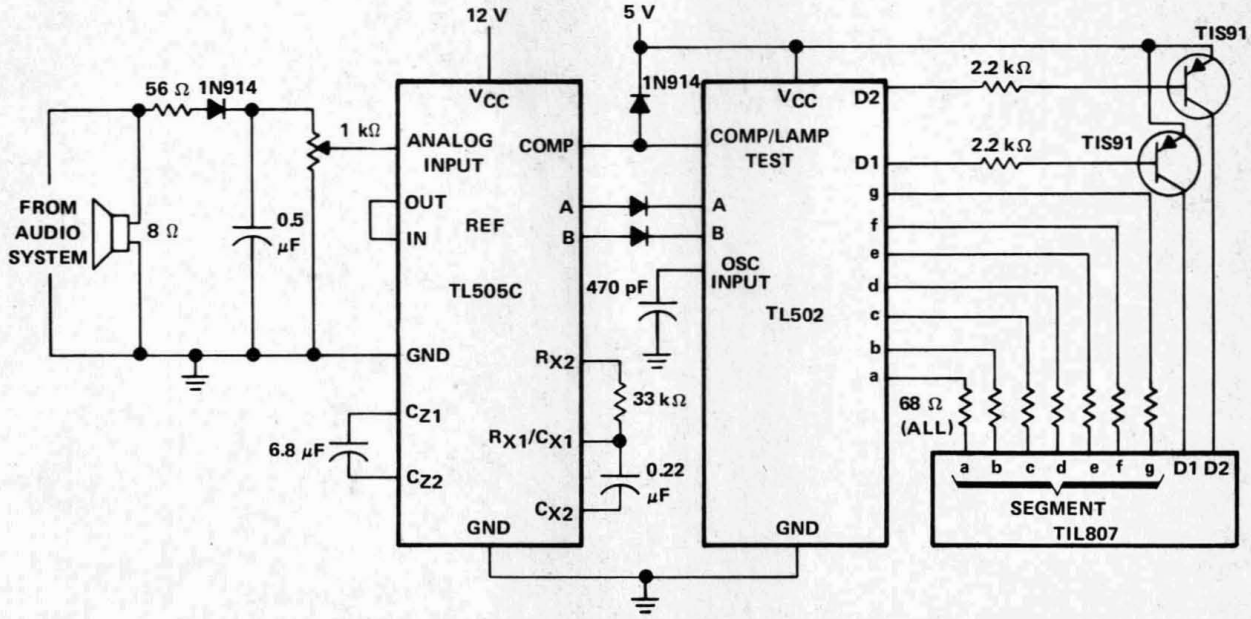
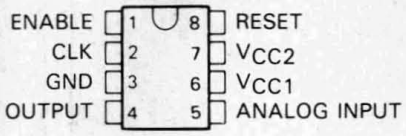


FIGURE 4. AUDIO PEAK POWER METER

D2503, OCTOBER 1979—REVISED OCTOBER 1988

- **Low Cost**
- **7-Bit Resolution**
- **Monotonicity Over Entire A/D Conversion Range**
- **Ratiometric Conversion**
- **Conversion Speed . . . Approximately 1 ms**
- **Single-Supply Operation . . . Either Unregulated 8-V to 18-V (V_{CC2} Input), or Regulated 3.5-V to 6-V (V_{CC1} Input)**
- **I^2L Technology**
- **Power Consumption at 5 V . . . 25 mW Typ**
- **Regulated 5.5 V Output (≤ 1 mA)**

P PACKAGE
(TOP VIEW)



FUNCTION TABLE

ANALOG INPUT CONDITION	ENABLE	OUTPUT
X	L†	H
$V_I < 200$ mV	H	L
$V_{ramp} > V_I > 200$ mV	H	H
$V_I > V_{ramp}$	H	L

†Low level on enable also inhibits the reset function.
H = high level, L = low level, X = irrelevant

A high level on the reset pin clears the counter to zero, which sets the internal ramp to 0.75 V_{CC}. Internal pull-down resistors keep the reset and enable pins low when not connected.

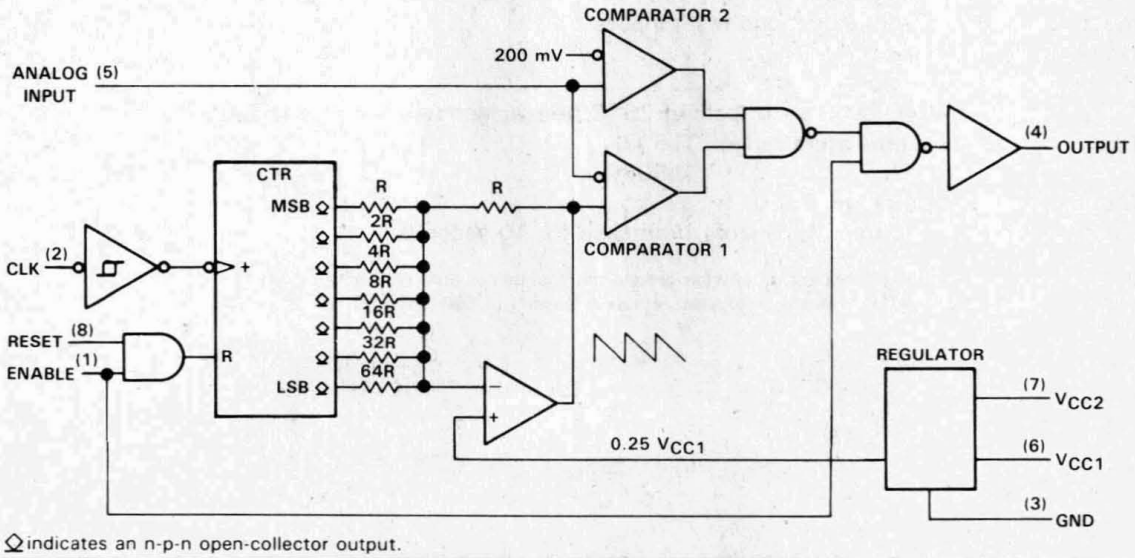
description

The TL507 is a low-cost single-slope analog-to-digital converter designed to convert analog input voltages between 0.25 V_{CC1} and 0.75 V_{CC1} into a pulse-width-modulated output code. The device contains a 7-bit synchronous counter, a binary weighted resistor ladder network, an operational amplifier, two comparators, a buffer amplifier, an internal regulator, and necessary logic circuitry. Integrated-injection logic (I^2L) technology makes it possible to offer this complex circuit at low cost in a small dual-in-line 8-pin package.

In continuous operation, conversion speeds of up to 1000 conversions per second are possible. The TL507 requires external signals for clock, reset, and enable. Versatility and simplicity of operation, coupled with low cost, makes this converter especially useful for a wide variety of applications.

The TL507I is characterized for operation from −40°C to 85°C, and the TL507C is characterized for operation from 0°C to 70°C.

functional block diagram (positive logic)



◇indicates an n-p-n open-collector output.

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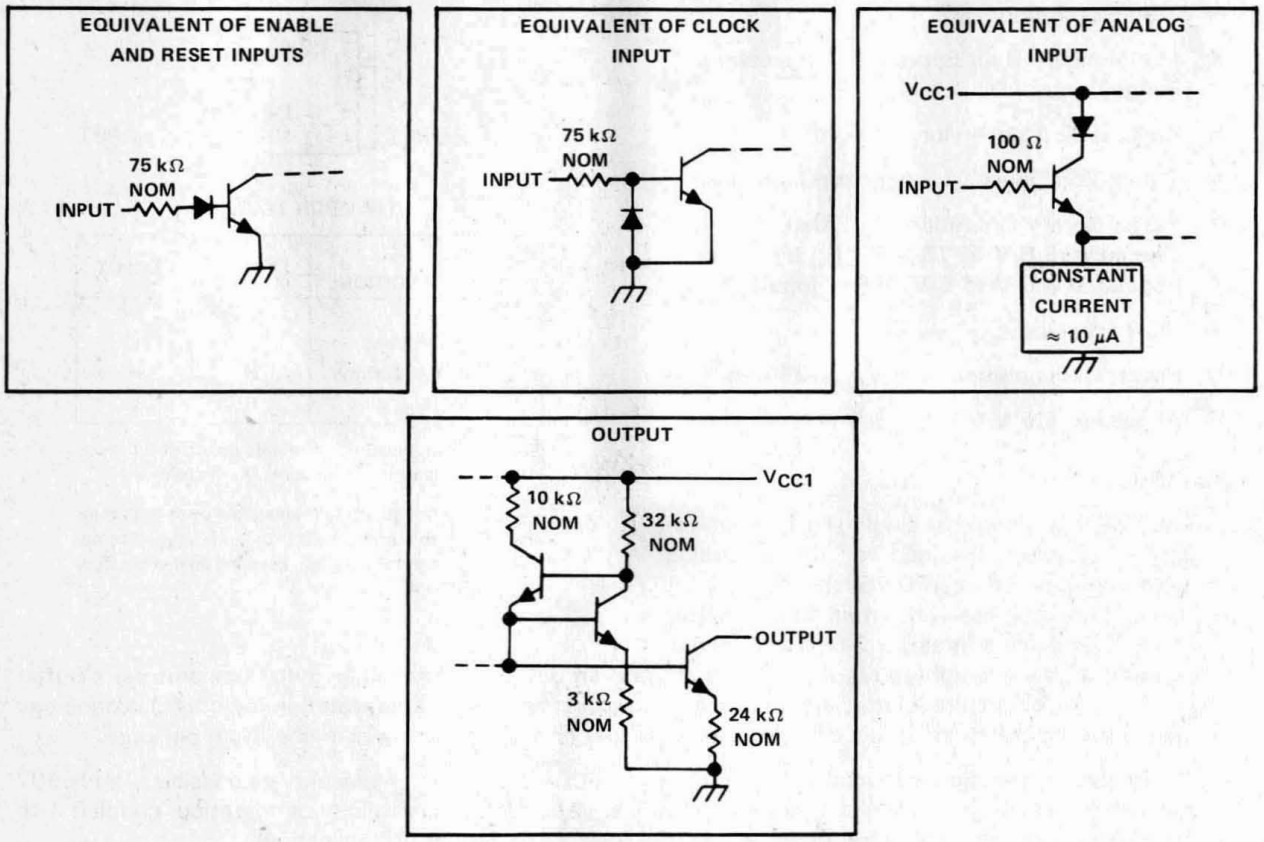
schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1)	6.5 V
Supply voltage, V_{CC2}	20 V
Input voltage at analog input	6.5 V
Input voltage at enable, clock, and reset inputs	±20 V
On-state output voltage	6 V
Off-state output voltage	20 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1000 mW
Operating free-air temperature range: TL507I	−40°C to 85°C
TL507C	0 to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. For operation above 25°C free-air temperature, derate linearly to 520 mW at 85°C at the rate of 8.0 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	3.5	5	6	V
Supply voltage, V_{CC2}	8	15	18	V
Input voltage at analog input	0		5.5	V
Input voltage at chip enable, clock, and reset inputs			±18	V
High-level input voltage, V_{IH}, reset and enable	2			V
Low-level input voltage, V_{IL}, reset and enable			0.8	V
On-state output voltage			5.5	V
Off-state output voltage			18	V
Clock frequency, f_{clock}	0	125	150	kHz

electrical characteristics over recommended operating free-air temperature range, V_{CC1} = V_{CC2} = 5 V (unless otherwise noted)

regulator section

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{CC1}	Supply voltage (output)	V_{CC2} = 10 to 18 V,	I_{CC1} = 0 to −1mA	5	5.5	6	V
I_{CC1}	Supply current	V_{CC1} = 5 V,	V_{CC2} open		5	8	mA
I_{CC2}	Supply current	V_{CC2} = 15 V,	V_{CC1} open		7	10	mA

inputs

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage‡	Clock Input				4.5	V
V_{T-}	Negative-going threshold voltage‡			0.4			V
V_{hys}	Hysteresis (V_{T+} − V_{T-})			2	2.6	4	V
I_{IH}	High-level input current	Reset, Enable, and Clock	V_I = 2.4 V		17	35	μA
			V_I = 18 V	130	220	320	
I_{IL}	Low-level input current		V_I = 0			±10	μA
I_I	Analog input current		V_I = 4 V		10	300	nA

output section

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{OH}	High-level output current	V_{OH} = 18 V		0.1	100	μA
I_{OL}	Low-level output current	V_{OL} = 5.5 V	5	10	15	mA
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA		80	400	mV

operating characteristics over recommended operating free-air temperature range, V_{CC1} = V_{CC2} = 5.12 V

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Overall error				±80	mV
Differential nonlinearity	See Figure 1			±20	mV
Zero error‡	Binary count = 0			±80	mV
Scale error	Binary count = 127			±80	mV
Full scale input voltage‡	Binary count = 127	3.74	3.82	3.9	V
Propagation delay time from reset or enable			2		μs

†All typical values are at T_A = 25°C.
‡These parameters are linear functions of V_{CC1}.

definitions

zero error

The absolute value of the difference between the actual analog voltage at the 01H-to-00H transition and the ideal analog voltage at that transition.

overall error

The magnitude of the deviation from a straight line between the endpoints of the transfer function.

differential nonlinearity

The maximum deviation of an analog-value change associated with a 1-bit code change (1 clock pulse) from its theoretical value of 1 LSB.

PARAMETER MEASUREMENT INFORMATION

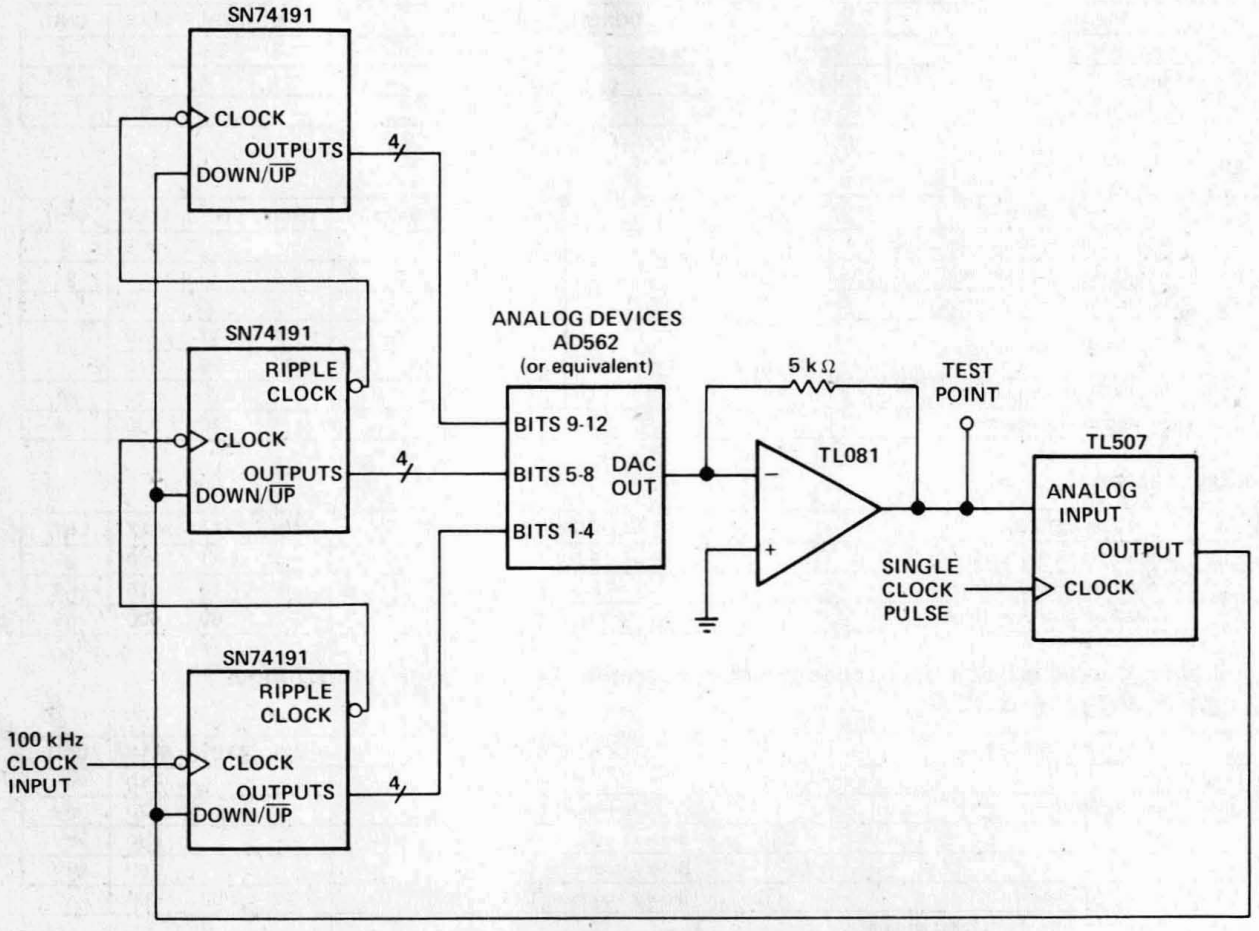


FIGURE 1. MONOTONICITY AND NONLINEARITY TEST CIRCUIT

PRINCIPLES OF OPERATION

The TL507 is a single-slope analog-to-digital converter. All single-slope converters are basically voltage-to-time or current-to-time converters. A study of the functional block diagram shows the versatility of the TL507.

An external clock signal is applied through a buffer to a negative-edge-triggered synchronous counter. Binary-weighted resistors from the counter are connected to an operational amplifier used as an adder. The operational amplifier generates a signal that ramps from $0.75 \cdot V_{CC1}$ down to $0.25 \cdot V_{CC1}$. Comparator 1 compares the ramp signal to the analog input signal. Comparator 2 functions as a fault defector. With the analog input voltage in the range $0.25 \cdot V_{CC1}$ to $0.75 \cdot V_{CC1}$, the duty cycle of the output signal is determined by the unknown analog input, as shown in Figure 2 and the Function Table.

For illustration, assume $V_{CC1} = 5.12$ V,

$$0.25 \cdot V_{CC1} = 1.28 \text{ V}$$

$$1 \text{ binary count} = \frac{(0.75 - 0.25)\, V_{CC1}}{128} = 20 \text{ mV}$$

$$0.75 \cdot V_{CC1} - 1 \text{ count} = 3.82 \text{ V}$$

The output is an open-collector n-p-n transistor capable of withstanding up to 18 V in the off state. The output is current limited to the 8- to 12-mA range; however, care must be taken to ensure that the output does not exceed 5.5 V in the on state.

The voltage regulator section allows operation from either an unregulated 8- to 18-V V_{CC2} source or a regulated 3.5- to 6-V V_{CC1} source. Regardless of which external power source is used, the internal circuitry operates at V_{CC1}. When operating from a V_{CC1} source, V_{CC2} may be connected to V_{CC1} or left open. When operating from a V_{CC2} source, V_{CC1} can be used as a reference voltage output.

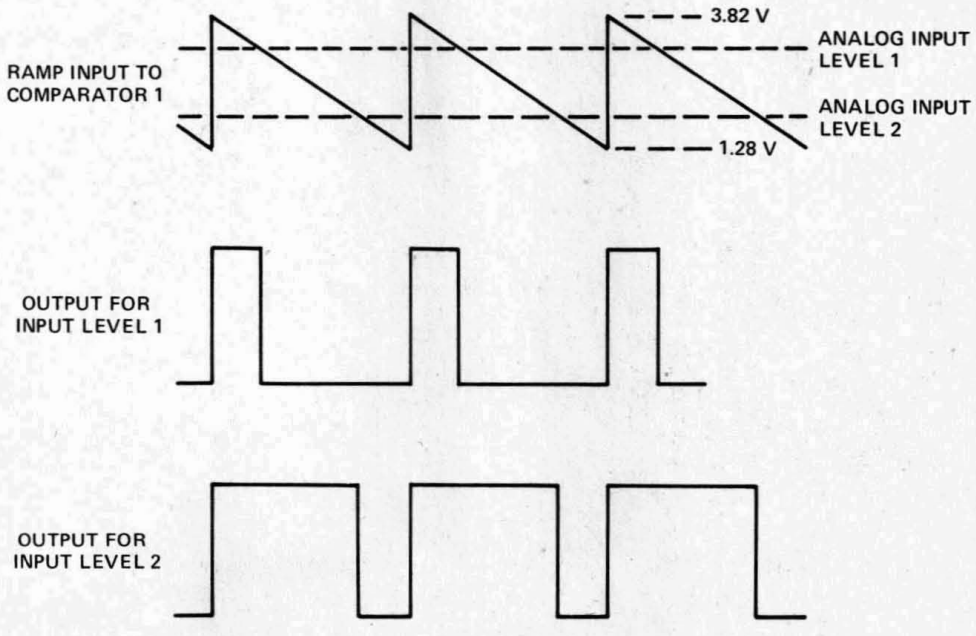


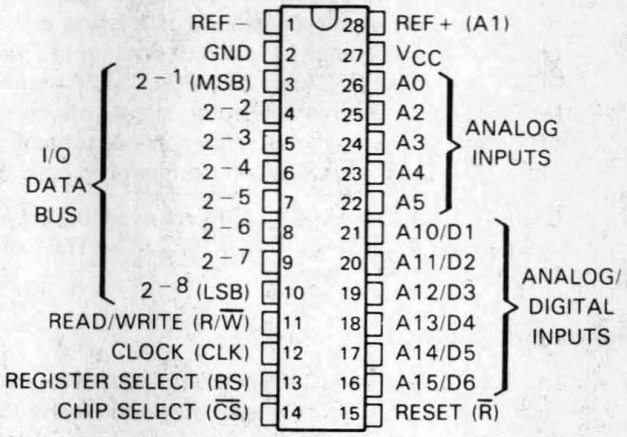
FIGURE 2

TLC532AM, TLC532AI, TLC533AM, TLC533AI
LinCMOS™ 8-BIT ANALOG-TO-DIGITAL PERIPHERALS WITH 5 ANALOG AND 6 DUAL-PURPOSE INPUTS

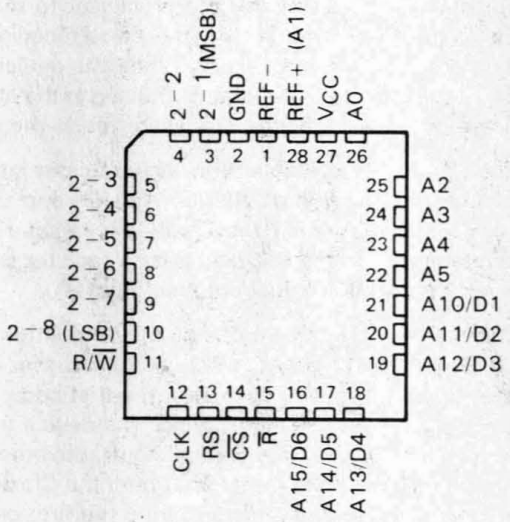
D2819, NOVEMBER 1983—REVISED SEPTEMBER 1986

- **LinCMOS™ Technology**
- **8-Bit Resolution**
- **Total Unadjusted Error . . . ±0.5 LSB Max**
- **Ratiometric Conversion**
- **Access Plus Conversion Time:**
  TLC532A . . . 15 μs Max
  TLC533A . . . 30 μs Max
- **3-State, Bidirectional I/O Data Bus**
- **5 Analog and 6 Dual-Purpose Inputs**
- **On-Chip 12-Channel Analog Multiplexer**
- **Three On-Chip 16-Bit Data Registers**
- **Software Compatible with Larger TL530 and TL531 (21-Input Versions)**
- **On-Chip Sample-and-Hold Circuit**
- **Single 5-V Supply Operation**
- **Low Power Consumption . . . 6.5 mW Typ**
- **Improved Direct Replacements for Texas Instruments TL532 and TL533, National Semiconductor ADC0829, and Motorola MC14442**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The TLC532A and TLC533A are monolithic LinCMOS™ peripheral integrated circuits each designed to interface a microprocessor for analog data acquisition. These devices are complete peripheral data acquisition systems on a single chip and can convert analog signals to digital data from up to 11 external analog terminals. Each device operates from a single 5-V supply and contains a 12-channel analog multiplexer, an 8-bit ratiometric analog-to-digital (A/D) converter, a sample-and-hold, three 16-bit registers, and microprocessor-compatible control circuitry. Additional features include a built-in self-test, six multipurpose (analog or digital) inputs, five external analog inputs, and an 8-pin input/output (I/O) data port. The three on-chip data registers store the control data, the conversion results, and the input digital data that can be accesssed via the microprocessor data bus in two 8-bit bytes (most-significant byte first). In this manner, a microprocessor can access up to 11 external analog inputs or 6 digital signals and the positive reference voltage that may be used for self-test.

FUNCTION TABLE

ADDRESS/CONTROL					DESCRIPTION
R/W	RS	CS	R	CLK	
X	X	X	L†		Reset
L	H	L	H	↓	Write bus data to control register
H	L	L	H	↑	Read data from analog conversion register
H	H	L	H	↑	Read data from ditigal data register
X	X	H	H	X	No response

H = High-level, L = Low-level, X = Irrelevant
↓ = High-to-low transition, ↑ = Low-to-high transition
†For proper operation, Reset must be low for at least three clock cycles.

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TEXAS INSTRUMENTS
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description (continued)

The A/D conversion uses the successive-approximation technique and switched-capacitor circuitry. This method eliminates the possibility of missing codes, nonmonotonicity, and a need for zero or full-scale adjustment. Any one of 11 analog inputs (or self-test) can be converted to an 8-bit digital word and stored within 10 μs (TLC532A) or 20 μs (TLC533A) after instructions from the microprocessor are recognized. The on-chip sample-and-hold automatically minimizes errors due to noise on the analog inputs. Furthermore, differential high-impedance reference inputs are available to help isolate the analog circuitry from the logic and supply noises while easing ratiometric conversion and scaling.

The TLC532AM and TLC533AM are available in both the N and FN plastic packages and are characterized for operation from −55°C to 125°C. The TLC532AI and TLC533AI are characterized for operation from −40°C to 85°C.

functional description

The TLC532A and TLC533A provide direct interface to a microprocessor-based system. Control of the TLC532A and TLC533A is handled via the 8-line TTL-compatible 3-state data bus, the three control inputs (Read/Write, Register Select, and Chip Select), and the Clock input. Each device contains three 16-bit internal registers — the control register, the analog conversion data register, and the digital data register.

A high level at the Read/Write input and a low level at the Chip Select input set the device to output data on the 8-line data bus for the processor to read. A low level at the Read/Write input and a low level at the Chip Select input set the device to receive instructions into the internal control register on the 8-line data bus from the processor. When the device is in the read mode and the Register Select input is low, the processor reads the data contained in the analog conversion data register. However, when the Register Select input is high, the processor reads the data contained in the digital data register.

The control register is a write-only register into which the microprocessor writes command instructions for the device to start A/D conversion and to select the analog channel to be converted. The analog conversion data register is a read-only register that contains the current converter status and most recent conversion results. The digital data register is also a read-only register that holds the digital input logic levels from the six dual-purpose inputs.

Internally each device contains a byte pointer that selects the appropriate byte during two cycles of the Clock input in a normal 16-bit microprocessor instruction. The internal pointer automatically points to the most significant (MS) byte after the first complete clock cycle any time that the Chip Select is at the high level for at least one clock cycle. The device treats the next signal on the 8-line data bus as the MS byte. A low level at the Chip Select input activates the inputs and outputs and an internal function decoder. However, no data is transferred until the Clock goes high. The internal byte pointer first points to the MS byte of the selected register during the first clock cycle. After the first clock cycle in which the MS byte is accessed, the internal pointer switches to the LS byte and remains there for as long as Chip Select is low. The MS byte of any register may be accessed by either an 8-bit or a 16-bit microprocessor instruction; however, the LS byte may only be accessed by a 16-bit microprocessor instruction.

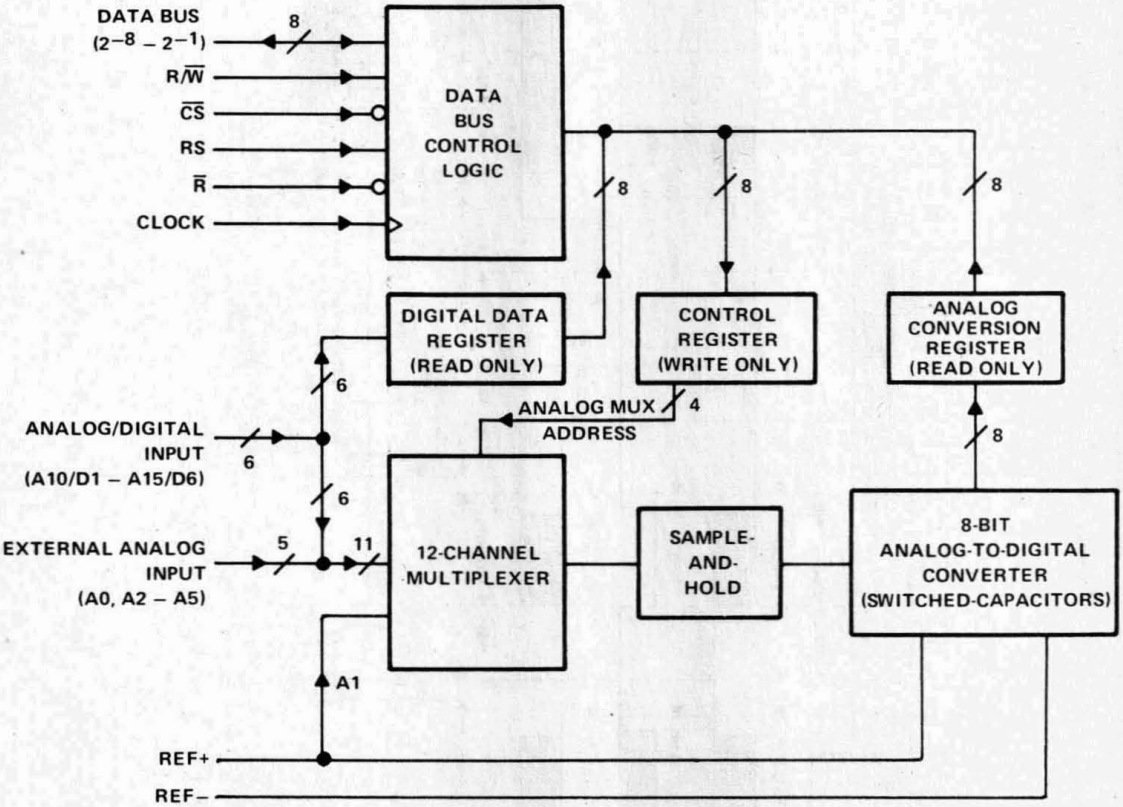
Normally, a 2-byte word is written or read from the controlling processor, but a single byte can be read by the processor by manipulating the Chip Select input. This can be used to read conversion status from the analog conversion data register or the digital multipurpose input levels from the digital data register. The format and content of each 2-byte word is shown in Figures 1 through 3.

functional description (continued)

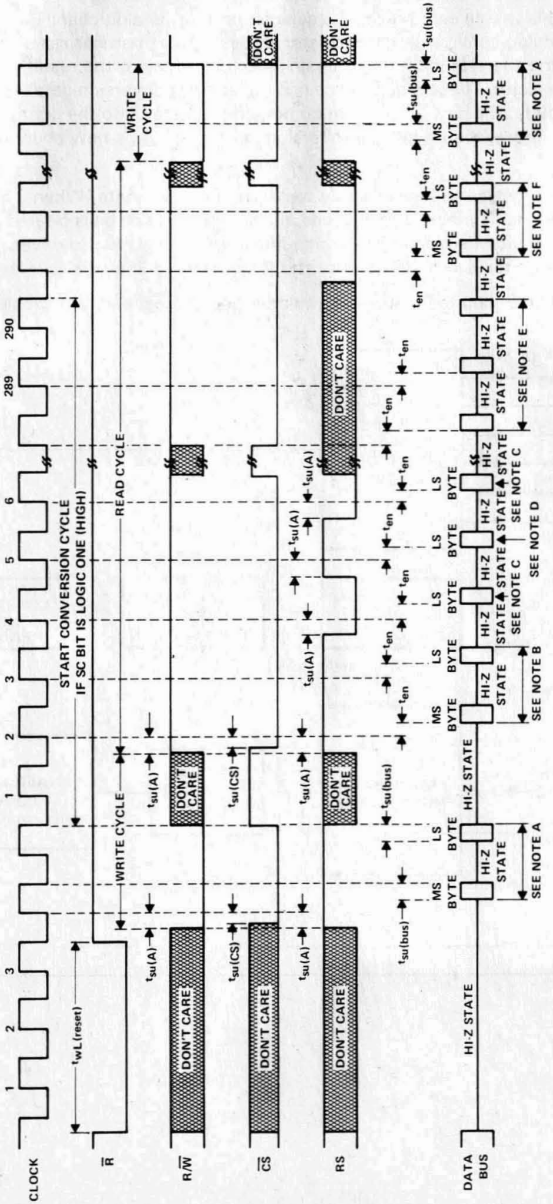
A conversion cycle starts after a 2-byte instruction is written to the control register and the start conversion (SC) bit is a logic high. This 2-byte instruction also selects the input analog channel to be converted. The status (EOC) bit in the analog conversion data register is reset, and it remains reset until the conversion is complete, at which time the status bit is set again. After conversion, the results are loaded into the analog conversion data register. These results remain in the analog conversion data register until the next conversion cycle is complete. If a new conversion command is entered into the control register while the conversion cycle is in progress, the on-going conversion is aborted and a new channel acquisition cycle begins immediately.

The Reset input allows the device to be externally forced to a known state. When a low level is applied to the Reset input for a minimum of three clock periods, the start conversion bit is cleared. The A/D converter is then idled and all the outputs are placed in the high-impedance off-state. However, the content of the analog conversion data register is not affected by the Reset input going to a low level.

Detailed information on interfacing to most popular microprocessors is readily available from the factory.

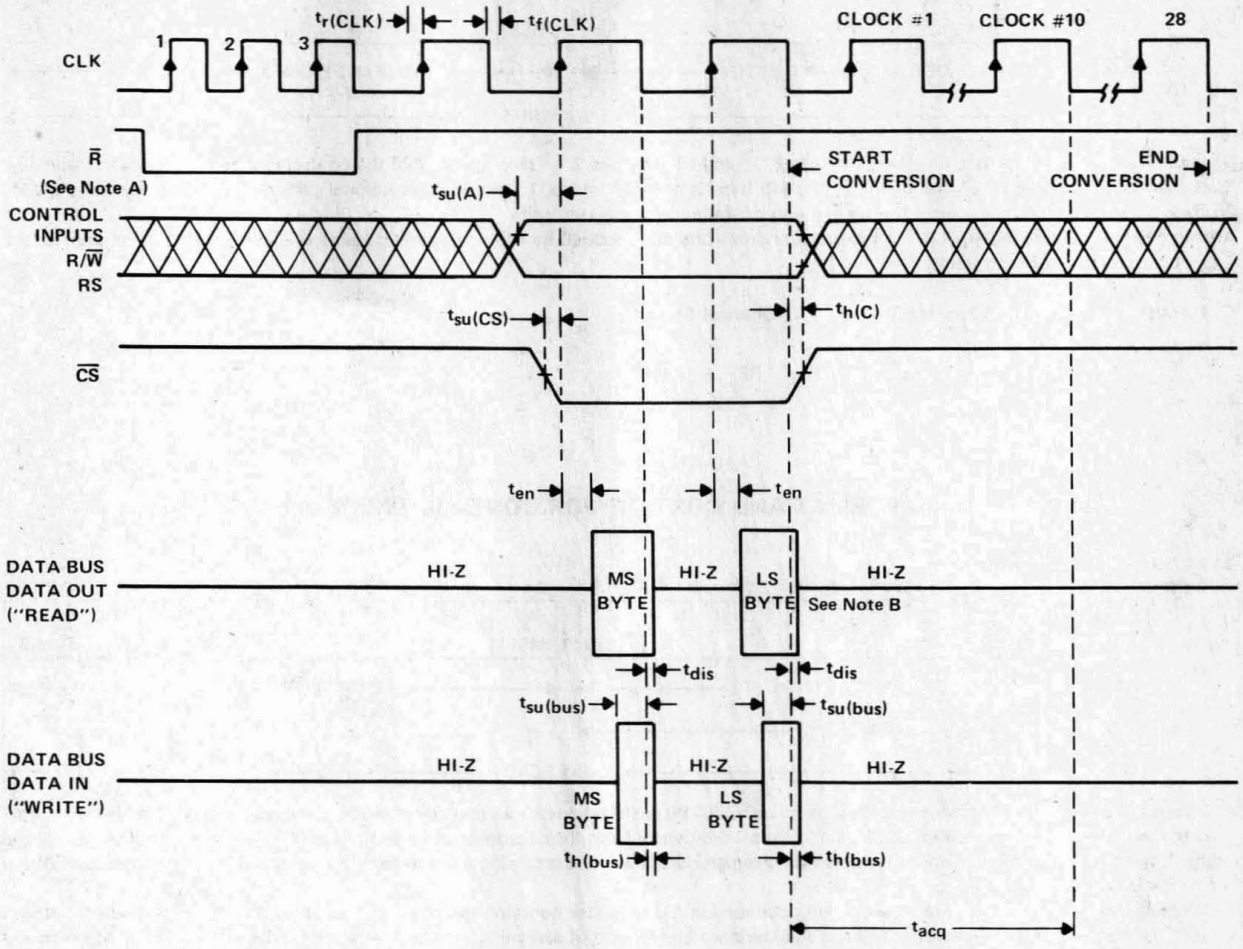


typical operating sequence



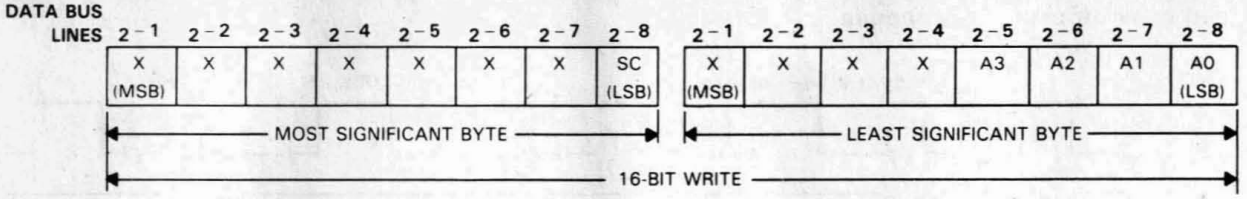
NOTES: A. This is a 16-bit input instruction from the microprocessor being sent to the control data register.
B. This is the 2-byte (16-bit) content of the digital data register being sent to the microprocessor.
C. This is the LS byte (8-bit) content of the analog conversion data register being sent to the microprocessor.
D. This is the LS byte (8-bit) content of the digital data register being sent to the microprocessor.
E. These are MS byte (8-bit), LS byte (8-bit), and LS byte (8-bit) content of the analog conversion data register or digital data register being sent to the microprocessor.
F. This is the 2-byte (16-bit) content of the analog conversion data register being sent to the microprocessor.

read or write cycle time sequence



NOTES: A. The reset pulse ($\overline{R}$ low) is required only during power-up.

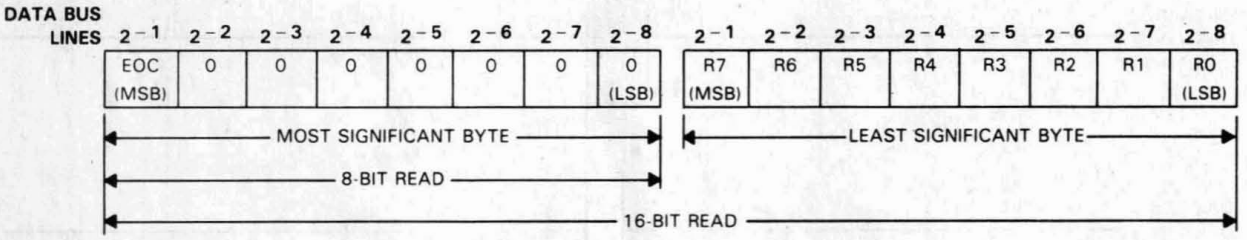
B. The most significant byte output of Data Out occurs when CLK is high. When CLK is low, Data Out is in the high-impedance (off) state. When CLK goes high again, the least significant byte is placed on the data bus. At this point, the least significant byte remains on the bus for as long as CLK is kept high.



Unused Bits (X) – The MS byte bits 2^{-1} through 2^{-7} and LS byte bits 2^{-1} through 2^{-4} of the control register are not used internally.
Start Conversion (SC) – When the SC bit in the MS byte is set to a logical 1, and analog-to-digital conversion on the specified analog channel begins immediately after the completion of the control register write.
Analog Multiplex Address (A0-A3) – These four address bits are decoded by the analog multiplexer and used to select the appropriate analog channel as shown below:

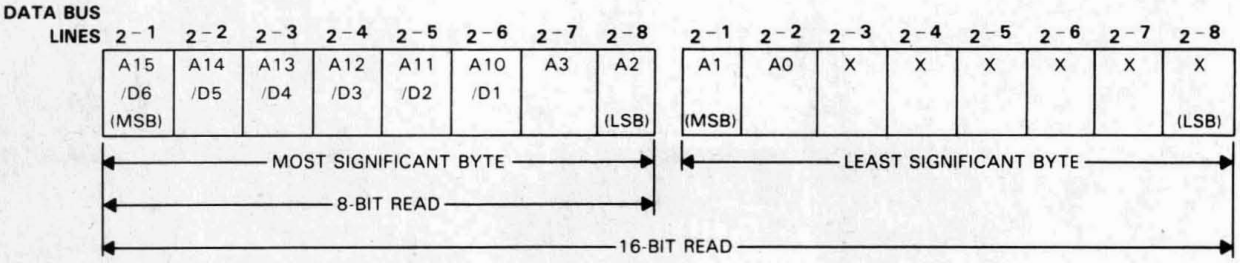
Hexadecimal Address (A3 = MSB)	Channel Select
0	A0
1	REF + (A1)
2-5	A2-A5
6-9 (not used)	
A-F	A10-A15

FIGURE 1. WORD FORMAT AND CONTENT FOR CONTROL REGISTER 2-BYTE WRITE



A/D Status (EOC) – The A/D status end-of-conversion (EOC) bit is set whenever an analog-to-digital conversion is successfully completed by the A/D converter. The status bit is cleared by a 16-bit write from the microprocessor to the control register. The remainder of the bits in the MS byte of the analog conversion data register are always reset to logical 0 to simplify microprocessor interrogation of the A/D converter status.
A/D Result (R0-R7) – The LS byte of the analog conversion data register contains the result of the analog-to-digital conversion. Result bit R7 is the MSB and the converter follows the standard convention of assigning a code of all ones (11111111) to a full-scale analog voltage. There are no special overflow or underflow indications.

FIGURE 2. WORD FORMAT AND CONTENT FOR ANALOG CONVERSION DATA REGISTER 1-BYTE AND 2-BYTE READ



Shared Digital Port (A10/D1-A15/D6) – The voltage present on these pins is interpreted as a digital signal, and the corresponding states are read from these bits. A digital value is given for each pin even if some or all of these pins are being used as analog inputs.
Analog Multiplexer Address (A0-A3) – The address of the selected analog channel presently addressed is given by these bits.
Unused Bits (X) – LS byte bits 2^{-3} through 2^{-8} of the digital data register are not used.

FIGURE 3. WORD FORMAT AND CONTENT FOR DIGITAL DATA REGISTER 1-BYTE AND 2-BYTE READ

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −0.3 V to 6.5 V
Input voltage range: Positive reference voltage . . . . . V_{REF-} to V_{CC} + 0.3 V
Negative reference voltage . . . . . −0.3 V to V_{REF+}
All other inputs . . . . . −0.3 V to V_{CC} + 0.3 V
Input current, I_I (any input) . . . . . ±10 mA
Total input current, (all inputs) . . . . . ±20 mA
Operating free-air temperature range: TLC532AM, TLC533AM . . . . . −55°C to 125°C
TLC532AI, TLC533AI . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C
Case temperature for 10 seconds: FN package . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

		TLC532A			TLC533A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.75	5	5.5	4.75	5	5.5	V
Positive reference voltage, V_{REF+} (see Note 2)		2.5	V_{CC}	$V_{CC}+0.1$	2.5	V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{REF-} (see Note 2)		−0.1	0	2.5	−0.1	0	2.5	V
Differential reference voltage, $V_{REF+} - V_{REF-}$		1	V_{CC}	$V_{CC}+0.2$	1	V_{CC}	$V_{CC}+0.2$	V
High-level input voltage, V_{IH}	Clock input	$V_{CC}-0.8$			$V_{CC}-0.8$			V
	All other digital inputs	2			2			
Low-level input voltage, V_{IL}	Any digital input			0.8			0.8	V
Clock frequency, f_{CLK}		0.1	2	2.048	0.1	1.048	1.06	MHz
CS setup time, $t_{su(CS)}$		75			100			ns
Address (R/W and RS) setup time, $t_{su(A)}$		100			145			ns
Data bus input setup time, $t_{su(bus)}$		140			185			ns
Control (R/W, RS, and CS) hold time, $t_{h(C)}$		10			20			ns
Data bus input hold time, $t_{h(bus)}$		15			20			ns
Pulse duration of control during read, $t_{w(C)}$		305			575			ns
Pulse duration, reset low, $t_{wL(reset)}$		3			3			Clock Cycles
Pulse duration of clock high, $t_{wH(CLK)}$		230			440			ns
Pulse duration of clock low, $t_{wL(CLK)}$		200			410			ns
Clock rise time, $t_{r(CLK)}$				15			25	ns
Clock fall time, $t_{f(CLK)}$				16			30	ns
Operating free-air temperature, T_A	TLC__AM	−55		125	−55		125	°C
	TLC__AI	−40		85	−40		85	

NOTE 2: Analog input voltages greater than or equal to that applied to the REF+ terminal convert to all ones (11111111), while input voltages equal to or less than that applied to the REF− terminal convert to all zeros (00000000). For proper operation, the positive reference voltage, V_{REF+}, must be at least 1 V greater than the negative reference voltage, V_{REF-}. In addition, unadjusted errors may increase as the differential reference voltage, $V_{REF+} - V_{REF-}$, falls below 4.75 V.

electrical characteristics over recommended operating free-air temperature range, V_{REF+} = V_{CC}, V_{REF-} at ground, f_{CLK} = 2 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −1.6 mA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 1.6 mA			0.4	V
I_{IH}	High-level input current	Any digital or Clock input	V_{IH} = 5.5 V			10	μA
		Any control input				1	
I_{IL}	Low-level input current	Any digital or Clock input	V_{IL} = 0			−10	μA
		Any control input				−1	
I_{OZ}	Off-state (high-impedance state) output current		V_O = V_{CC}			10	μA
			V_O = 0			−10	
I_I	Analog input current (see Note 3)		V_I = 0 to V_{CC}			±500	nA
	Leakage current between selected channel and all other analog channels		V_I = 0 to V_{CC}, Clock input at 0 V			±400	nA
C_i	Input capacitance	Digital pins 3 thru 10			4	30	pF
		Any other input pin			2	15	
$I_{CC}+I_{REF+}$	Supply current plus reference current		V_{CC} = V_{REF+} = 5.5 V, Outputs open		1.5	3	mA
I_{CC}	Supply current		V_{CC} = 5.5 V		1.4	2	mA

NOTE 3: Analog input current is an average of the current flowing into a selected analog channel input during one full conversion cycle.

operating characteristics over recommended operating free-air temperature range, V_{REF+} = V_{CC}, V_{REF-} at ground, f_{CLK} = 2 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	Linearity error (see Note 4)					±0.5	LSB
	Zero error (see Note 5)					±0.5	LSB
	Full-scale error (see Note 5)					±0.5	LSB
	Total unadjusted error (see Note 6)					±0.5	LSB
	Absolute accuracy error (see Note 7)					±1	LSB
t_{conv}	Conversion time (including channel acquisition time)				30		Clock Cycles
t_{acq}	Channel acquisition time prior to starting conversion				10		Clock Cycles
t_{en}	Data output enable time (see Note 8)		C_L = 50 pF, R_L = 3 kΩ,			250	ns
t_{dis}	Data output disable time		C_L = 50 pF, R_L = 3 kΩ	10			ns
$t_{r(bus)}$	Data bus output rise time	High impedance to high level	C_L = 50 pF, R_L = 3 kΩ			150	ns
		Low-to-high level				300	
$t_{f(bus)}$	Data bus output fall time	High impedance to low level	C_L = 50 pF, R_L = 3 kΩ			150	ns
		High-to-low level				300	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 4. Linearity error is the deviation from the best straight line through the A/D transfer characteristics.
5. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
6. Total unadjusted error is the sum of linearity, zero, and full-scale errors.
7. Absolute accuracy error is the maximum difference between an analog value and the nominal midstep value within any step. This includes all errors including inherent quantization error, which is the ±0.5 LSB uncertainty caused by the A/D converters' finite resolution.
8. If chip-select setup time, $t_{su(CS)}$, is less than 0.14 μs, the effective data output enable time, t_{en}, may extend such that $t_{su(CS)}+t_{en}$ is equal to a maximum of 0.475 μs.

electrical characteristics over recommended ranges V_{CC}, V_{REF+}, and operating free-air temperature, V_{REF-} at ground, f_{CLK} = 1.048 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −1.6 mA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 1.6 mA			0.4	V
I_{IH}	High-level input current	Any digital or Clock input	V_{IH} = 5.5 V			10	μA
		Any control input				1	
I_{IL}	Low-level input current	Any digital or Clock input	V_{IL} = 0			−10	μA
		Any control input				−1	
I_{OZ}	Off-state (high-impedance state) output current		$V_O = V_{CC}$			10	μA
			V_O = 0			−10	
I_I	Analog input current (see Note 3)		V_I = 0 to V_{CC}			±500	nA
	Leakage current between selected channel and all other analog channels		V_I = 0 to V_{CC}, Clock input at 0 V			±400	nA
C_i	Input capacitance	Digital pins 3 thru 10			4	30	pF
		Any other input pin			2	15	
$I_{CC}+I_{REF+}$	Supply current plus reference current		V_{CC} = V_{REF+} = 5.5 V, Outputs open		1.3	3	mA
I_{CC}	Supply current		V_{CC} = 5.5 V		1.2	2	mA

NOTE 3: Analog input current is an average of the current flowing into a selected analog channel input during one full conversion cycle.

operating characteristics over recommended ranges V_{CC}, V_{REF+}, and operating free-air temperature, V_{REF-} at ground, f_{clock} = 1.048 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	Linearity error (see Note 4)					±0.5	LSB
	Zero error (see Note 5)					±0.5	LSB
	Full-scale error (see Note 5)					±0.5	LSB
	Total unadjusted error (see Note 6)					±0.5	LSB
	Absolute accuracy error (see Note 7)					±1	LSB
t_{conv}	Conversion time (including channel acquisition time)				30		Clock Cycles
t_{acq}	Channel acquisition time prior to starting conversion				10		Clock Cycles
t_{en}	Data output enable time (see Note 8)		C_L = 50 pF, R_L = 3 kΩ,			335	ns
t_{dis}	Data output disable time		C_L = 50 pF, R_L = 3 kΩ	10			ns
$t_{r(bus)}$	Data bus output rise time	High impedance to high level	C_L = 50 pF, R_L = 3 kΩ			150	ns
		Low-to-high level				300	
$t_{f(bus)}$	Data bus output fall time	High impedance to low level	C_L = 50 pF, R_L = 3 kΩ			150	ns
		High-to-low level				300	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 4. Linearity error is the deviation from the best straight line through the A/D transfer characteristics.

5. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.

6. Total unadjusted error is the sum of linearity, zero, and full-scale errors.

7. Absolute accuracy error is the maximum difference between an analog value and the nominal midstep value within any step. This includes all errors including inherent quantization error, which is the ±0.5 LSB uncertainty caused by the A/D converters' finite resolution.

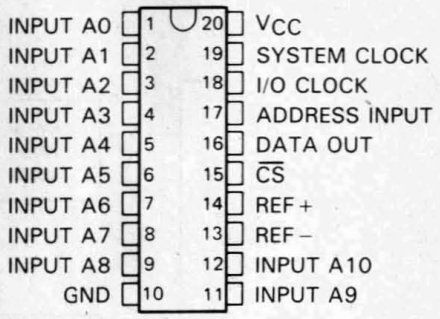
8. If chip-select setup time, $t_{su(CS)}$, is less than 0.14 μs, the effective data output enable time, t_{en}, may extend such that $t_{su(CS)}$ + t_{en} is equal to a maximum of 0.475 μs.

TLC540M, TLC540I, TLC541M, TLC541I
LinCMOS™ 8-BIT ANALOG-TO-DIGITAL PERIPHERALS WITH SERIAL CONTROL AND 11 INPUTS

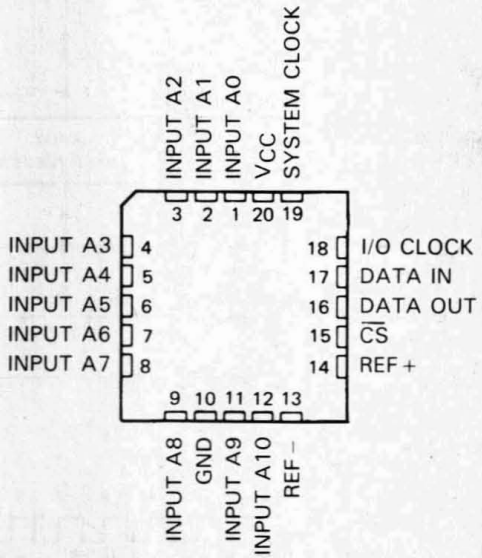
D2799, OCTOBER 1983—REVISED OCTOBER 1988

- **LinCMOS™ Technology**
- **8-Bit Resolution A/D Converter**
- **Microprocessor Peripheral or Stand-Alone Operation**
- **On-Chip 12-Channel Analog Multiplexer**
- **Built-In Self-Test Mode**
- **Software-Controllable Sample and Hold**
- **Total Unadjusted Error . . . ±0.5 LSB Max**
- **TLC541 is Direct Replacement for Motorola MC145040 and National Semiconductor ADC0811. TLC540 is Capable of Higher Speed**
- **Pinout and Control Signals Compatible with TLC1540 Family of 10-Bit A/D Converters**

DW OR N PACKAGE
(TOP VIEW)



FN CHIP CARRIER PACKAGE
(TOP VIEW)



TYPICAL PERFORMANCE	TLC540	TLC541
Channel Acquisition Sample Time	2 μs	3.6 μs
Conversion Time	9 μs	17 μs
Samples per Second	75 × 10^3	40 × 10^3
Power Dissipation	6 mW	6 mW

description

The TLC540 and TLC541 are LinCMOS™ A/D peripherals built around an 8-bit switched-capacitor successive-approximation A/D converter. They are designed for serial interface to a microprocessor or peripheral via a three-state output with up to four control inputs [including independent System Clock, I/O Clock, Chip Select ($\overline{CS}$), and Address Input]. A 4-MHz system clock for the TLC540 and a 2.1-MHz system clock for the TLC541 with a design that includes simultaneous read/write operation allow high-speed data transfers and sample rates of up to 75,180 samples per second for the TLC540 and 40,000 samples per second for the TLC541. In addition to the high-speed converter and versatile control logic, there is an on-chip 12-channel analog multiplexer that can be used to sample any one of 11 inputs or an internal "self-test" voltage, and a sample-and-hold that can operate automatically or under microprocessor control. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The converters incorporated in the TLC540 and TLC541 feature differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and analog circuitry isolation from logic and supply noises. A switched-capacitor design allows low-error (±0.5 LSB) conversion in 9 μs for the TLC540 and 17 μs for the TLC541 over the full operating temperature range.

The M-suffix versions are characterized for operation from −55°C to 125°C. The I-suffix versions are characterized for operation from −40°C to 85°C.

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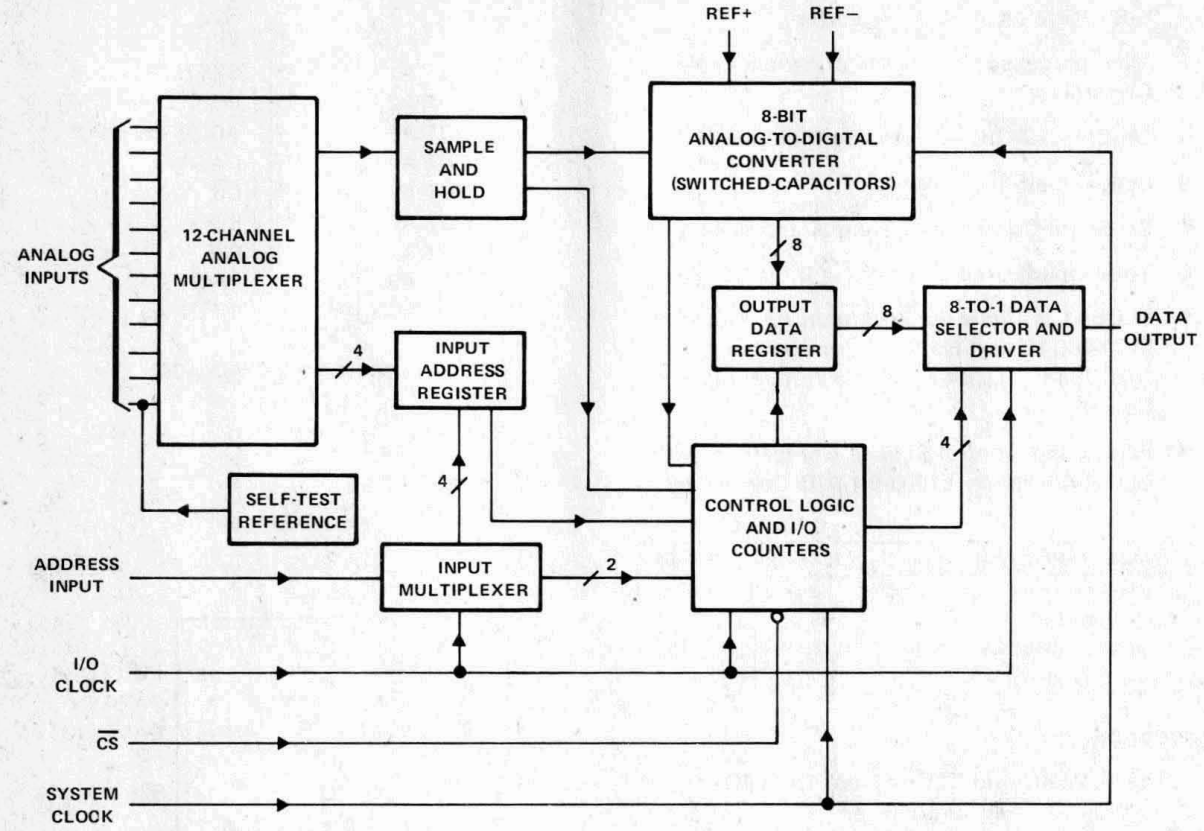
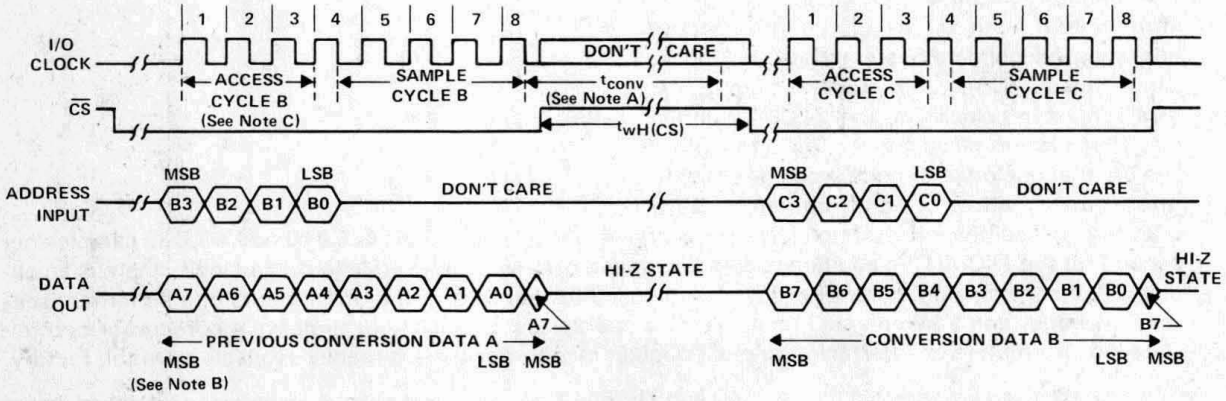
functional block diagram



operating sequence



NOTES: A. The conversion cycle, which requires 36 System Clock periods, is initiated on the 8th falling edge of the I/O Clock after $\overline{CS}$ goes low for the channel whose address exists in memory at that time. If $\overline{CS}$ is kept low during conversion, the I/O Clock must remain low for at least 36 System Clock cycles to allow conversion to be completed.

B. The most significant bit (MSB) will automatically be placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining seven bits (A6-A0) will be clocked out on the first seven I/O Clock falling edges.

C. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for three System Clock cycles (or less) after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip-select setup time has elapsed.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range (any input) . . . . . −0.3 V to V_{CC} + 0.3 V
Output voltage range . . . . . −0.3 V to V_{CC} + 0.3 V
Peak input current range (any input) . . . . . ±10 mA
Peak total input current (all inputs) . . . . . ±30 mA
Operating free-air temperature range: TLC540I, TLC541I . . . . . −40°C to 85°C
TLC540M, TLC541M . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package . . . . . 260°C

NOTE 1: All voltage values are with respect to digital ground with REF− and GND wired together (unless otherwise noted).

recommended operating conditions

			TLC540			TLC541			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.75	5	5.5	4.75	5	5.5	V
Positive reference voltage, V_{REF+} (see Note 2)			2.5	V_{CC}	$V_{CC}+0.1$	2.5	V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{REF-} (see Note 2)			−0.1	0	2.5	0.1	0	2.5	V
Differential reference voltage, $V_{REF+} - V_{REF-}$ (see Note 2)			1	V_{CC}	$V_{CC}+0.2$	1	V_{CC}	$V_{CC}+0.2$	V
Analog input voltage (see Note 2)			0		V_{CC}	0		V_{CC}	V
High-level control input voltage, V_{IH}			2			2			V
Low-level control input voltage, V_{IL}					0.8			0.8	V
Setup time, address bits at data input before I/O CLK↑, $t_{su(A)}$			200			400			ns
Hold time, address bits after I/O CLK↑, $t_{h(A)}$			0			0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 3)			3			3			System clock cycles
$\overline{CS}$ high during conversion, $t_{wH(CS)}$			36			36			System clock cycles
Input/Output clock frequency, $f_{CLK(I/O)}$			0		2.048	0		1.1	MHz
System clock frequency, $f_{CLK(SYS)}$			$f_{CLK(I/O)}$		4	$f_{CLK(I/O)}$		2.1	MHz
System clock high, $t_{wH(SYS)}$			110			210			ns
System clock low, $t_{wL(SYS)}$			100			190			ns
Input/Output clock high, $t_{wH(I/O)}$			200			404			ns
Input/Output clock low, $t_{wL(I/O)}$			200			404			ns
Clock transition time (see Note 4)	System	$f_{CLK(SYS)} \le 1048$ kHz			30			30	ns
		$f_{CLK(SYS)} > 1048$ kHz			20			20	
	I/O	$f_{CLK(I/O)} \le 525$ kHz			100			100	ns
		$f_{CLK(I/O)} > 525$ kHz			40			40	
Operating free-air temperature, T_A		TLC540M, TLC541M	−55		125	−55		125	°C
		TLC540I, TLC541I	−40		85	−40		85	

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all "1"s (11111111), while input voltages less than that applied to REF− convert as all "0"s (00000000). For proper operation, REF+ voltage must be at least 1 V higher than REF− voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.

3. To minimize errors caused by noise at the chip select input, the internal circuitry waits for three System Clock cycles (or less) after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in an address until the minimum chip select setup time has elapsed.

4. This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 μs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating temperature range, V_{CC} = V_{REF+} = 4.75 V to 5.5 V (unless otherwise noted), $f_{CLK(I/O)}$ = 2.048 MHz for TLC540 or $f_{CLK(I/O)}$ = 1.1 MHz for TLC541

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (pin 16)		V_{CC} = 4.75 V,	I_{OH} = 360 μA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V,	I_{OL} = 1.6 mA			0.4	V
I_{OZ}	Off-state (high-impedance state) output current		V_O = V_{CC},	$\overline{CS}$ at V_{CC}			10	μA
			V_O = 0,	$\overline{CS}$ at V_{CC}			−10	
I_{IH}	High-level input current		V_I = V_{CC}			0.005	2.5	μA
I_{IL}	Low-level input current		V_I = 0			−0.005	−2.5	μA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			1.2	2.5	mA
	Selected channel leakage current		Selected channel at V_{CC}, Unselected channel at 0 V			0.4	1	μA
			Selected channel at 0 V, Unselected channel at V_{CC}			−0.4	−1	
I_{CC} + I_{REF}	Supply and reference current		V_{REF+} = V_{CC},	$\overline{CS}$ at 0 V		1.3	3	mA
C_i	Input capacitance	Analog inputs				7	55	pF
		Control inputs				5	15	

†All typical values are at T_A = 25°C.

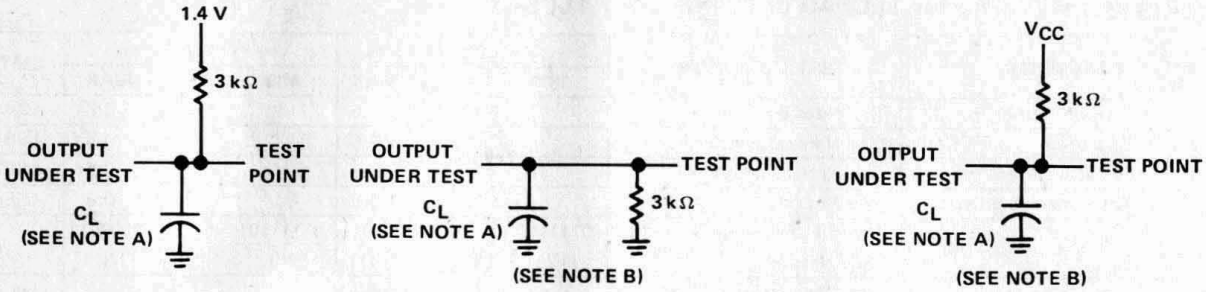
operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{REF+} = 4.75$ V to 5.5 V, $f_{CLK(I/O)} = 2.048$ MHz for TLC540 or 1.1 MHz for TLC541, $f_{CLK(SYS)} = 4$ MHz for TLC540 or 2.1 MHz for TLC541.

PARAMETER		TEST CONDITIONS	TLC540			TLC541			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
	Linearity error	See Note 5			±0.5			±0.5	LSB
	Zero error	See Notes 2 and 6			±0.5			±0.5	LSB
	Full-scale error	See Notes 2 and 6			±0.5			±0.5	LSB
	Total unadjusted error	See Note 7			±0.5			±0.5	LSB
	Self-test output code	Input A11 address = 1011 (See Note 8)	01111101 (125)		10000011 (131)	01111101 (125)		10000011 (131)	
t_{conv}	Conversion time	See Operating Sequence			9			17	μs
	Total access and conversion time	See Operating Sequence			13.3			25	μs
t_{acq}	Channel acquisition time (sample cycle)	See Operating Sequence			4			4	I/O clock cycles
t_v	Time output data remains valid after I/O clock↓		10			10			ns
t_d	Delay time, I/O clock↓ to data output valid	See Parameter Measurement Information			300			400	ns
t_{en}	Output enable time				150			150	ns
t_{dis}	Output disable time				150			150	ns
$t_{r(bus)}$	Data bus rise time				300			300	ns
$t_{f(bus)}$	Data bus fall time				300			300	ns

NOTES: 2. Analog input voltages greater than that applied to REF+ convert to all "1"s (11111111), while input voltages less than that applied to REF− convert to all "0"s (00000000). For proper operation, REF+ voltage must be at least 1 V higher than REF− voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.

5. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
6. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
7. Total unadjusted error is the sum of linearity, zero, and full-scale errors.
8. Both the input address and the output codes are expressed in positive logic.

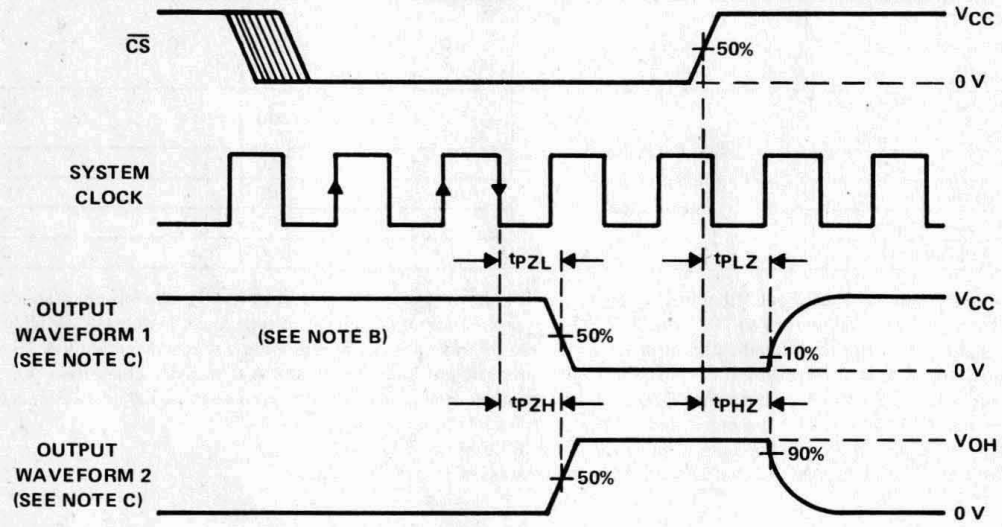
PARAMETER MEASUREMENT INFORMATION



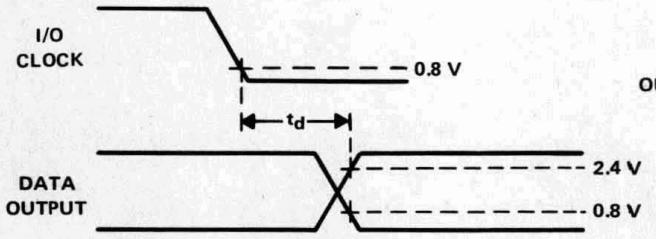
LOAD CIRCUIT FOR t_d, t_r, AND t_f

LOAD CIRCUIT FOR t_{PZH} AND t_{PHZ}

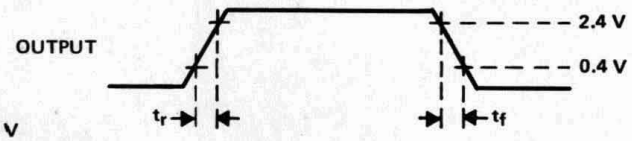
LOAD CIRCUIT FOR t_{PZL} AND t_{PLZ}



VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORM FOR DELAY TIME



VOLTAGE WAVEFORM FOR RISE AND FALL TIMES

NOTES: A. C_L = 50 pF for TLC540 and 100 pF for TLC541.
B. t_{en} = t_{PZH} or t_{PZL}, t_{dis} = t_{PHZ} or t_{PLZ}.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

principles of operation

The TLC540 and TLC541 are each complete data acquisition systems on a single chip. They include such functions as analog multiplexer, sample-and-hold, 8-bit A/D converter, data and control registers, and control logic. For flexibility and access speed, there are four control inputs [two clocks, chip select ($\overline{CS}$), and address]. These control inputs and a TTL-compatible 3-state output are intended for serial communications with a microprocessor or microcomputer. With judicious interface timing, with TLC540 a conversion can be completed in 9 μs, while complete input-conversion-output cycles can be repeated every 13 μs. With TLC541 a conversion can be completed in 17 μs, while complete input-conversion-output cycles are repeated every 25 μs. Furthermore, this fast conversion can be executed on any of 11 inputs or its built-in "self-test," and in any order desired by the controlling processor.

The System and I/O Clocks are normally used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Once a clock signal within the specification range is applied to the System Clock input, the control hardware and software need only be concerned with addressing the desired analog channel, reading the previous conversion result, and starting the conversion by using the I/O Clock. The System Clock will drive the "conversion crunching" circuitry so that the control hardware and software need not be concerned with this task.

When $\overline{CS}$ is high, the Data Output pin is in a three-state condition and the Address Input and I/O Clock pins are disabled. This feature allows each of these pins, with the exception of the $\overline{CS}$ pin, to share a control logic point with their counterpart pins on additional A/D devices when additional TLC540/541 devices are used. In this way, the above feature serves to minimize the required control logic pins when using multiple A/D devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. $\overline{CS}$ is brought low. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and then a falling edge of the System Clock after a low $\overline{CS}$ transition, before the low transition is recognized. This technique is used to protect the device against noise when the device is used in a noisy environment. The MSB of the previous conversion result will automatically appear on the Data Out pin.
2. A new positive-logic multiplexer address is shifted in on the first four rising edges of the I/O Clock. The MSB of the address is shifted in first. The negative edges of these four I/O clock pulses shift out the second, third, fourth, and fifth most significant bits of the previous conversion result. The on-chip sample-and-hold begins sampling the newly addressed analog input after the fourth falling edge. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Three clock cycles are then applied to the I/O pin and the sixth, seventh, and eighth conversion bits are shifted out on the negative edges of these clock cycles.
4. The final eighth clock cycle is applied to the I/O Clock pin. The falling edge of this clock cycle completes the analog sampling process and initiates the hold function. Conversion is then performed during the next 36 System Clock cycles. After this final I/O Clock cycle, $\overline{CS}$ must go high or the I/O Clock must remain low for at least 36 System Clock cycles to allow for the conversion function.

$\overline{CS}$ can be kept low during periods of multiple conversion. When keeping $\overline{CS}$ low during periods of multiple conversion, special care must be exercised to prevent noise glitches on the I/O Clock line. If glitches occur on the I/O Clock line, the I/O sequence between the microprocessor/controller and the device will lose synchronization. Also, if $\overline{CS}$ is taken high, it must remain high until the end of the conversion. Otherwise, a valid falling edge of $\overline{CS}$ will cause a reset condition, which will abort the conversion in progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 36 System Clock cycles occur. Such action will yield the conversion result of the previous conversion and not the ongoing conversion.

principles of operation (continued)

It is possible to connect the System and I/O Clock pins together in special situations in which controlling circuitry points must be minimized. In this case, the following special points must be considered in addition to the requirements of the normal control sequence previously described.

1. When $\overline{CS}$ is recognized by the device to be at a low level, the common clock signal is used as an I/O Clock. When $\overline{CS}$ is recognized by the device to be at a high level, the common clock signal is used to drive the ''conversion crunching'' circuitry.
2. The device will recognize a $\overline{CS}$ low transition only when the $\overline{CS}$ input changes and subsequently the System Clock pin receives two positive edges and then a negative edge. For this reason, after a $\overline{CS}$ negative edge, the first two clock cycles will not shift in the address because a low $\overline{CS}$ must be recognized before the I/O Clock can shift in an analog channel address. Also, upon shifting in the address, $\overline{CS}$ must be raised after the sixth I/O Clock pulse that has been recognized by the device, so that a $\overline{CS}$ low level will be recognized upon the lowering of the eighth I/O Clock signal that is recognized by the device. Otherwise, additional common clock cycles will be recognized as I/O Clock pulses and will shift in an erroneous address.

For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in time. This device will accommodate these applications. Although the on-chip sample-and-hold begins sampling upon the negative edge of the fourth I/O Clock cycle, the hold function is not initiated until the negative edge of the eighth I/O Clock cycle. Thus, the control circuitry can leave the I/O Clock signal in its high state during the eighth I/O Clock cycle until the moment at which the analog signal must be converted. The TLC540/TLC541 will continue sampling the analog input until the eighth falling edge of the I/O Clock. The control circuitry or software will then immediately lower the I/O Clock signal and hold the analog signal at the desired point in time and start conversion.

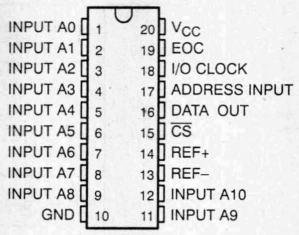
Detailed information on interfacing to most popular microprocessors is readily available from the factory.

- LinCMOS™ Technology
- 8-Bit Resolution A/D Converter
- Microprocessor Peripheral or Stand-Alone Operation
- On-Chip 12-Channel Analog Multiplexer
- Built-in Self-Test Mode
- Software-Controllable Sample and Hold
- Total Unadjusted Error . . . ±0.5 LSB Max
- Direct Replacement for Motorola MC145041
- On-Board System Clock
- End-of-Conversion (EOC) Output
- Pinout and Control Signals Compatible With TLC540 and TLC1540 Family of 10-Bit A/D Converters

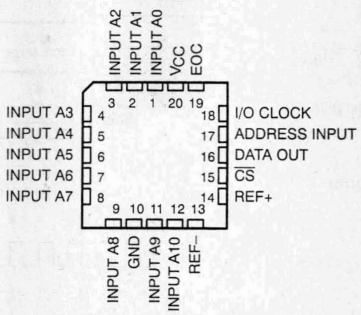
TYPICAL PERFORMANCE

Channel Acquisition/Sample Time	16 μs
Conversion TIme	20 μs
Samples per Second	25×10^3
Power Dissipation	10 mW

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The TLC542 is a LinCMOS™ A/D peripheral built around an 8-bit switched-capacitor successive-approximation A/D converter. The device is designed for serial interface to a microprocessor or peripheral via a 3-state output with three inputs (including I/O CLOCK, $\overline{CS}$ (chip select), and ADDRESS INPUT). The TLC542 allows high-speed data transfers and sample rates of up to 40,000 samples per second. In additioin to the high-speed converter and versatile control logic, an on-chip 12-channel analog multiplexer can sample any one of 11 inputs or an internal "self-test" voltage, and the sample and hold is started under microprocessor control. At the end of conversion, the end-of-conversion (EOC) output pin goes high to indicate that conversion is complete. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The converter incorporated in the TLC542 features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noises. A switched-capacitor design allows low-error (±0.5 LSB) conversion in 20 μs over the full operating temperature range.

The TLC542M is available in both the N and FN plastic packages. The TLC542C is characterized for operation from 0°C to 70°C, and the TLC542M is characterized for operation from –55°C to 125°C, and the TLC542I is characterized for operation from –40°C to 85°C.

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TLC542C, TLC542I, TLC542M
LinCMOS™ 8-BIT ANALOG-TO-DIGITAL PERIPHERALS
WITH SERIAL CONTROL AND 11 INPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

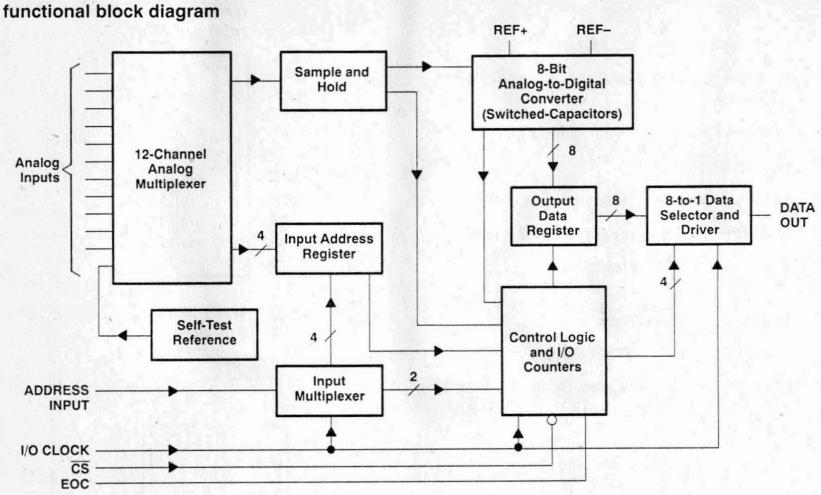
Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range (any input) . . . . . –0.3 V to V_{CC} + 0.3 V
Output voltage range . . . . . –0.3 V to V_{CC} + 0.3 V
Peak input current range (any input) . . . . . ±20 mA
Peak total input current (all inputs) . . . . . ±30 mA
Operating free-air temperature range: TLC542C . . . . . 0°C to 70°C
TLC542I . . . . . –40°C to 85°C
TLC542IM . . . . . –55°C to 125°C
Storage temperature range . . . . . –65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTE 1: All voltage values are with respect to digital ground with REF– and GND wired together (unless otherwise noted).

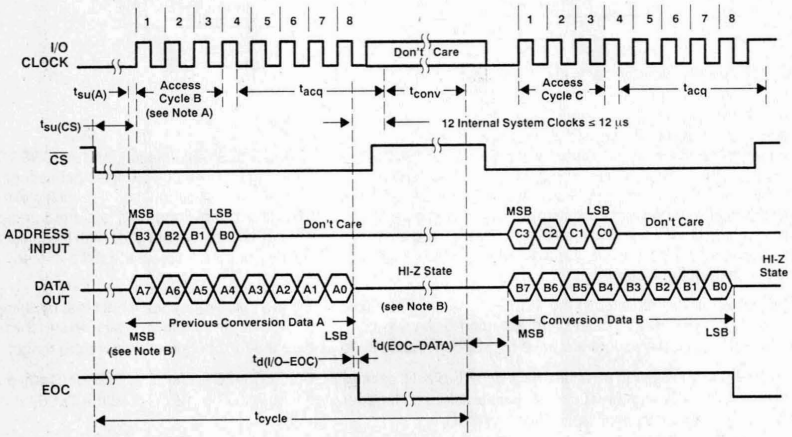
recommended operating conditions, V_{CC} = 4.75 to 5.5 V

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.5	V
Positive reference voltage, V_{REF+} (see Note 2)	V_{REF-}	V_{CC}	V_{CC} + 0.1	V
Negative reference voltage, V_{REF-} (see Note 2)	–0.1	0	V_{REF+}	V
Differential reference voltage, $V_{REF+} - V_{REF-}$ (see Note 2)	1	V_{CC}	V_{CC} + 0.2	V
Analog input voltage (see Note 4)	0		V_{CC}	V
	2			V

functional block diagram



operating sequence



NOTES: A. To minimize errors caused by noise at the chip select input, the internal circuitry waits for two rising edges and one falling edge of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. The $\overline{CS}$ setup time is given by the $t_{su(\overline{CS})}$ specifications. Therefore, no attempt should be made to clock-in an address until the minimum chip select setup time has elapsed.

B. The ouput is three-stated on $\overline{CS}$ going high or on the negative edge of the 8th I/O clock.

TLC542C, TLC542I, TLC542M
LinCMOS™ 8-BIT ANALOG-TO-DIGITAL PERIPHERALS
WITH SERIAL CONTROL AND 11 INPUTS

electrical characteristics over recommended operating temperature range, $V_{CC} = V_{REF+} = 4.75V$ to 5.5V (unless otherwise noted), $f_{CLK(I/O)} = 1.1$ MHz

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (DATA OUT)		V_{CC} = 4.75 V, I_{OH} = –360 µA		2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V, I_{OL} = 1.6 mA				0.4	V
	Off-state (high-impedance state) output current		$V_O = V_{CC}$, $\overline{CS}$ at V_{CC}				10	µA
			V_O = 0, $\overline{CS}$ at V_{CC}				–10	
I_{IH}	High-level input current		$V_I = V_{CC}$			0.005	2	µA
I_{IL}	Low-level input current		V_I = 0			–0.005	–2.5	µA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			1.2	2	mA
	Selected channel leakage current		Selected channel at V_{CC}, Unselected channel at 0 V	0°C to 70 °C			0.4	µA
				– 40°C to 85°C			0.4	
				– 55°C to 125°C			1	
			Selected channel at V_{CC}, Unselected channel at 0 V	0°C to 70 °C			0.4	
				– 40°C to 85 °C			–0.4	
				– 55°C to 125°C			–1	
I_{REF}	Maximum static analog reference current into REF+		$V_{REF+} = V_{CC}$, $V_{REF–}$ = GND				10	µA
C_i	Input capacitance	Analog inputs				7	55	pF
		Control inputs				5	15	

† All typical values are at T_A = 25°C.

operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{REF+} = 4.75$ to 5.5 V, $f_{CLK(I/O)} = 1$ MHZ

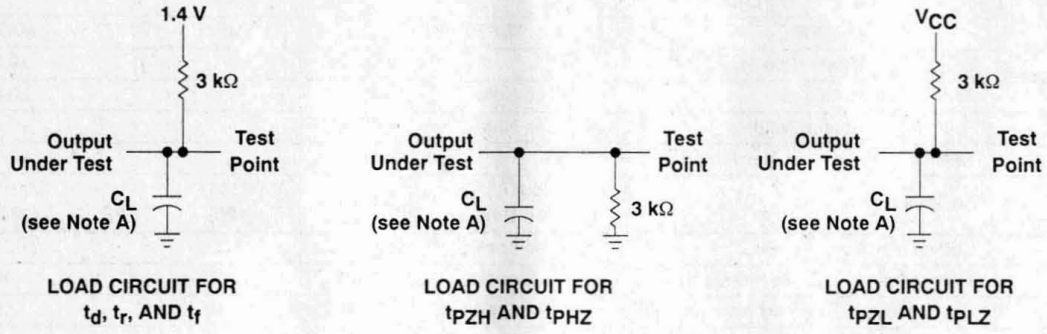
	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	Linearity error (see Note 5)				±0.5	LSB
	Zero error (see Note 6)	See Note 2			±0.5	LSB
	Full-scale error (see Note 6)	See Note 2			±0.5	LSB
	Total unadjusted error (see Note 7)				±0.5	LSB
	Self-test output code	Input A11 address = 1011, See Note 8	01111101 (126)	128	10000011 (130)	
t_{conv}	Conversion time	See operating sequence			20	µs
t_{cycle}	Total access and conversion cycle time	See operating sequence			40	µs
t_{acq}	Channel acquisition time (sample cycle)	See operating sequence			16	µs
t_v	Time ouput data remains valid after I/O CLK ↓	See Figure 5	10			ns
$t_{d(IO-DATA)}$	Delay time, I/O CLK ↓ to data output valid	See Figure 5			400	ns
$t_{d(IO-EOC)}$	Delay time, 8th I/O CLK ↓ to EOC ↓	See Figure 6			500	ns
$t_{d(EOC-DATA)}$	Delay time, EOC ↑ to data out (MSB)	See Figure 7			400	ns
t_{ZH}, t_{PZL}	Delay time, CS ↓ to data out (MSB)	See Figure 2			3.4	µs
t_{PHZ}, t_{PLZ}	Delay time, CS ↑ to data out (MSB)	See Figure 2			150	ns
$t_{r(EOC)}$	Rise time	See Figure 7			100	ns
$t_{f(EOC)}$	Fall time	See Figure 6			100	ns
$t_{r(bus)}$	Data bus rise time	See Figure 5			300	ns
$t_{f(bus)}$	Data bus fall time	See Figure 5			300	ns

† All typical values are at $T_A = 25°C$

NOTES: 2. Analog input voltages greater than that applied to REF+ convert to all ones (11111111), while input voltages less than that applied to REF– convert to all zeros (00000000). For proper operation, REF+ must be at least 1 V higher than REF–. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.

5. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
6. Zero Error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
7. Total unadjusted error is the sum of linearity, zero, and full-scale errors.
8. Both the input address and the output codes are expressed in positive logic. The A11 analog input signal is internally generated and is used for test purposes.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L = 50 pF.

Figure 1. Load Circuits

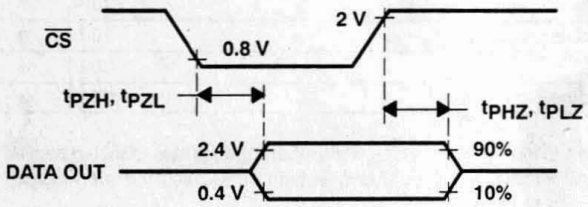


Figure 2. $\overline{CS}$ to Data Output Timing

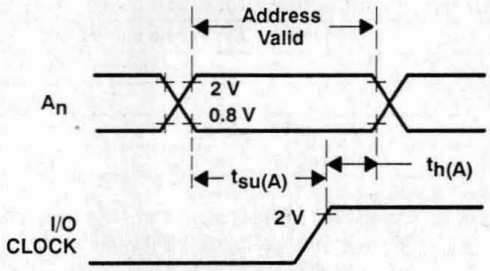


Figure 3. Address Timing

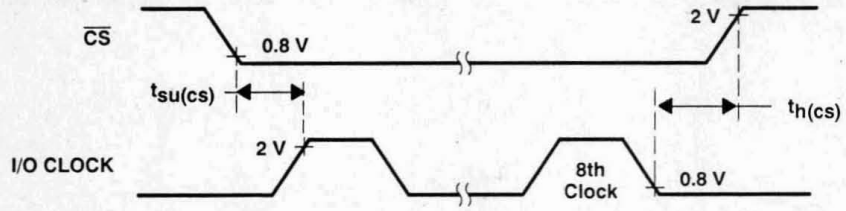


Figure 4. $\overline{CS}$ to I/O CLOCK Timing

PARAMETER MEASUREMENT INFORMATION

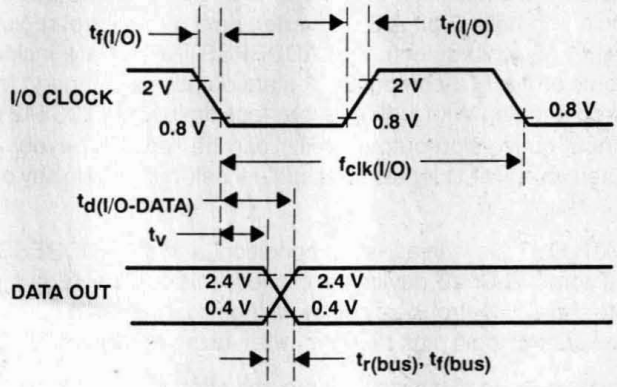


Figure 5. Data Output Timing

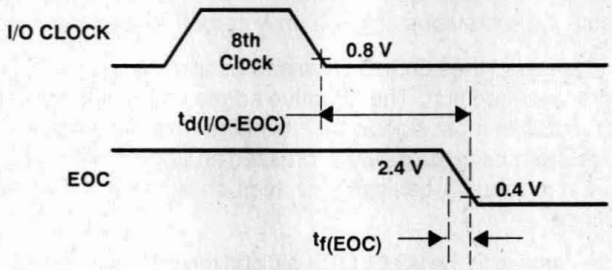


Figure 6. EOC Timing

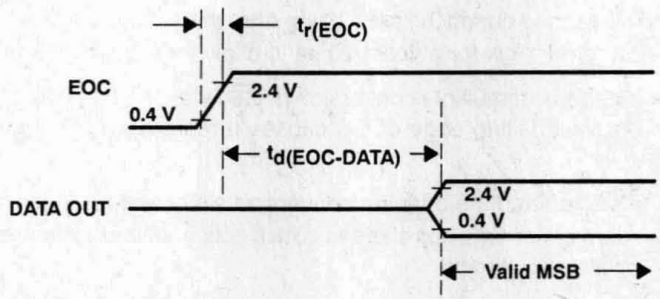


Figure 7. Data Output to EOC Timing

principles of operation

The TLC542 is a complete data acquisition system on a single chip. The device includes such functions as analog multiplexer, sample and hold, 8-bit A/D converter, data and control registers, and control logic. Three control inputs (I/O CLOCK, $\overline{CS}$ (chip select), and ADDRESS INPUT) are included for flexibility and access speed. These control inputs and a TTL-compatible 3-state output are intended for serial communications with a microprocessor or microcomputer. With judicious interface timing, the TLC542 can complete a conversion in 20 μs, while complete input-conversion-output cycles can be repeated every 40 μs. Futhermore, this fast conversion can be executed on any of 11 inputs or its built-in "self-test" and in any order desired by the controlling processor.

When $\overline{CS}$ is high, the DATA OUT pin is in a 3-state condition, and the ADDRESS INPUT and I/O CLOCK pins are disabled. When additional TLC542 devices are used, this feature allows each of these pins, with the exception of the $\overline{CS}$ pin, to share a control logic point with their counterpart pins on additional A/D devices. Thus, this feature minimizes the control logic pins required when using multiple A/D devices.

The control sequence is designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is as follows:

1. $\overline{CS}$ is brought low. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and then a falling edge of the internal system clock before recognizing the low $\overline{CS}$ transition. The MSB of the result of the previous conversion automatically appears on the DATA OUT pin.
2. On the first four rising edges of the I/O CLOCK, a new positive-logic multiplexer address is shifted in, with the MSB of this address shifted first. The negative edges of these four I/O CLOCK pulses shift out the second, third, fourth, and fifth most significant bits of the result of the previous conversion. The on-chip sample and hold begins sampling the newly addressed analog input after the fourth falling edge of the I/O CLOCK. The sampling operation basically involves charging the internal capacitors to the level of the analog input voltage.
3. Three clock cycles are applied to the I/O CLOCK pin and the sixth, seventh, and eighth conversion bits are shifted out on the negative edges of these clock cycles.
4. The final eighth clock cycle is applied to the I/O CLOCK pin. The falling edge of this clock cycle initiates a 12-system clock (≈ 12 μs) additional sampling period while the output is in the high-impedance state. Conversion is then performed during the next 20 μs. After this final I/O CLOCK cycle, $\overline{CS}$ must go high or the I/O CLOCK must remain low for at least 20 μs to allow for the conversion function.

$\overline{CS}$ can be kept low during periods of multiple conversion. If $\overline{CS}$ is taken high, it must remain high until the end of conversion. Otherwise, a valid falling edge of $\overline{CS}$ causes a reset condition, which aborts the conversion process.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 20-μs conversion time has elapsed.. Such action yields the conversion result of the previous conversion and not the ongoing conversion.

The end-of-conversion (EOC) output goes low on the negative edge of the eighth I/O CLOCK. The subsequent low-to-high transition of EOC indicates the A/D conversion is complete and the conversion is ready for transfer.

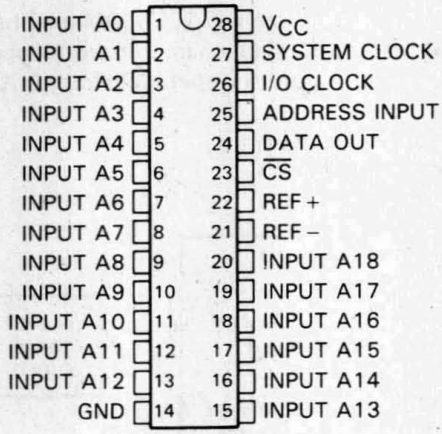
TLC545M, TLC545I, TLC545C, TLC546M, TLC546I, TLC546C
LinCMOS™ 8-BIT ANALOG-TO-DIGITAL PERIPHERALS WITH SERIAL CONTROL AND 19 INPUTS

D2850, DECEMBER 1985—REVISED SEPTEMBER 1988

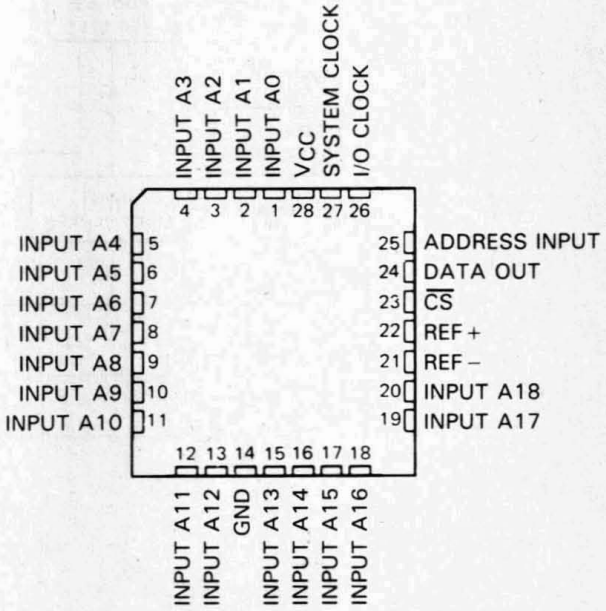
- LinCMOS™ Technology
- 8-Bit Resolution A/D Converter
- Microprocessor Peripheral or Stand-Alone Operation
- On-Chip 20-Channel Analog Multiplexer
- Built-In Self-Test Mode
- Software-Controllable Sample and Hold
- Total Unadjusted Error . . . ±0.5 LSB Max
- Timing and Control Signals Compatible with 8-Bit TLC540 and 10-Bit TLC1540 A/D Converter Families

TYPICAL PERFORMANCE	TL545	TL546
Channel Acquisition Time	1.5 μs	2.7 μs
Conversion Time	9 μs	17 μs
Sampling Rate	76 × 10^3	40 × 10^3
Power Dissipation	6 mW	6 mW

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



FN CHIP CARRIER PACKAGE
(TOP VIEW)



description

The TLC545 and TLC546 are LinCMOS™ A/D peripherals built around an 8-bit switched-capacitor successive-approximation A/D converter. They are designed for serial interface to a microprocessor or peripheral via a 3-state output with up to four control inputs [including independent System Clock, I/O Clock, Chip Select ($\overline{CS}$), and Address Input]. A 4-MHz system clock for the TLC545 and a 2.1-MHz system clock for the TLC546 with a design that includes simultaneous read/write operation allowing high-speed data transfers and sample rates of up to 76,923 samples per second for the TLC545, and 40,000 samples per second for the TLC546. In addition to the high-speed converter and versatile control logic, there is an on-chip 20-channel analog multiplexer that can be used to sample any one of 19 inputs or an internal ''self-test'' voltage, and a sample-and-hold that can operate automatically or under microprocessor control.

The converters incorporated in the TLC545 and TLC546 feature differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and analog circuitry isolation from logic and supply noises. A totally switched-capacitor design allows low-error (±0.5 LSB)

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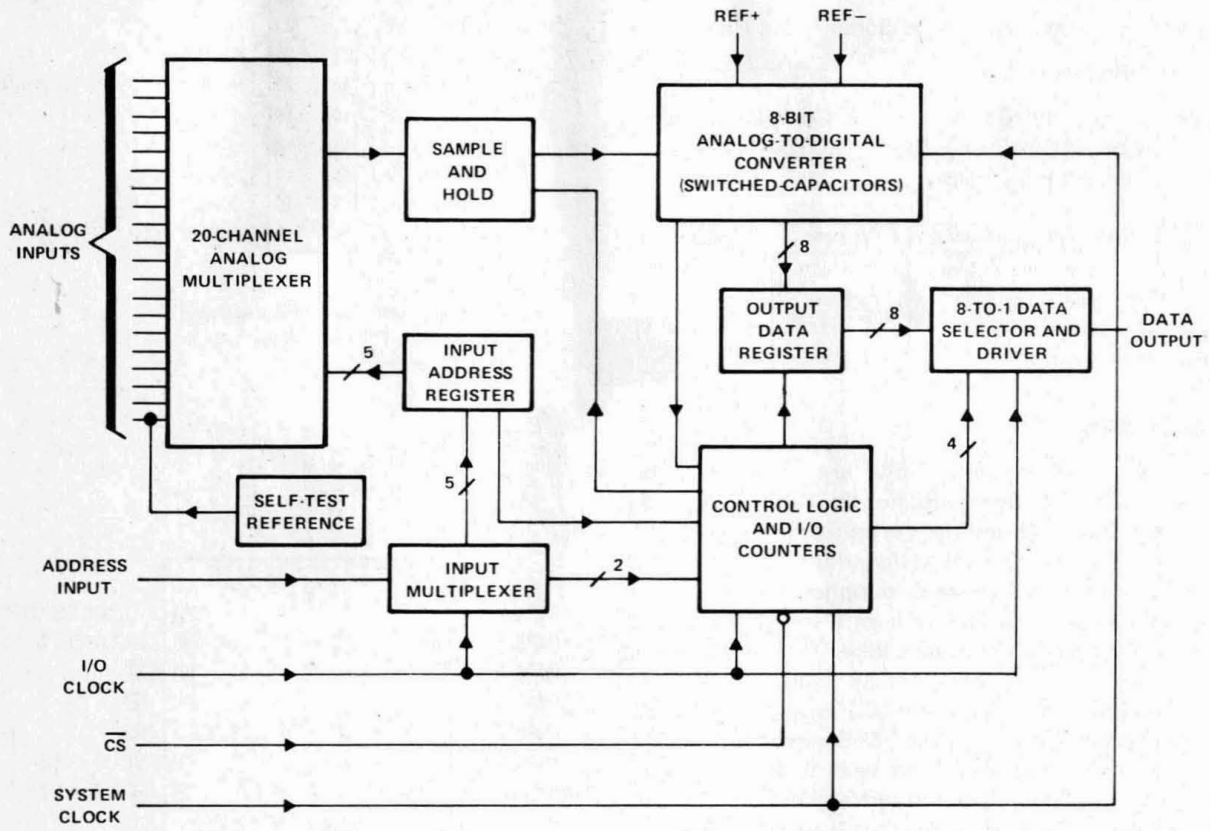
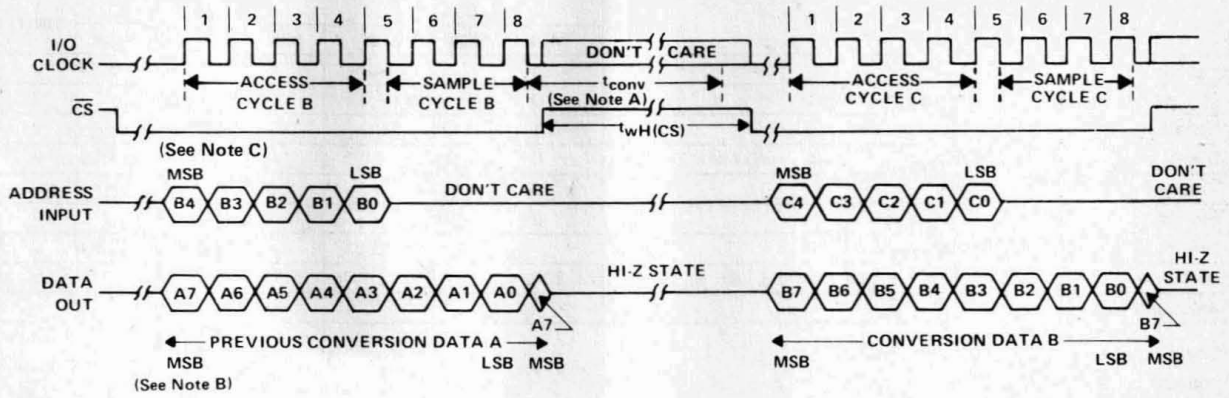
conversion in 9 μs for the TLC545, and 17 μs for the TLC546, over the full operating temperature range. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The TLC545M and the TLC546M are characterized for operation from −55°C to 125°C. The TLC545I and the TLC546I are characterized for operation from −40°C to 85°C. The TLC545C and the TLC546C are characterized for operation from 0°C to 70°C.

functional block diagram



operating sequence



NOTES: A. The conversion cycle, which requires 36 system clock periods, is initiated with the 8th I/O clock↓ after CS↓ for the channel whose address exists in memory at that time.

B. The most significant bit (MSB) will automatically be placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining seven bits (A6-A0) will be clocked out on the first seven I/O clock falling edges.

C. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for three system clock cycles (or less) after a chip select transition before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip-select setup time has elapsed.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range (any input) . . . . . −0.3 V to V_{CC} +0.3 V
Output voltage range . . . . . −0.3 V to V_{CC} +0.3 V
Peak input current range (any input) . . . . . ±10 mA
Peak total input current (all inputs) . . . . . ±30 mA
Operating free-air temperature range: TLC545M, TLC546M . . . . . −55°C to 125°C
TLC545I, TLC546I . . . . . −40°C to 85°C
TLC545C, TLC546C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

			TLC545			TLC546			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.75	5	5.5	4.75	5	5.5	V
Positive reference voltage, V_{ref+} (see Note 3)			0	V_{CC}	$V_{CC}+0.1$	0	V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{ref-} (see Note 2)			−0.1	0	V_{CC}	−0.1	0	V_{CC}	V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)			0	V_{CC}	$V_{CC}+0.2$	0	V_{CC}	$V_{CC}+0.2$	V
Analog input voltage (see Note 2)			0		V_{CC}	0		V_{CC}	V
High-level control input voltage, V_{IH}			2			2			V
Low-level control input voltage, V_{IL}					0.8			0.8	V
Setup time, address bits at data input before I/O CLK↑, $t_{su(A)}$			200			400			ns
Address hold time, t_h			0			0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 3)			3			3			System clock cycles
Chip select high during conversion, $t_{wH(CS)}$			36			36			System clock cycles
Input/Output clock frequency, $f_{CLK(I/O)}$			0		2.048	0		1.1	MHz
System clock frequency, $f_{CLK(SYS)}$			$f_{CLK(I/O)}$		4	$f_{CLK(I/O)}$		2.1	MHz
System clock high, $t_{wH(SYS)}$			110			210			ns
System clock low, $t_{wL(SYS)}$			100			190			ns
Input/Output clock high, $t_{wH(I/O)}$			200			404			ns
Input/Output clock low, $t_{wL(I/O)}$			200			404			ns
Clock transition time (see Note 4)	System	$f_{CLK(SYS)} \le 1048$ kHz			30			30	ns
		$f_{CLK(SYS)} > 1048$ kHz			20			20	
	I/O	$f_{CLK(I/O)} \le 525$ kHz			100			100	ns
		$f_{CLK(I/O)} > 525$ kHz			40			40	
Operating free-air temperature, T_A		TLC545M, TLC546M	−55		125	−55		125	°C
		TLC545I, TLC546I	−40		85	−40		85	
		TLC545C, TLC546C	0		70	0		70	

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all "1"s (11111111), while input voltages less than that applied to REF− convert as all "0"s (00000000). As the differential reference voltage decreases below 4.75 V, the total unadjusted error tends to increase.

3. To minimize errors caused by noise at the Chip Select input, the internal circuitry waits for three system clock cycles (or less) after a chip select falling edge or rising edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip select setup time has elapsed.

4. This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 μs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating temperature range, V_{CC} = V_{ref+} = 4.75 V to 5.5 V (unless otherwise noted), $f_{CLK(I/O)}$ = 2.048 MHz for TLC545 or $f_{CLK(I/O)}$ = 1.1 MHz for TLC546

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (pin 24)		V_{CC} = 4.75 V,	I_{OH} = −360 μA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V,	I_{OL} = 3.2 mA			0.4	V
I_{OZ}	Off-state (high-impedance state) output current		V_O = V_{CC},	$\overline{CS}$ at V_{CC}			10	μA
			V_O = 0,	$\overline{CS}$ at V_{CC}			−10	
I_{IH}	High-level input current		V_I = V_{CC}			0.005	2.5	μA
I_{IL}	Low-level input current		V_I = 0			−0.005	−2.5	μA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			1.2	2.5	mA
	Selected channel leakage current		Selected channel at V_{CC}, Unselected channel at 0 V			0.4	1	μA
			Selected channel at 0 V, Unselected channel at V_{CC}			−0.4	−1	
I_{CC} + I_{ref}	Supply and reference current		V_{ref+} = V_{CC},	$\overline{CS}$ at 0 V		1.3	3	mA
C_i	Input capacitance	Analog inputs				7	55	pF
		Control inputs				5	15	

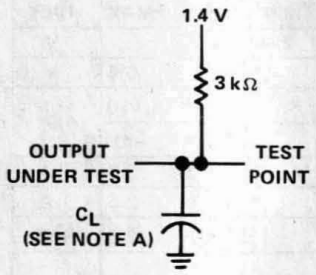
†All typical values are at T_A = 25°C.

operating characteristics over recommended operating free-air temperature range, V_{CC} = V_{ref+} = 4.75 V to 5.5 V, $f_{CLK(I/O)}$ = 2.048 MHz for TLC545 or 1.1 MHz for TLC546, $f_{CLK(SYS)}$ = 4 MHz for TLC545 or 2.1 MHz for TLC546

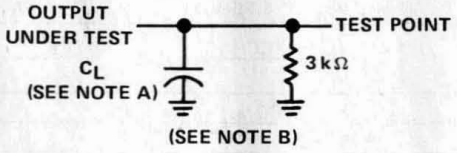
	PARAMETER	TEST CONDITIONS	TLC545			TLC546			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
	Linearity error	See Note 5			±0.5			±0.5	LSB
	Zero error	See Note 6			±0.5			±0.5	LSB
	Full-scale error	See Note 6			±0.5			±0.5	LSB
	Total unadjusted error	See Note 7			±0.5			±0.5	LSB
	Self-test output code	Input A19 address = 10011 (See Note 8)	01111101 (125)		10000011 (131)	01111101 (125)		10000011 (131)	
t_{conv}	Conversion time	See Operating Sequence			9			17	μs
	Total access and conversion time	See Operating Sequence			13			25	μs
t_{acq}	Channel acquisition time (sample cycle)	See Operating Sequence			3			3	I/O clock cycles
t_v	Time output data remains valid after I/O clock↓		10			10			ns
t_d	Delay time, I/O clock↓ to data output valid	See Parameter Measurement Information			300			400	ns
t_{en}	Output enable time				150			150	ns
t_{dis}	Output disable time				150			150	ns
$t_{r(bus)}$	Data bus rise time				300			300	ns
$t_{f(bus)}$	Data bus fall time				300			300	ns

NOTES: 5. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
6. Zero Error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
7. Total unadjusted error is the sum of linearity, zero, and full-scale errors.
8. Both the input address and the output codes are expressed in positive logic. The A19 analog input signal is internally generated and is used for test purposes.

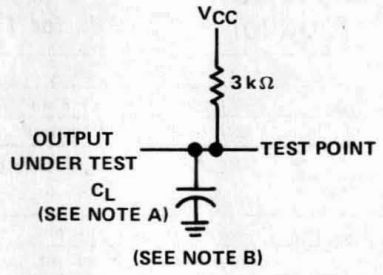
PARAMETER MEASUREMENT INFORMATION



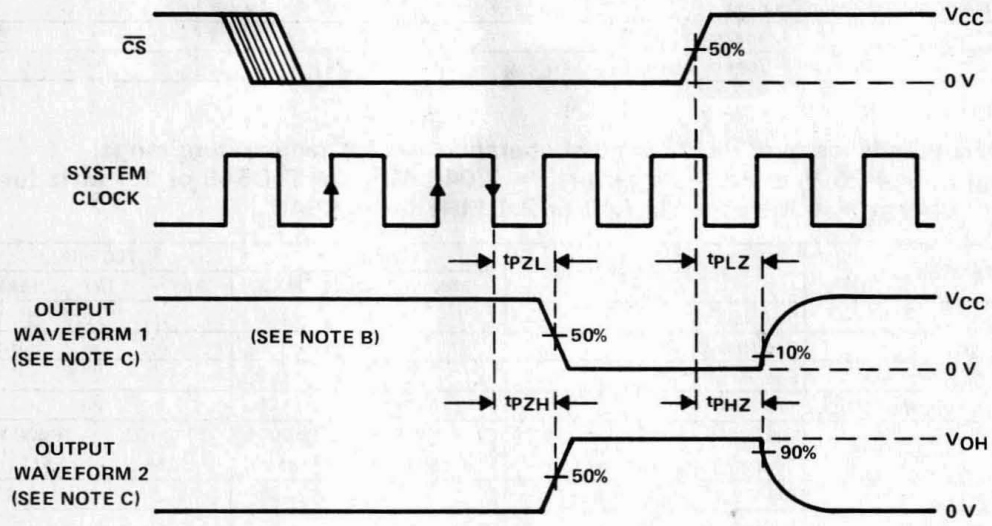
LOAD CIRCUIT FOR t_d, t_r, AND t_f



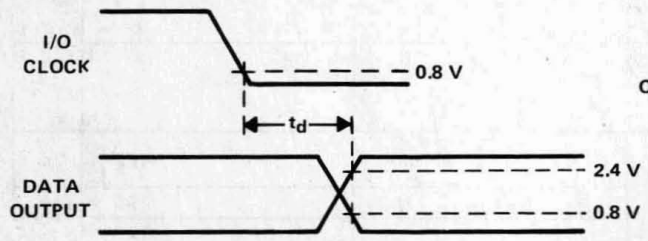
LOAD CIRCUIT FOR t_{PZH} AND t_{PHZ}



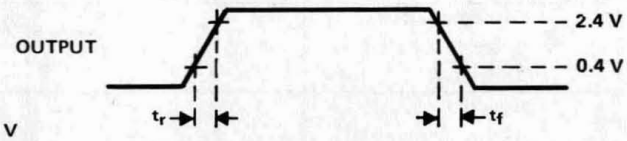
LOAD CIRCUIT FOR t_{PZL} AND t_{PLZ}



VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORM FOR DELAY TIME



VOLTAGE WAVEFORM FOR RISE AND FALL TIMES

NOTES: A. C_L = 50 pF for TLC545 and 100 pF for TLC546
B. t_{en} = t_{PZH} or t_{PZL}, t_{dis} = t_{PHZ} or t_{PLZ}
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

principles of operation

The TLC545 and TLC546 are both complete data acquisition systems on single chips. Each includes such functions as system clock, sample-and-hold, 8-bit A/D converter, data and control registers, and control logic. For flexibility and access speed, there are four control inputs; Chip Select ($\overline{CS}$), Address Input, I/O clock, and System clock. These control inputs and a TTL-compatible 3-state output facilitate serial communications with a microprocessor or microcomputer. The TLC545 and TLC546 can complete conversions in a maximum of 9 and 17 μs respectively, while complete input-conversion-output cycles can be repeated at a maximum of 13 and 25 μs, respectively.

The System and I/O clocks are normally used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Once a clock signal within the specification range is applied to the System clock input, the control hardware and software need only be concerned with addressing the desired analog channel, reading the previous conversion result, and starting the conversion by using the I/O clock. The System clock will drive the "conversion crunching" circuitry so that the control hardware and software need not be concerned with this task.

When $\overline{CS}$ is high, the Data Output pin is in a high-impedance condition, and the Address Input and I/O Clock pins are disabled. This feature allows each of these pins, with the exception of the $\overline{CS}$, to share a control logic point with their counterpart pins on additional A/D devices when additional TLC545/TLC546 devices are used. Thus, the above feature serves to minimize the required control logic pins when using multiple A/D devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. $\overline{CS}$ is brought low. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and then a falling edge of the System clock after a $\overline{CS}$ transition before the transition is recognized. The MSB of the previous conversion result will automatically appear on the Data Out pin.
2. A new positive-logic multiplexer address is shifted in on the first five rising edges of the I/O clock. The MSB of the address is shifted in first. The negative edges of these five I/O clocks shift out the 2nd, 3rd, 4th, 5th, and 6th most significant bits of the previous conversion result. The on-chip sample-and hold begins sampling the newly addressed analog input after the 5th falling edge. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Two clock cycles are then applied to the I/O pin and the 7th and 8th conversion bits are shifted out on the negative edges of these clock cycles.
4. The final 8th clock cycle is applied to the I/O clock pin. The falling edge of this clock cycle completes the analog sampling process and initiates the hold function. Conversion is then performed during the next 36 system clock cycles. After this final I/O clock cycle, $\overline{CS}$ must go high or the I/O clock must remain low for at least 36 system clock cycles to allow for the conversion function.

$\overline{CS}$ can be kept low during periods of multiple conversion. When keeping $\overline{CS}$ low during periods of multiple conversion, special care must be exercised to prevent noise glitches on the I/O Clock line. If glitches occur on the I/O Clock line, the I/O sequence between the microprocessor/controller and the device will lose synchronization. Also, if $\overline{CS}$ is taken high, it must remain high until the end of conversion. Otherwise, a valid falling edge of $\overline{CS}$ will cause a reset condition, which will abort the conversion in progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 36 system clock cycles occur. Such action will yield the conversion result of the previous conversion and not the ongoing conversion.

principles of operation (continued)

It is possible to connect the system and I/O clocks together in special situations in which controlling circuitry points must be minimized. In this case, the following special points must be considered in addition to the requirements of the normal control sequence previously described.

1. When $\overline{CS}$ is recognized by the device to be at a low level, the common clock signal is used as an I/O clock. When the $\overline{CS}$ is recognized by the device to be at a high level, the common clock signal is used to drive the ''conversion crunching'' circuitry.
2. The device will recognize a $\overline{CS}$ transition only when the $\overline{CS}$ input changes and subsequently the system clock pin receives two positive edges and then a negative edge. For this reason, after a $\overline{CS}$ negative edge, the first two clock cycles will not shift in the address because a low $\overline{CS}$ must be recognized before the I/O clock can shift in an analog channel address. Also, upon shifting in the address, $\overline{CS}$ must be raised after the 6th I/O clock, which has been recognized by the device, so that a $\overline{CS}$ low level will be recognized upon the lowering of the 8th I/O clock signal recognized by the device. Otherwise, additional common clock cycles will be recognized as I/O clocks and will shift in an erroneous address.

For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in time. This device will accommodate these applications. Although the on-chip sample-and-hold begins sampling upon the negative edge of the 5th I/O clock cycle, the hold function is not initiated until the negative edge of the 8th I/O clock cycle. Thus, the control circuitry can leave the I/O clock signal in its high state during the 8th I/O clock cycle, until the moment at which the analog signal must be converted. The TLC545/546 will continue sampling the analog input until the 8th falling edge of the I/O clock. The control circuitry or software must then immediately lower the I/O clock signal to initiate the hold function at the desired point in time and to start conversion.

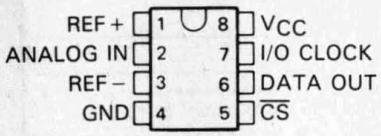
Detailed information on interfacing to most popular microprocesors is readily available from the factory.

TLC548, TLC549
LinCMOS™ 8-BIT ANALOG-TO-DIGITAL PERIPHERAL WITH SERIAL CONTROL

D2816, NOVEMBER 1983—REVISED OCTOBER 1988

- **LinCMOS™ Technology**
- **Microprocessor Peripheral or Stand-Alone Operation**
- **8-Bit Resolution A/D Converter**
- **Differential Reference Input Voltages**
- **Conversion Time . . . 17 μs Max**
- **Total Access and Conversion Cycles Per Second**
  TLC548 . . . up to 45,500
  TLC549 . . . up to 40,000
- **On-Chip Software-Controllable Sample-and-Hold**
- **Total Unadjusted Error . . . ±0.5 LSB Max**
- **4-MHz Typical Internal System Clock**
- **Wide Supply Range . . . 3 V to 6 V**
- **Low Power Consumption . . . 6 mW Typ**
- **Ideal for Cost-Effective, High-Performance Applications Including Battery-Operated Portable Instrumentation**
- **Pinout and Control Signals Compatible with the TLC540 and TLC545 8-Bit A/D Converters and with the TLC1540 10-Bit A/D Converter**

D OR P PACKAGE
(TOP VIEW)



description

The TLC548 and TLC549 are LinCMOS™ A/D peripheral integrated circuits built around an 8-bit switched-capacitor successive-approximation ADC. They are designed for serial interface with a microprocessor or peripheral through a 3-state data output and an analog input. The TLC548 and TLC549 use only the Input/Output Clock (I/O Clock) input along with the Chip Select ($\overline{CS}$) input for data control. The maximum I/O clock input frequency of the TLC548 is guaranteed up to 2.048 MHz, and the I/O clock input frequency of the TLC549 is guaranteed to 1.1 MHz. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

Operation of the TLC548 and the TLC549 is very similar to that of the more complex TLC540 and TLC541 devices; however, the TLC548 and TLC549 provide an on-chip system clock that operates typically at 4 MHz and requires no external components. The on-chip system clock allows internal device operation to proceed independently of serial input/output data timing and permits manipulation of the TLC548 and TLC549 as desired for a wide range of software and hardware requirements. The I/O Clock together with the internal system clock allow high-speed data transfer and conversion rates of 45,500 conversions per second for the TLC548, and 40,000 conversions per second for the TLC549.

Additional TLC548 and TLC549 features include versatile control logic, an on-chip sample-and-hold circuit that can operate automatically or under microprocessor control, and a high-speed converter with differential high-impedance reference voltage inputs that ease ratiometric conversion, scaling, and circuit isolation from logic and supply noises. Design of the totally switched-capacitor successive-approximation converter circuit allows conversion with a maximum total error of ±0.5 least significant bit (LSB) in less than 17 μs.

The TLC548M and TLC549M are characterized for operation over the temperature range of −55°C to 125°C. The TLC548I and TLC549I are characterized for operation from −40°C to 85°C. The TLC548C and TLC549C are characterized for operation from 0°C to 70°C.

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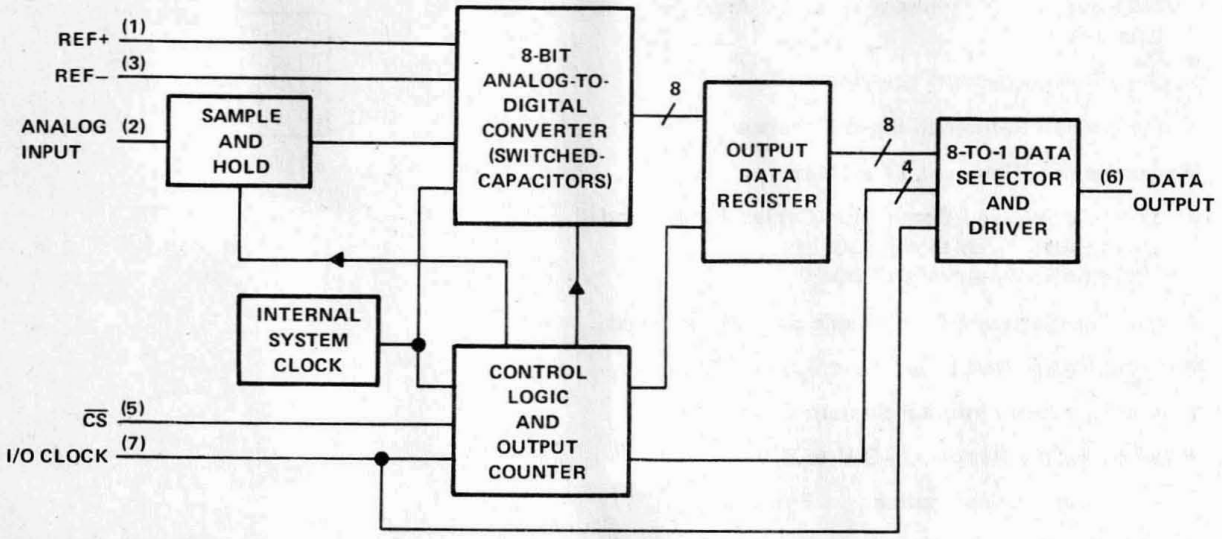
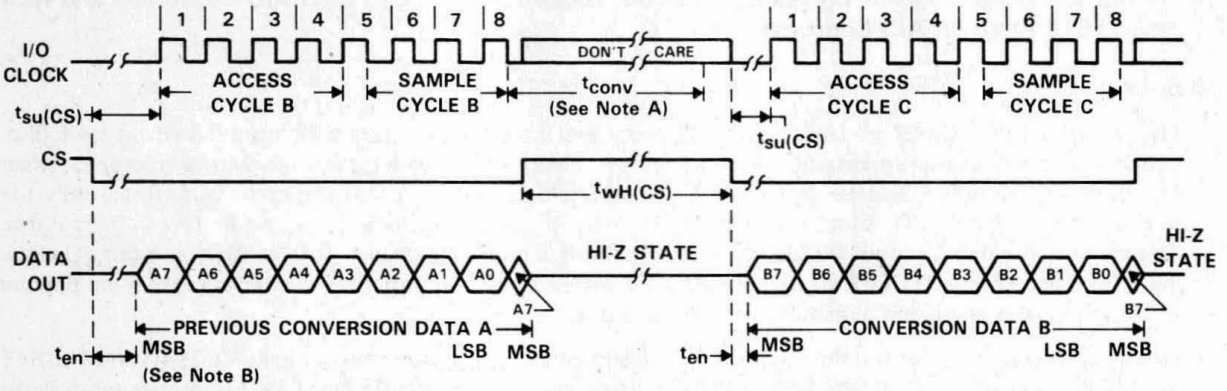
functional block diagram



operating sequence



NOTES: A. The conversion cycle, which requires 36 internal system clock periods (17 μs maximum), is initiated with the 8th I/O clock pulse trailing edge after $\overline{CS}$ goes low for the channel whose address exists in memory at the time.

B. The most significant bit (A7) will automatically be placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining seven bits (A6-A0) will be clocked out on the first seven I/O clock falling edges. B7-B0 will follow in the same manner.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range at any input . . . . . −0.3 V to V_{CC} + 0.3 V
Output voltage range . . . . . −0.3 V to V_{CC} + 0.3 V
Peak input current range (any input) . . . . . ±10 mA
Peak total input current range (all inputs) . . . . . ±30 mA
Operating free-air temperature range (see Note 2): TLC548M, TLC549M . . . . . −55°C to 125°C
TLC548I, TLC549I . . . . . −40°C to 85°C
TLC548C, TLC549C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal with the REF− and GND terminal pins connected together, unless otherwise noted.
2. The D package is not recommended below −40°C.

recommended operating conditions

		TLC548			TLC549			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		3	5	6	3	5	6	V
Positive reference voltage, V_{REF+} (see Note 3)		2.5	V_{CC}	V_{CC}+0.1	2.5	V_{CC}	V_{CC}+0.1	V
Negative reference voltage, V_{REF-} (see Note 3)		−0.1	0	2.5	−0.1	0	2.5	V
Differential reference voltage, V_{REF+}, V_{REF-} (see Note 3)		1	V_{CC}	V_{CC}+0.2	1	V_{CC}	V_{CC}+0.2	V
Analog input voltage (see Note 3)		0		V_{CC}	0		V_{CC}	V
High-level control input voltage, V_{IH} (for V_{CC} = 4.75 V to 5.5 V)		2			2			V
Low-level control input voltage, V_{IL} (for V_{CC} = 4.75 V to 5.5 V)				0.8			0.8	V
Input/output clock frequency, $f_{CLK(I/O)}$ (for V_{CC} = 4.75 V to 5.5 V)		0		2.048	0		1.1	MHz
Input/output clock high, $t_{wH(I/O)}$ (for V_{CC} = 4.75 V to 5.5 V)		200			404			ns
Input/output clock low, $t_{wL(I/O)}$ (for V_{CC} = 4.75 V to 5.5 V)		200			404			ns
Input/output clock transition time, $t_{t(I/O)}$ (see Note 4) (for V_{CC} = 4.75 V to 5.5 V)				100			100	ns
Duration of $\overline{CS}$ input high state during conversion, $t_{wH(CS)}$ (for V_{CC} = 4.75 V to 5.5 V)		17			17			μs
Setup time, $\overline{CS}$ low before first I/O clock, $t_{su(CS)}$ (for V_{CC} = 4.75 V to 5.5 V) (see Note 5)		1.4			1.4			μs
Operating free-air temperature, T_A	TLC548M, TLC549M	−55		125	−55		125	°C
	TLC548I, TLC549I	−40		85	−40		85	
	TLC548C, TLC549C	0		70	0		70	

NOTES: 3. Analog input voltages greater than that applied to REF+ convert to all ones (11111111), while input voltages less than that applied to REF− convert to all zeros (00000000). For proper operation, the positive reference voltage V_{REF+}, must be at least 1 V greater than the negative reference voltage V_{REF-}. In addition, unadjusted errors may increase as the differential reference voltage $V_{REF+} - V_{REF-}$ falls below 4.75 V.
4. This is the time required for the input/output clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 μs for remote data acquisition applications in which the sensor and the ADC are placed several feet away from the controlling microprocessor.
5. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and one falling edge of internal system clock after $\overline{CS}$↓ before responding to control input signals. This $\overline{CS}$ set-up time is given by the t_{en} and $t_{su(CS)}$ specifications.

electrical characteristics over recommended operating free-air temperature range, $V_{CC} = V_{REF+} = 4.75$ V to 5.5 V (unless otherwise noted), $f_{CLK(I/O)} = 2.048$ MHz for TLC548 or 1.1 MHz for TLC549

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = 4.75 V,	I_{OH} = −360 μA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V,	I_{OL} = 3.2 mA			0.4	V
I_{OZ}	Off-state (high-impedance state) output current		$V_O = V_{CC}$,	$\overline{CS}$ at V_{CC}			10	V
			V_O = 0,	$\overline{CS}$ at V_{CC}			−10	
I_{IH}	High-level input current, control inputs		$V_I = V_{CC}$			0.005	2.5	μA
I_{IL}	Low-level input current, control inputs		V_I = 0			−0.005	−2.5	μA
$I_{I(on)}$	Analog channel on-state input current, during sample cycle		Analog input at V_{CC}			0.4	1	μA
			Analog input at 0 V			−0.4	−1	
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			1.8	2.5	mA
$I_{CC}+I_{REF}$	Supply and reference current		$V_{REF+} = V_{CC}$			1.9	3	mA
C_i	Input capacitance	Analog inputs				7	55	pF
		Control inputs				5	15	

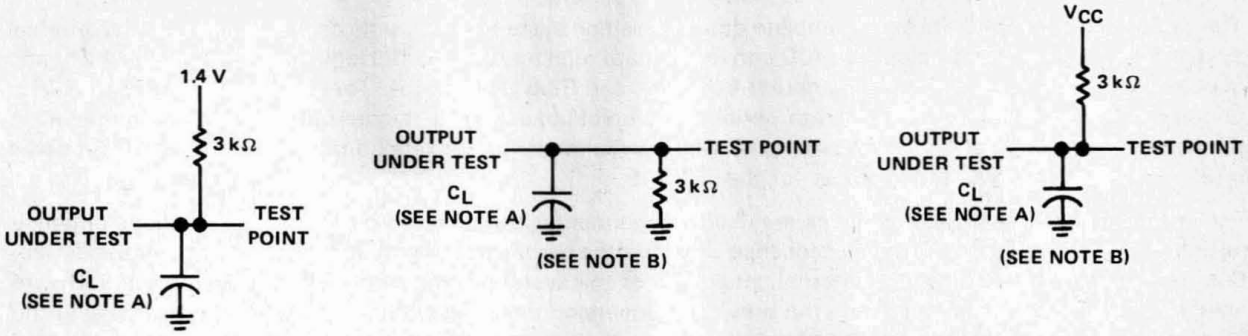
operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{REF+} = 4.75$ V to 5.5 V (unless otherwise noted), $f_{CLK(I/O)} = 2.048$ MHz for TLC548 or 1.1 MHz for TLC549

PARAMETER		TEST CONDITIONS	TLC548			TLC549			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
	Linearity error	See Note 6			±0.5			±0.5	LSB
	Zero error	See Note 7			±0.5			±0.5	LSB
	Full-scale error	See Note 7			±0.5			±0.5	LSB
	Total unadjusted error	See Note 8			±0.5			±0.5	LSB
t_{conv}	Conversion time	See Operating Sequence		8	17		12	17	μs
	Total access and conversion time	See Operating Sequence		12	22		19	25	μs
t_{acq}	Channel acquisition time (sample cycle)	See Operating Sequence			4			4	I/O clock cycles
t_v	Time output data remains valid after I/O clock↓		10			10			ns
t_d	Delay time to data output valid	I/O clock↓			300			400	ns
t_{en}	Output enable time				1.4			1.4	μs
t_{dis}	Output disable time	See Parameter Measurement Information			150			150	ns
$t_{r(bus)}$	Data bus rise time				300			300	ns
$t_{f(bus)}$	Data bus fall time				300			300	ns

†All typicals are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 6. Linearity error is the deviation from the best straight line through the A/D transfer characteristics.
7. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
8. Total unadjusted error is the sum of linearity, zero, and full-scale errors.

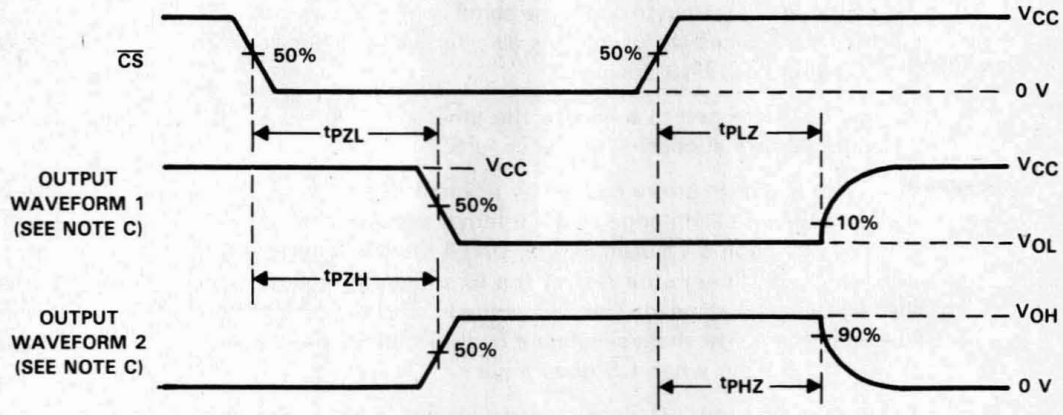
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR t_d, t_r, AND t_f

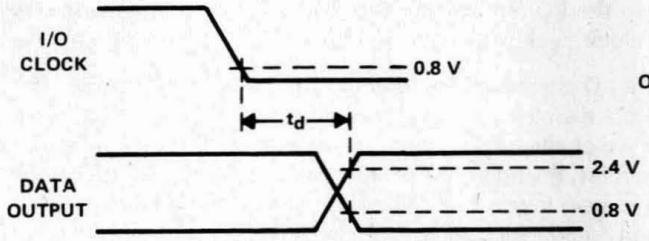
LOAD CIRCUIT FOR t_{PZH} AND t_{PHZ}

LOAD CIRCUIT FOR t_{PZL} AND t_{PLZ}

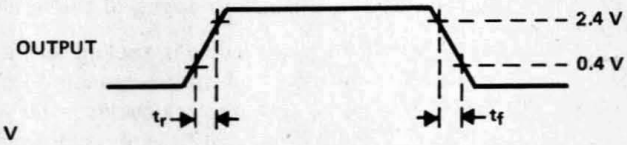


(SEE NOTE B)

VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORM FOR DELAY TIME



VOLTAGE WAVEFORM FOR RISE AND FALL TIMES

NOTES: A. C_L = 50 pF for TLC548 and 100 pF for TLC549; C_L includes jig capacitance.
B. t_{en} = t_{PZH} or t_{PZL}, t_{dis} = t_{PHZ} or t_{PLZ}.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

PRINCIPLES OF OPERATION

The TLC548 and TLC549 are each complete data acquisition systems on a single chip. Each contains an internal system clock, sample-and-hold, 8-bit A/D converter, data register, and control logic circuitry. For flexibility and access speed, there are two control inputs: I/O Clock and Chip Select ($\overline{CS}$). These control inputs and a TTL-compatible three-state output facilitate serial communications with a microprocessor or minicomputer. A conversion can be completed in 17 μs or less, while complete input-conversion-output cycles can be repeated in 22 μs for the TLC548 and in 25 μs for the TLC549.

The internal system clock and I/O clock are used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Due to this independence and the internal generation of the system clock, the control hardware and software need only be concerned with reading the previous conversion result and starting the conversion by using the I/O clock. In this manner, the internal system clock drives the "conversion crunching" circuitry so that the control hardware and software need not be concerned with this task.

When $\overline{CS}$ is high, the data output pin is in a high-impedance condition and the I/O clock pin is disabled. This $\overline{CS}$ control function allows the I/O Clock pin to share the same control logic point with its counterpart pin when additional TLC548 and TLC549 devices are used. This also serves to minimize the required control logic pins when using multiple TLC548 and TLC549 devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. $\overline{CS}$ is brought low. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and then a falling edge of the internal system clock after a $\overline{CS}\downarrow$ before the transition is recognized. However, upon a $\overline{CS}$ rising edge, DATA OUT will go to a high-impedance state within the t_{dis} specification even though the rest of the IC's circuitry will not recognize the transition until the $t_{su(CS)}$ specification has elapsed. This technique is used to protect the device against noise when used in a noisy environment. The most significant bit (MSB) of the previous conversion result will initially appear on the DATA OUT pin when $\overline{CS}$ goes low.
2. The falling edges of the first four I/O clock cycles shift out the 2nd, 3rd, 4th, and 5th most significant bits of the previous conversion result. The on-chip sample-and-hold begins sampling the analog input after the 4th high-to-low transition of the I/O Clock. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Three more I/O clock cycles are then applied to the I/O pin and the 6th, 7th, and 8th conversion bits are shifted out on the falling edges of these clock cycles.
4. The final, (the 8th), clock cycle is applied to the I/O clock pin. The on-chip sample-and-hold begins the hold function upon the high-to-low transition of this clock cycle. The hold function will continue for the next four internal system clock cycles, after which the holding function terminates and the conversion is performed during the next 32 system clock cycles, giving a total of 36 cycles. After the 8th I/O clock cycle, $\overline{CS}$ must go high or the I/O clock must remain low for at least 36 internal system clock cycles to allow for the completion of the hold and conversion functions. $\overline{CS}$ can be kept low during periods of multiple conversion. When keeping $\overline{CS}$ low during periods of multiple conversion, special care must be exercised to prevent noise glitches on the I/O Clock line. If glitches occur on the I/O Clock line, the I/O sequence between the microprocessor/controller and the device will lose synchronization. If $\overline{CS}$ is taken high, it must remain high until the end of conversion. Otherwise, a valid high-to-low transition of $\overline{CS}$ will cause a reset condition, which will abort the conversion in progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 36 internal system clock cycles occur. Such action will yield the conversion result of the previous conversion and not the ongoing conversion.

PRINCIPLES OF OPERATION

For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in time. This device will accommodate these applications. Although the on-chip sample-and-hold begins sampling upon the high-to-low transition of the 4th I/O clock cycle, the hold function does not begin until the high-to-low transition of the 8th I/O clock cycle, which should occur at the moment when the analog signal must be converted. The TLC548 and TLC549 will continue sampling the analog input until the high-to-low transition of the 8th I/O clock pulse. The control circuitry or software will then immediately lower the I/O clock signal and start the holding function to hold the analog signal at the desired point in time and start conversion.

Detailed information on interfacing to the most popular microprocessor is readily available from Texas Instruments.

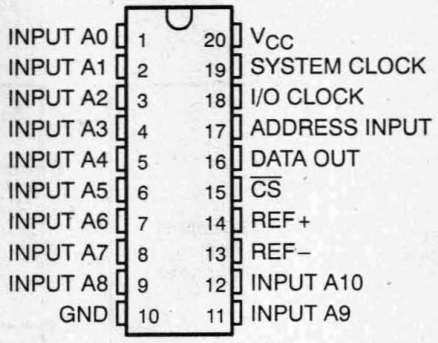
TLC1540C, TLC1540I, TLC1540M, TLC1541C, TLC1541I, TLC1541M
LinCMOS™ 10-BIT ANALOG-TO-DIGITAL PERIPHERALS WITH SERIAL CONTROL AND 11 INPUTS

D2859, DECEMBER 1985–REVISED AUGUST 1991

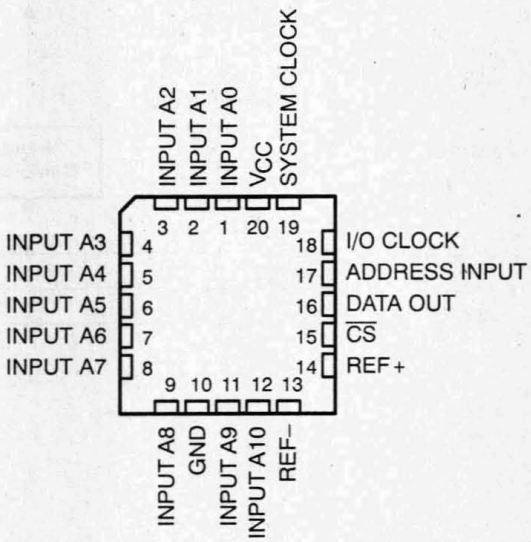
- **LinCMOS™ Technology**
- **10-Bit Resolution A/D Converter**
- **Microprocessor Peripheral or Stand-Alone Operation**
- **On-Chip 12-Channel Analog Multiplexer**
- **Built-In Self-Test Mode**
- **Software-Controllable Sample and Hold**
- **Total Unadjusted Error**
  - **TLC1540: ±0.5 LSB Max**
  - **TLC1541: ±1 LSB Max**
- **Pinout and Control Signals Compatible With TLC540 and TLC549 Families of 8-Bit A/D Converters**

TYPICAL PERFORMANCE	
Channel Acquisition Sample Time	5.5 μs
Conversion Time	21 μs
Samples Per Second	32×10^3
Power Dissipation	6 mW

DW, J, OR N PACKAGE
(TOP VIEW)



FK OR FN PACKAGE
(TOP VIEW)



description

The TLC1540 and TLC1541 are LinCMOS™ A/D peripherals built around a 10-bit, switched-capacitor, successive-approximation A/D converter. They are designed for serial interface to a microprocessor or peripheral via a 3-state output with up to four control inputs [including independent system clock, I/O clock, chip select ($\overline{CS}$), and address input]. A 2.1-MHz system clock for the TLC1540 and TLC1541, with a design that includes simultaneous read/write operation, allows high-speed data transfers and sample rates of up to 32,258 samples per second. In addition to the high-speed converter and versatile control logic, there is an on-chip, 12-channel analog multiplexer that can be used to sample any one of 11 inputs or an internal "self-test" voltage and a sample and hold that can operate automatically or under microprocessor control. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The converters incorporated in the TLC1540 and TLC1541 feature differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and analog circuitry isolation from logic and supply noises. A totally switched-capacitor design allows low-error conversion (±0.5 LSB for the TLC1540, ±1 LSB for the TLC1541) in 21 μs over the full operating temperature range.

The TLC1540 and the TLC1541 are available in DW, FK, FN, J, and N packages. The C-suffix versions are characterized for operation from 0°C to 70°C. The I-suffix versions are characterized for operation from −40°C to 85°C. The M-suffix versions are characterized for operation from −55°C to 125°C.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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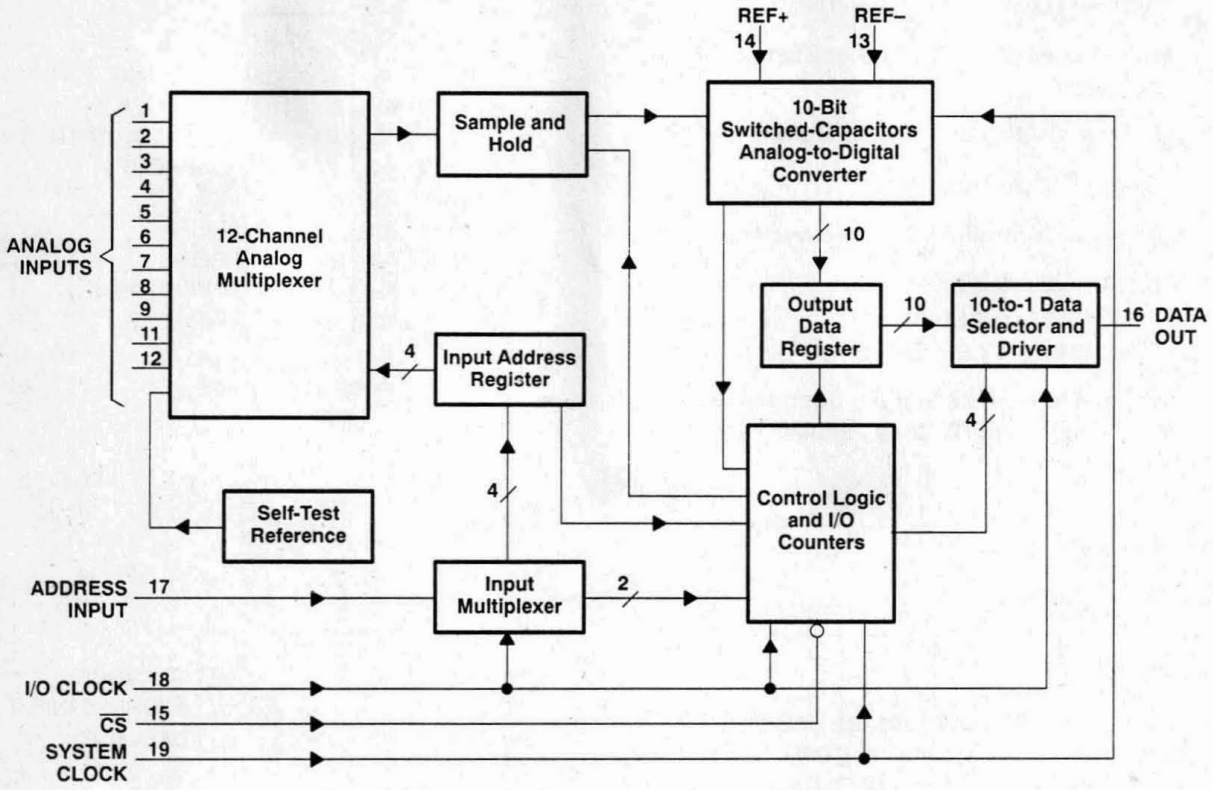
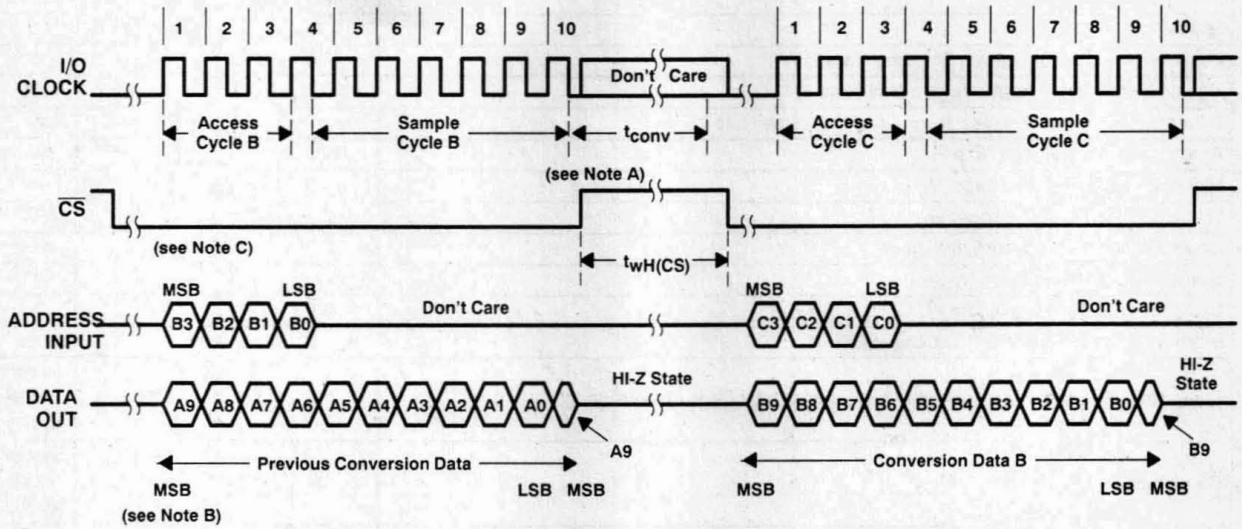
functional block diagram



operating sequence



NOTES: A. The conversion cycle, which requires 44 system clock periods, is initiated on the 10th falling edge of the I/O clock after $\overline{CS}$ goes low for the channel whose address exists in memory at that time. If $\overline{CS}$ is kept low during conversion, the I/O clock must remain low for at least 44 system clock cycles to allow conversion to be completed.

B. The most significant bit (MSB) will automatically be placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining nine bits (A8–A0) will be clocked out on the first nine I/O clock falling edges.

C. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for three system clock cycles (or less) after a chip-select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip-select setup time has elapsed.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	6.5 V
Input voltage range (any input)	−0.3 V to V_{CC} + 0.3 V
Output voltage range	−0.3 V to V_{CC} + 0.3 V
Peak input current (any input)	±10 mA
Peak total input current (all inputs)	±30 mA
Operating free-air temperature range: TLC1540C, TLC1541C	0°C to 70°C
TLC1540I, TLC1541I	−40°C to 85°C
TLC1540M, TLC1541M	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J package	300°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to digital ground with REF− and GND wired together (unless otherwise noted).

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}			4.75	5	5.5	V
Positive reference voltage, V_{REF+} (see Note 2)			2.5	V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{REF-} (see Note 2)			−0.1	0	2.5	V
Differential reference voltage, $V_{REF+} - V_{REF-}$ (see Note 2)			1	V_{CC}	$V_{CC}+0.2$	V
Analog input voltage (see Note 2)			0		V_{CC}	V
High-level control input voltage, V_{IH}			2			V
Low-level control input voltage, V_{IL}					0.8	V
Input/Output clock frequency, $f_{CLK(I/O)}$			0		1.1	MHz
System clock frequency, $f_{CLK(SYS)}$			$f_{CLK(I/O)}$		2.1	MHz
Setup time, address bits before I/O CLK↑, $t_{su(A)}$			400			ns
Hold time, address bits after I/O CLK↑, $t_{h(A)}$			0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 3)			3			System clock cycles
$\overline{CS}$ high during conversion, $t_{wH(CS)}$			44			System clock cycles
System clock high, $t_{wH(SYS)}$			210			ns
System clock low, $t_{wL(SYS)}$			190			ns
Input/Output clock high, $t_{wH(I/O)}$			404			ns
Input/Output clock low, $t_{wL(I/O)}$			404			ns
Clock transition time (see Note 4)	System	$f_{CLK(SYS)} \le 1048$ kHz			30	ns
		$f_{CLK(SYS)} > 1048$ kHz			20	
	I/O	$f_{CLK(I/O)} \le 525$ kHz			100	ns
		$f_{CLK(I/O)} > 525$ kHz			40	
Operating free-air temperature, T_A		TLC1540C, TLC1541C	0		70	°C
		TLC1540I, TLC1541I	−40		85	
		TLC1540M, TLC1541M	−55		125	

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all "1"s (1111111111), while input voltages less than that applied to REF− convert as all "0"s (0000000000). For proper operation, REF+ voltage must be at least 1 V higher than REF− voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.

3. To minimize errors caused by noise at the chip select input, the internal circuitry waits for three system clock cycles (or less) after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum chip select setup time has elapsed.

4. This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 µs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating temperature range, V_{CC} = V_{REF+} = 4.75 V to 5.5 V (unless otherwise noted), $f_{CLK(I/O)}$ = 1.1 MHz, $f_{CLK(SYS)}$ = 2.1 MHz

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (pin 16)		V_{CC} = 4.75 V, I_{OH} = 360 μA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V, I_{OL} = 3.2 mA			0.4	V
I_{OZ}	Off-state (high-impedance state) output current		V_O = V_{CC}, $\overline{CS}$ at V_{CC}			10	μA
			V_O = 0, $\overline{CS}$ at V_{CC}			−10	
I_{IH}	High-level input current		V_I = V_{CC}		0.005	2.5	μA
I_{IL}	Low-level input current		V_I = 0		−0.005	−2.5	μA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V		1.2	2.5	mA
	Selected channel leakage current		Selected channel at V_{CC}, Unselected channel at 0 V		0.4	1	μA
			Selected channel at 0 V, Unselected channel at V_{CC}		−0.4	−1	
I_{CC} + I_{REF}	Supply and reference current		V_{REF+} = V_{CC}, $\overline{CS}$ at 0 V		1.3	3	mA
C_i	Input capacitance	Analog inputs			7	55	pF
		Control inputs			5	15	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

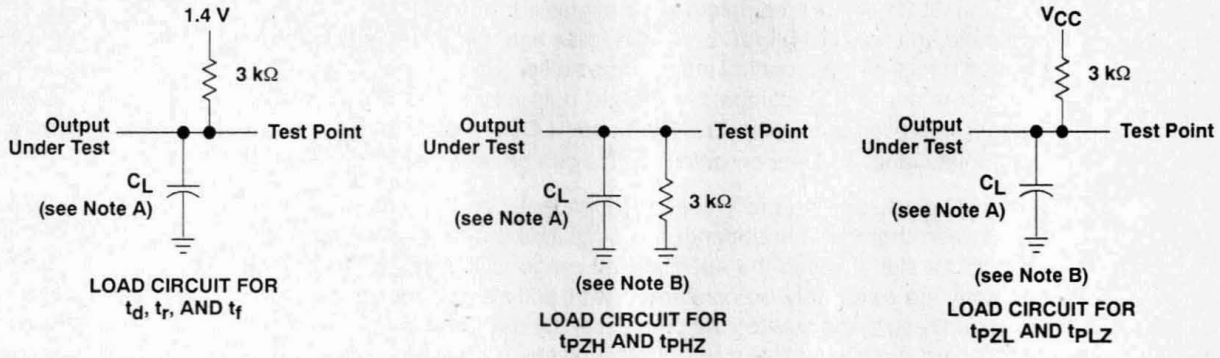
operating characteristics over recommended operating temperature range, $V_{CC} = V_{REF+} = 4.75$ V to 5.5 V, $f_{CLK(I/O)} = 1.1$ MHz, $f_{CLK(SYS)} = 2.1$ MHz

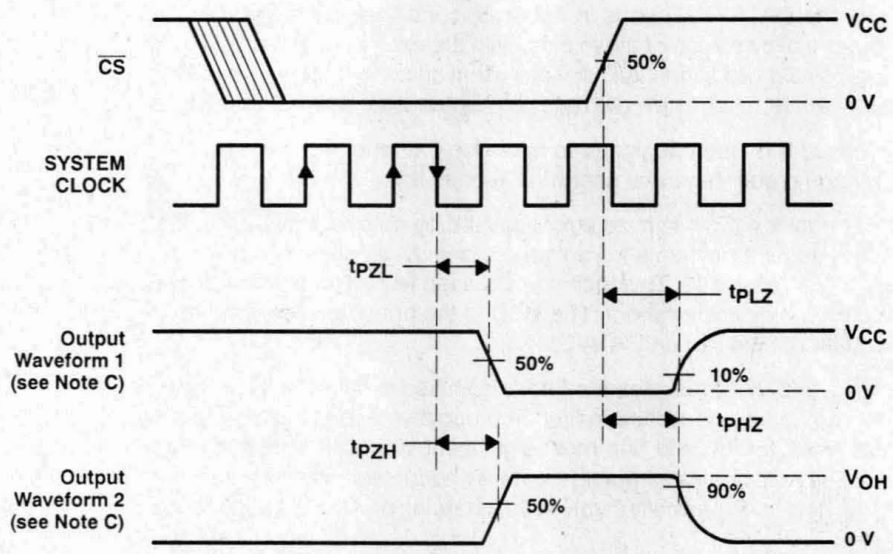
PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
	Linearity error	TLC1540	See Note 5		±0.5	LSB
		TLC1541			±1	
	Zero error	TLC1540	See Notes 2 and 6		±0.5	LSB
		TLC1541			±1	
	Full-scale error	TLC1540	See Notes 2 and 6		±0.5	LSB
		TLC1541			±1	
	Total unadjusted error	TLC1540	See Note 7		±0.5	LSB
		TLC1541			±1	
	Self-test output code		Input A11 address = 1011 (See Note 8)	0111110100 (500)	1000001100 (524)	
t_{conv}	Conversion time		See Operating Sequence		21	µs
	Total access and conversion time		See Operating Sequence		31	µs
t_{acq}	Channel acquisition time (sample cycle)		See Operating Sequence		6	I/O clock cycles
t_v	Time output data remains valid after I/O clock↓			10		ns
t_d	Delay time, I/O clock↓ to data output valid		See Parameter Measurement Information		400	ns
t_{en}	Output enable time				150	ns
t_{dis}	Output disable time				150	ns
$t_{r(bus)}$	Data bus rise time				300	ns
$t_{f(bus)}$	Data bus fall time				300	ns

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all "1"s (1111111111), while input voltages less than that applied to REF– convert as all "0"s (0000000000). For proper operation, REF+ voltage must be at least 1 V higher than REF– voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.

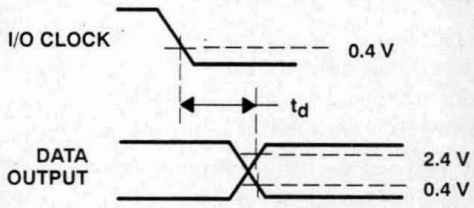
5. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
6. Zero error is the difference between 0000000000 and the converted output for zero input voltage; full-scale error is the difference between 1111111111 and the converted output for full-scale input voltage.
7. Total unadjusted error comprises linearity, zero, and full-scale errors.
8. Both the input address and the output codes are expressed in positive logic. The A11 analog input signal is internally generated and is used for test purposes.

PARAMETER MEASUREMENT INFORMATION

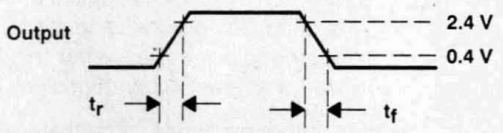




VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS FOR DELAY TIME



VOLTAGE WAVEFORMS FOR RISE AND FALL TIMES

NOTES: A. C_L = 50 pF
B. t_{en} = t_{PZH} or t_{PZL}, t_{dis} = t_{PHZ} or t_{PLZ}.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

principles of operation

The TLC1540 and TLC1541 are complete data acquisition systems on single chips. Each includes such functions as sample and hold, 10-bit A/D converter, data and control registers, and control logic. For flexibility and access speed, there are four control inputs: chip select ($\overline{CS}$), address input, I/O clock, and system clock. These control inputs and a TTL-compatible 3-state output are intended for serial communications with a microprocessor or microcomputer. The TLC1540 and TLC1541 can complete conversions in a maximum of 21 μs, while complete input-conversion-output cycles can be repeated at a maximum of 31 μs.

The system and I/O clocks are normally used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Once a clock signal within the specification range is applied to the system clock input, the control hardware and software need only be concerned with addressing the desired analog channel, reading the previous conversion result, and starting the conversion by using the I/O clock. The system clock will drive the "conversion crunching" circuitry so that the control hardware and software need not be concerned with this task.

When $\overline{CS}$ is high, the DATA OUT pin is in a 3-state condition and the address input and I/O clock pins are disabled. This feature allows each of these pins, with the exception of the $\overline{CS}$ pin, to share a control logic point with its counterpart pins on additional A/D devices when additional TLC1540/1541 devices are used. In this way, the above feature serves to minimize the required control logic pins when using multiple A/D devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. $\overline{CS}$ is brought low. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and then a falling edge of the system clock after a low $\overline{CS}$ transition before the low transition is recognized. This technique is used to protect the device against noise when the device is used in a noisy environment. The MSB of the previous conversion result will automatically appear on the data out pin (or "on DATA OUT").
2. A new positive-logic multiplexer address is shifted in on the first four rising edges of the I/O clock. The MSB of the address is shifted in first. The negative edges of these four I/O clock pulses shift out the second, third, fourth, and fifth most significant bits of the previous conversion result. The on-chip sample and hold begins sampling the newly addressed analog input after the fourth falling edge. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Five clock cycles are then applied to the I/O pin, and the sixth, seventh, eighth, ninth, and tenth conversion bits are shifted out on the negative edges of these clock cycles.
4. The final tenth clock cycle is applied to the I/O clock pin. The falling edge of this clock cycle completes the analog sampling process and initiates the hold function. Conversion is then performed during the next 44 system clock cycles. After this final I/O clock cycle, $\overline{CS}$ must go high or the I/O clock must remain low for at least 44 system clock cycles to allow for the conversion function.

$\overline{CS}$ can be kept low during periods of multiple conversion. When keeping $\overline{CS}$ low during periods of multiple conversion, special care must be exercised to prevent noise glitches on the I/O clock line. If glitches occur on the I/O clock line, the I/O sequence between the microprocessor/controller and the device will lose synchronization. Also, if $\overline{CS}$ is taken high, it must remain high until the end of the conversion. Otherwise, a valid falling edge of $\overline{CS}$ will cause a reset condition, which will abort the conversion in progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 44 system clock cycles occur. Such action will yield the conversion result of the previous conversion and not the ongoing conversion.

principles of operation (continued)

It is possible to connect the system and I/O clock pins together in special situations in which controlling circuitry points must be minimized. In this case, the following special points must be considered in addition to the requirements of the normal control sequence previously described.

1. When $\overline{CS}$ is recognized by the device to be at a low level, the common clock signal is used as an I/O clock. When $\overline{CS}$ is recognized by the device to be at a high level, the common clock signal is used to drive the "conversion crunching" circuitry.
2. The device will recognize a $\overline{CS}$ low transition only when the $\overline{CS}$ input changes and the system clock pin subsequently receives two positive edges and then a negative edge. For this reason, after a $\overline{CS}$ negative edge, the first two clock cycles will not shift in the address because a low $\overline{CS}$ must be recognized before the I/O clock can shift in an analog channel address. Also, upon shifting in the address, $\overline{CS}$ must go high after the eighth I/O clock that has been recognized by the device so that a $\overline{CS}$ low level will be recognized on the falling edge of the tenth I/O clock signal that is recognized by the device. Otherwise, additional common clock cycles will be recognized as I/O clock pulses and will shift in an erroneous address.

For certain applications, such as strobing, it is necessary to start conversion at a specific point in time. This device will accommodate these applications. Although the on-chip sample and hold begins sampling upon the falling edge of the fourth I/O clock cycle, the hold function is not initiated until the fallling edge of the tenth I/O clock cycle. Thus, the control circuitry can leave the I/O clock signal in its high state during the tenth I/O clock cycle until the moment at which the analog signal must be converted. The TLC1540/TLC1541 will continue sampling the analog input until the tenth falling edge of the I/O clock. The control circuitry or software will then immediately lower the I/O clock signal and hold the analog signal at the desired point in time and start conversion.

Detailed information on interfacing to most popular microprocessors is readily available from the factory.

General Information 1
General Purpose ADCs 2
General Purpose DACs 3
Video and High-Speed ADCs and DACs 4
DSP Analog Interface and Conversion 5
Video Interface Palettes 6
Analog Switches 7
Filters 8
Data Manuals 9
Application Reports 10
Mechanical Data 11

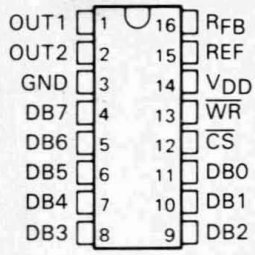
AD7524
Advanced LinCMOS™ 8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

D3100, APRIL 1988

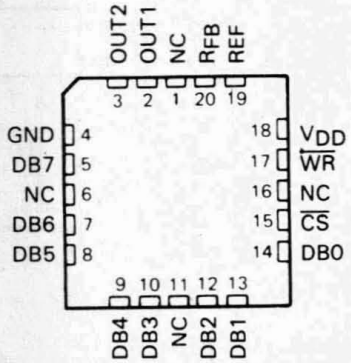
- **Advanced LinCMOS™ Silicon-Gate Technology**
- **Easily Interfaced to Microprocessors**
- **On-Chip Data Latches**
- **Monotonicity Over Entire A/D Conversion Range**
- **Segmented High-Order Bits Ensure Low-Glitch Output**
- **Designed to be Interchangeable with Analog Devices AD7524, PMI PM-7524, and Micro Power Systems MP7524**
- **Fast Control Signaling for Digital Signal Processor Applications Including Interface with TMS320**

KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 Bits
Linearity error	½ LSB Max
Power dissipation at V_{DD} = 5 V	5 mW Max
Settling time	100 ns Max
Propagation delay	80 ns Max

N PACKAGE
(TOP VIEW)



AD7524J . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

The AD7524 is an Advanced LinCMOS™ 8-bit digital-to-analog converter (DAC) designed for easy interface to most popular microprocessors.

The AD7524 is an 8-bit multiplying DAC with input latches and with a load cycle similar to the "write" cycle of a random access memory. Segmenting the high-order bits minimizes glitches during changes in the most-significant bits, which produce the highest glitch impulse. The AD7524 provides accuracy to ½ LSB without the need for thin-film resistors or laser trimming, while dissipating less than 5 mW typically.

Featuring operation from a 5-V to 15-V single supply, the AD7524 interfaces easily to most microprocessor buses or output ports. Excellent multiplying (2 or 4 quadrant) makes the AD7524 an ideal choice for many microprocessor-controlled gain-setting and signal-control applications.

The AD7524A is characterized for operation from −25°C to 85°C, and the AD7524J is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING TEMPERATURE RANGE
DEVICE	PACKAGE SUFFIXES	
AD7524A	N	−25°C to 85°C
AD7524J	N, FN	0°C to 70°C

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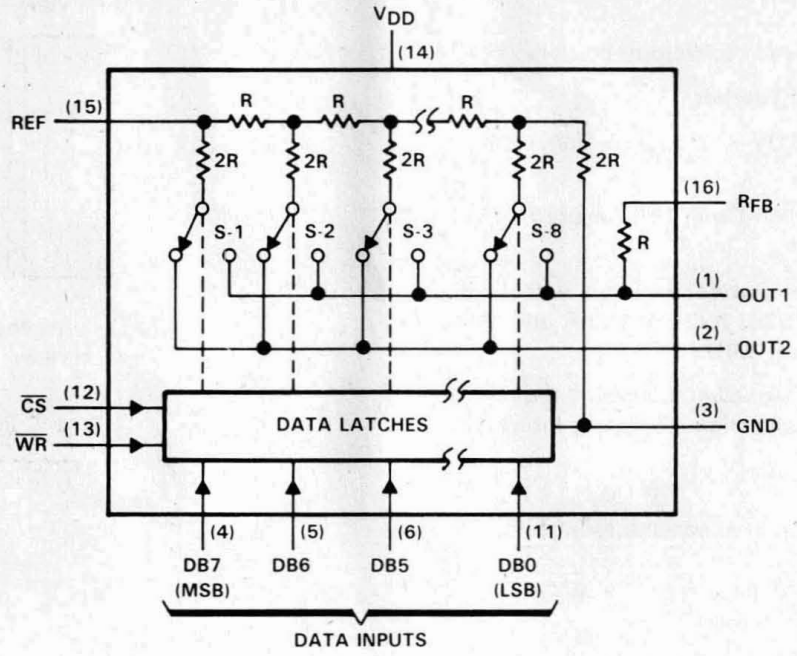
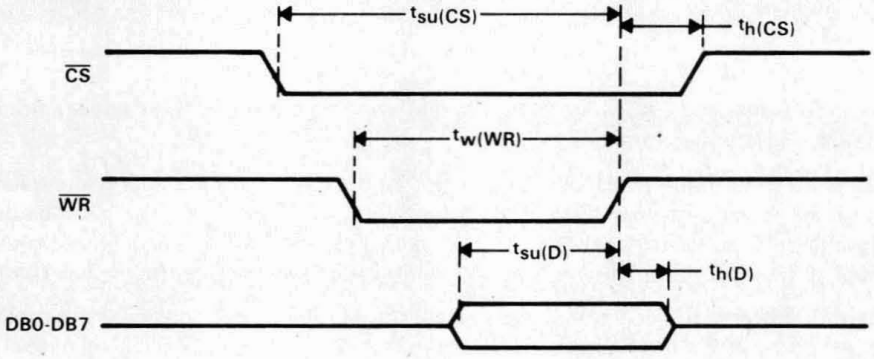
functional block diagram



operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD}	−0.3 V to 17 V
Voltage between R_{FB} and GND	±25 V
Digital input voltage, V_I	−0.3 V to V_{DD} + 0.3 V
Reference voltage, V_{ref}	±25 V
Peak digital input current, I_I	10 μA
Operating free-air temperature range: AD7524A	−25°C to 85°C
AD7524J	0°C to 70°C
Storage temperature range	−65°C to 150°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package	260°C

recommended operating conditions

		V_{DD} = 5 V			V_{DD} = 15 V			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4.75	5	5.25	14.5	15	15.5	V
Reference voltage, V_{ref}			±10			±10		V
High-level input voltage, V_{IH}		2.4			13.5			V
Low-level input voltage, V_{IL}				0.8			1.5	V
$\overline{CS}$ setup time, $t_{su(CS)}$		40			40			ns
$\overline{CS}$ hold time, $t_{h(CS)}$		0			0			ns
Data bus input setup time, $t_{su(D)}$		25			25			ns
Data bus input hold time, $t_{h(D)}$		10			10			ns
Pulse duration, $\overline{WR}$ low, $t_{w(WR)}$		40			40			ns
Operating free-air temperature, T_A	AD7524A	−25		85	−25		85	°C
	AD7524J	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range, V_{ref} = 10 V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER			TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{IH}	High-level input current		$V_I = V_{DD}$	Full range			10			10	μA
				25°C			1			1	
I_{IL}	Low-level input current		V_I = 0	Full range			−10			−10	μA
				25°C			−1			−1	
I_{lkg}	Output leakage current	OUT1	DB0-DB7 at 0, $\overline{WR}$ and $\overline{CS}$ at 0 V, V_{ref} = ±10 V	Full range			±400			±200	nA
				25°C			±50			±50	
		OUT2	DB0-DB7 at V_{DD}, $\overline{WR}$ and $\overline{CS}$ at 0 V, V_{ref} = ±10 V	Full range			±400			±200	
				25°C			±50			±50	
I_{DD}	Supply current	Quiescent	DB0-DB7 at V_{IH}min or V_{IL}max	Full range			2			2	mA
				25°C			1			2	
		Standby	DB0-DB7 at 0 V or V_{DD}	Full range			500			500	μA
				25°C			100			100	
k_{SVS}	Supply voltage sensitivity, $\Delta gain/\Delta V_{DD}$		ΔV_{DD} = 10%	Full range		0.01	0.16		0.005	0.04	%/%
				25°C		0.002	0.08		0.001	0.02	
C_i	Input capacitance, DB0-DB7, $\overline{WR}$, $\overline{CS}$		V_I = 0				5			5	pF
C_o	Output capacitance	OUT1	DB0-DB7 at 0, $\overline{WR}$ and $\overline{CS}$ at 0 V				30			30	pF
		OUT2					120			120	
		OUT1	DB0-DB7 at V_{DD}, $\overline{WR}$ and $\overline{CS}$ at 0 V				120			120	
		OUT2					30			30	
	Reference input impedance (REF to GND)				5		20	5		20	kΩ

operating characteristics over recommended operating free-air temperature range, V_{ref} = 10 V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC} = 5 V		V_{DD} = 15 V		UNIT
			MIN	MAX	MIN	MAX	
Linearity error				±0.2		±0.2	%FSR
Gain error	See Note 1	Full range		±1.4		±0.6	%FSR
		25°C		±1		±0.5	
Settling time (to 1/2 LSB)	See Note 2			100		100	ns
Propagation delay from digital input to 90% of final analog output current	See Note 2			80		80	ns
Feedthrough at OUT1 or OUT2	V_{ref} = ±10 V (100 kHz sinewave), $\overline{WR}$ and $\overline{CS}$ at 0, DB0-DB7 at 0	Full range		0.5		0.5	%FSR
		25°C		0.25		0.25	
Temperature coefficient of gain	T_A = 25°C to t_{min} or t_{max}			±0.004		±0.001	%FSR/°C

NOTES: 1. Gain error is measured using the internal feedback resistor. Nominal Full Scale Range (FSR) = V_{ref} − 1 LSB.
2. OUT1 load = 100 Ω, C_{ext} = 13 pF, $\overline{WR}$ at 0 V, $\overline{CS}$ at 0 V, DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.

PRINCIPLES OF OPERATION

The AD7524 is an 8-bit multiplying D/A converter consisting of an inverted R-2R ladder, analog switches, and data input latches. Binary weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state. The high-order bits are decoded and these decoded bits, through a modification in the R-2R ladder, control three equally weighted current sources. Most applications only require the addition of an external operational amplifier and a voltage reference.

The equivalent circuit for all digital inputs low is seen in Figure 1. With all digital inputs low, the entire reference current, I_{ref}, is switched to OUT2. The current source I/256 represents the constant current flowing through the termination resistor of the R-2R ladder, while the current source I_{lkg} represents leakage currents to the substrate. The capacitances appearing at OUT1 and OUT2 are dependent upon the digital input code. With all digital inputs high, the off-state switch capacitance (30 pF maximum) appears at OUT2 and the on-state switch capacitance (120 pF maximum) appears at OUT1. With all digital inputs low, the situation is reversed as shown in Figure 1. Analysis of the circuit for all digital inputs high is similar to Figure 1; however, in this case, I_{ref} would be switched to OUT1.

Interfacing the AD7524 D/A converter to a microprocessor is accomplished via the data bus and the $\overline{CS}$ and $\overline{WR}$ control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, the AD7524 analog output responds to the data activity on the DB0-DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the $\overline{CS}$ signal or $\overline{WR}$ signal goes high, the data on the DB0-DB7 inputs are latched until the $\overline{CS}$ and $\overline{WR}$ signals go low again. When $\overline{CS}$ is high, the data inputs are disabled regardless of the state of the $\overline{WR}$ signal.

The AD7524 is capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant or 4-quadrant multiplication are shown in Figures 2 and 3. Input coding for unipolar and bipolar operation are summarized in Tables 1 and 2, respectively.

PRINCIPLES OF OPERATION

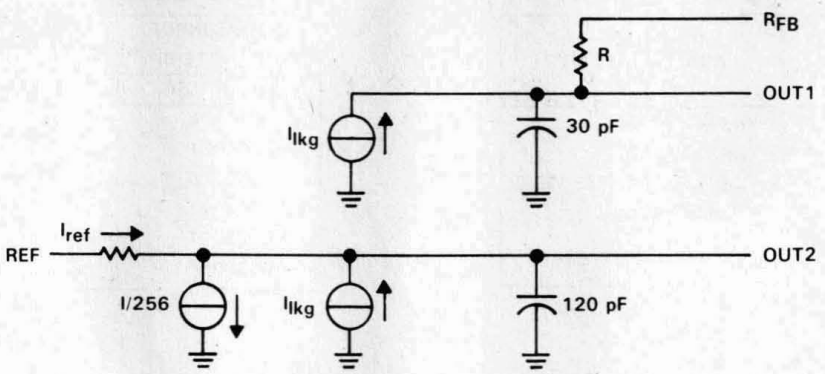


FIGURE 1. AD7524 EQUIVALENT CIRCUIT WITH ALL DIGITAL INPUTS LOW

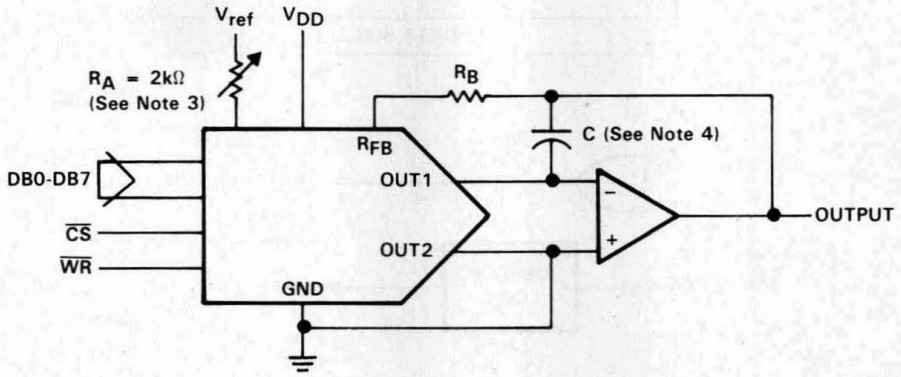


FIGURE 2. UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)

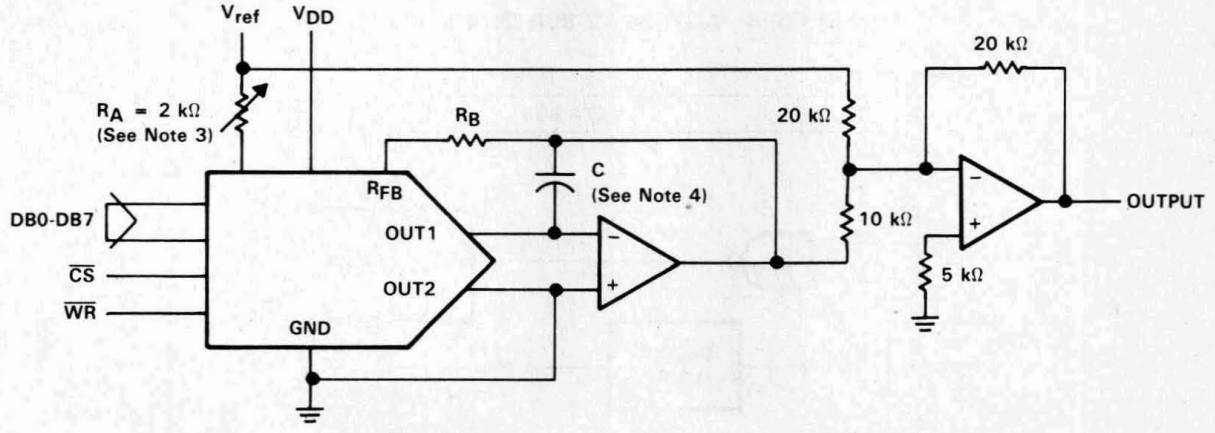


FIGURE 3. BIPOLAR OPERATION (4-QUADRANT OPERATION)

NOTES: 3. R_A and R_B used only if gain adjustment is required.
4. C phase compensation (10-15 pF) is required when using high-speed amplifiers to prevent ringing or oscillation.

PRINCIPLES OF OPERATION

Table 1. Unipolar Binary Code

DIGITAL INPUT (SEE NOTE 5) MSB LSB	ANALOG OUTPUT
11111111	$-V_{ref}$ (255/256)
10000001	$-V_{ref}$ (129/256)
10000000	$-V_{ref}$ (128/256) = $-V_{ref}/2$
01111111	$-V_{ref}$ (127/256)
00000001	$-V_{ref}$ (1/256)
00000000	0

Table 2. Bipolar (Offset Binary) Code

DIGITAL INPUT (SEE NOTE 6) MSB LSB	ANALOG OUTPUT
11111111	V_{ref} (127/128)
10000001	V_{ref} (1/128)
10000000	0
01111111	$-V_{ref}$ (1/128)
00000001	$-V_{ref}$ (127/128)
00000000	$-V_{ref}$

NOTES: 5. LSB = 1/256 (V_{ref}).
6. LSB = 1/128 (V_{ref}).

microprocessor interfaces

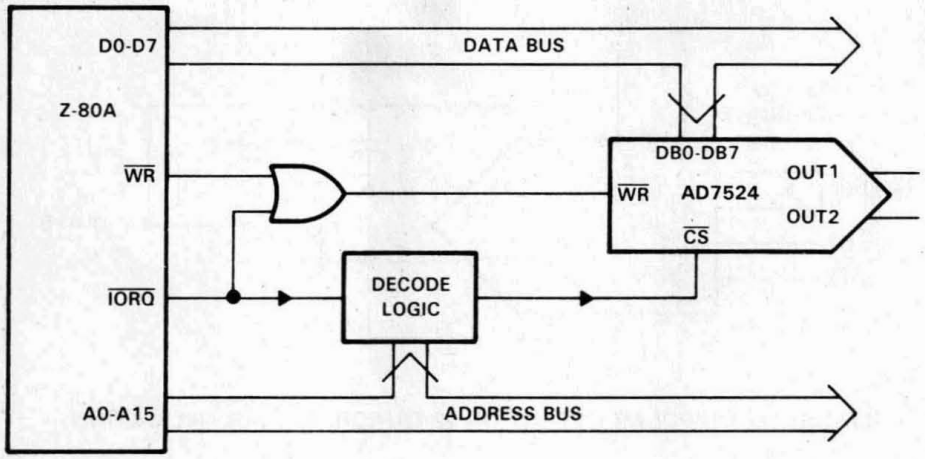


FIGURE 4. AD7524—Z-80A INTERFACE

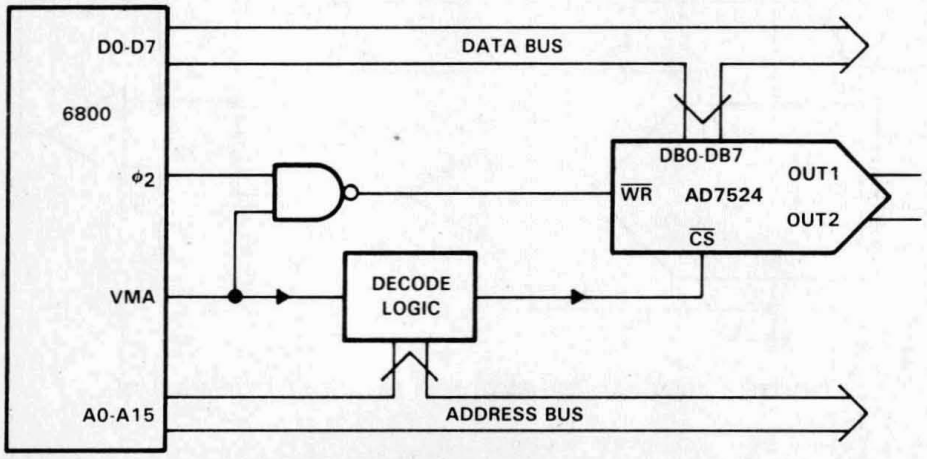


FIGURE 5. AD7524—6800 INTERFACE

microprocessor interfaces (continued)

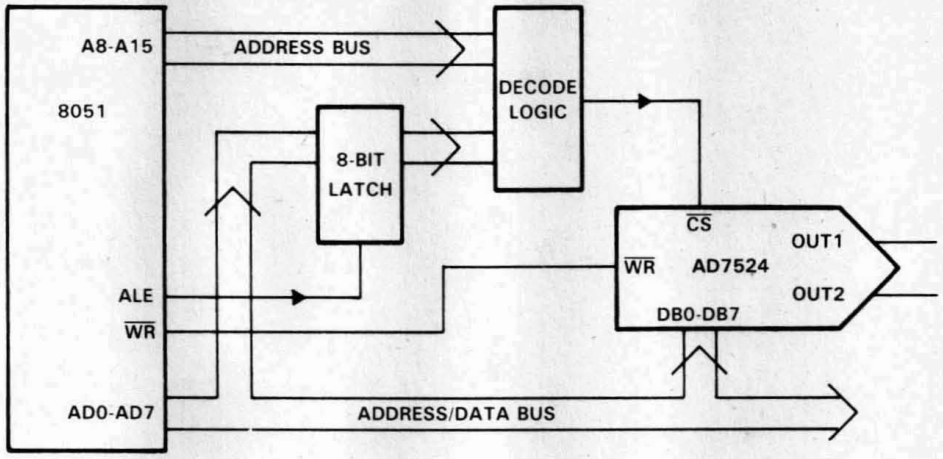


FIGURE 6. AD7524—8051 INTERFACE

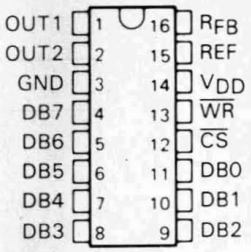
AD7524M
Advanced LinCMOS™ 8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

D3320, SEPTEMBER 1989

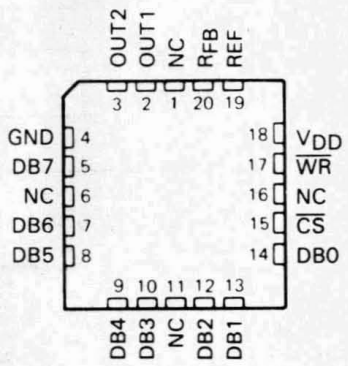
- **Advanced LinCMOS™ Silicon-Gate Technology**
- **Easily Interfaced to Microprocessors**
- **On-Chip Data Latches**
- **Monotonicity Over Entire A/D Conversion Range**
- **Segmented High-Order Bits Ensure Low-Glitch Output**
- **Designed to be Interchangeable with Analog Devices AD7524, PMI PM-7524, and Micro Power Systems MP7524**
- **Fast Control Signaling for Digital Signal Processor Applications Including Interface with SMJ320**

KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 Bits
Linearity error	½ LSB Max
Power dissipation at V_{DD} = 5 V	5 mW Max
Settling time	100 ns Max
Propagation delay	80 ns Max

J PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The AD7524M is an Advanced LinCMOS™ 8-bit digital-to-analog converter (DAC) designed for easy interface to most popular microprocessors.

The AD7524M is an 8-bit multiplying DAC with input latches and with a load cycle similar to the "write" cycle of a random access memory. Segmenting the high-order bits minimizes glitches during changes in the most-significant bits, which produce the highest glitch impulse. The AD7524M provides accuracy to ½ LSB without the need for thin-film resistors or laser trimming, while dissipating less than 5 mW typically.

Featuring operation from a 5-V to 15-V single supply, the AD7524M interfaces easily to most microprocessor buses or output ports. Excellent multiplying (2 or 4 quadrant) makes the AD7524M an ideal choice for many microprocessor-controlled gain-setting and signal-control applications.

The AD7524M is characterized for operation from −55°C to 125°C.

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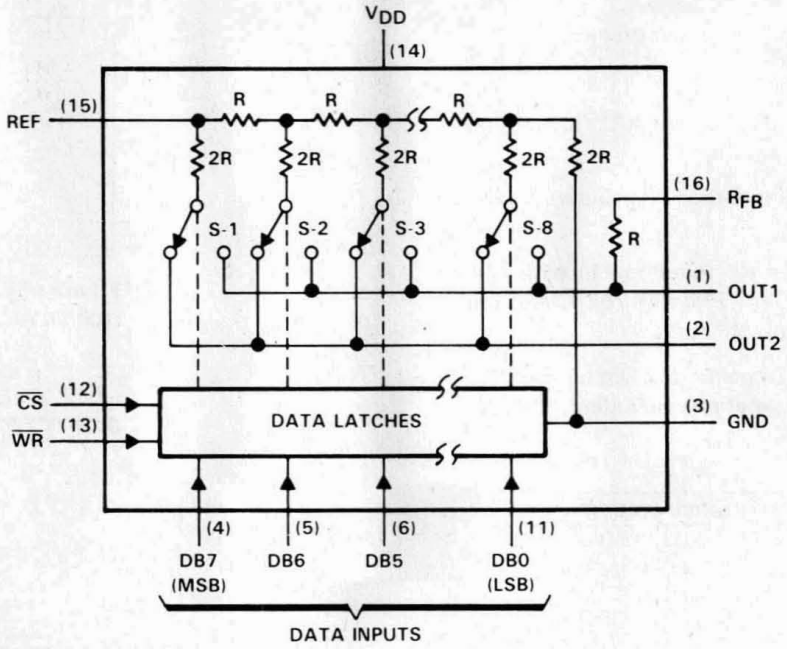
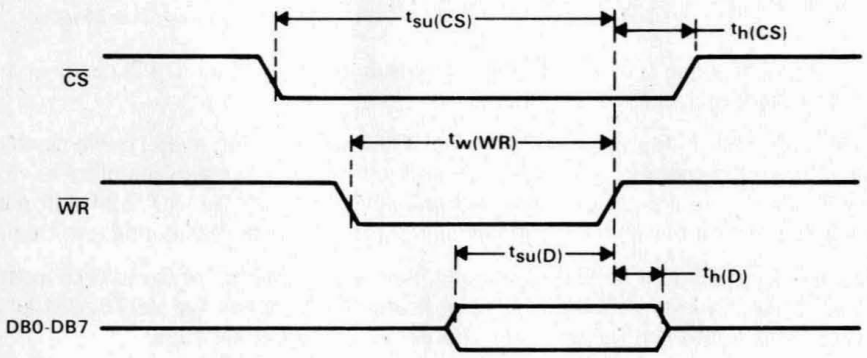
functional block diagram



operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD}	−0.3 V to 17 V
Voltage between R_{FB} and GND	±25 V
Digital input voltage, V_I	−0.3 V to V_{DD} +0.3 V
Reference voltage, V_{ref}	±25 V
Peak digital input current, I_I	10 μA
Operating free-air temperature range	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C

recommended operating conditions

	V_{DD} = 5 V			V_{DD} = 15 V			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}	4.75	5	5.25	14.5	15	15.5	V
Reference voltage, V_{ref}		±10			±10		V
High-level input voltage, V_{IH}	2.4			13.5			V
Low-level input voltage, V_{IL}			0.8			1.5	V
$\overline{CS}$ setup time, $t_{su(CS)}$	40			40			ns
$\overline{CS}$ hold time, $t_{h(CS)}$	0			0			ns
Data bus input setup time, $t_{su(D)}$	25			25			ns
Data bus input hold time, $t_{h(D)}$	10			10			ns
Pulse duration, $\overline{WR}$ low, $t_{w(WR)}$	40			40			ns
Operating free-air temperature, T_A	−55		125	−55		125	°C

electrical characteristics over recommended operating free-air temperature range, V_{ref} = 10 V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER			TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{IH}	High-level input current		$V_I = V_{DD}$	Full range			10			10	μA
				25°C			1			1	
I_{IL}	Low-level input current		$V_I = 0$	Full range			−10			−10	μA
				25°C			−1			−1	
I_{lkg}	Output leakage current	OUT1	DB0-DB7 at 0, $\overline{WR}$ and $\overline{CS}$ at 0 V, V_{ref} = ±10 V	Full range			±400			±200	nA
				25°C			±50			±50	
		OUT2	DB0-DB7 at V_{DD}, $\overline{WR}$ and $\overline{CS}$ at 0 V, V_{ref} = ±10 V	Full range			±400			±200	
				25°C			±50			±50	
I_{DD}	Supply current	Quiescent	DB0-DB7 at V_{IH}min or V_{IL}max				2			2	mA
		Standby	DB0-DB7 at 0 V or V_{DD}	Full range			500			500	μA
				25°C			100			100	
k_{SVS}	Supply voltage sensitivity, $\Delta gain/\Delta V_{DD}$		ΔV_{DD} = 10%	Full range			0.16			0.04	%/%
				25°C		0.002	0.02		0.001	0.02	
C_i	Input capacitance, DB0-DB7, $\overline{WR}$, $\overline{CS}$		$V_I = 0$				5			5	pF
C_o	Output capacitance	OUT1	DB0-DB7 at 0, $\overline{WR}$ and $\overline{CS}$ at 0 V				30			30	pF
		OUT2					120			120	
		OUT1	DB0-DB7 at V_{DD}, $\overline{WR}$ and $\overline{CS}$ at 0 V				120			120	
		OUT2					30			30	
	Reference input impedance (REF to GND)				5		20	5		20	kΩ

operating characteristics over recommended operating free-air temperature range, V_{ref} = 10 V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC} = 5 V		V_{DD} = 15 V		UNIT
			MIN	MAX	MIN	MAX	
Linearity error				±0.2		±0.2	%FSR
Gain error	See Note 1	Full range		±1.4		±0.6	%FSR
		25°C		±1		±0.5	
Settling time (to 1/2 LSB)	See Note 2			100		100	ns
Propagation delay from digital input to 90% of final analog output current	See Note 2			80		80	ns
Feedthrough at OUT1 or OUT2	V_{ref} = ±10 V (100 kHz sinewave), $\overline{WR}$ and $\overline{CS}$ at 0, DB0-DB7 at 0	Full range		0.5		0.5	%FSR
		25°C		0.25		0.25	
Temperature coefficient of gain	T_A = 25°C to t_{min} or t_{max}			±0.004		±0.001	%FSR/°C

NOTES: 1. Gain error is measured using the internal feedback resistor. Nominal Full Scale Range (FSR) = V_{ref} − 1 LSB.
2. OUT1 load = 100 Ω, C_{ext} = 13 pF, $\overline{WR}$ at 0 V, $\overline{CS}$ at 0 V, DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.

PRINCIPLES OF OPERATION

The AD7524M is an 8-bit multiplying D/A converter consisting of an inverted R-2R ladder, analog switches, and data input latches. Binary weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state. The high-order bits are decoded and these decoded bits, through a modification in the R-2R ladder, control three equally weighted current sources. Most applications only require the addition of an external operational amplifier and a voltage reference.

The equivalent circuit for all digital inputs low is seen in Figure 1. With all digital inputs low, the entire reference current, I_{ref}, is switched to OUT2. The current source I/256 represents the constant current flowing through the termination resistor of the R-2R ladder, while the current source I_{lkg} represents leakage currents to the substrate. The capacitances appearing at OUT1 and OUT2 are dependent upon the digital input code. With all digital inputs high, the off-state switch capacitance (30 pF maximum) appears at OUT2 and the on-state switch capacitance (120 pF maximum) appears at OUT1. With all digital inputs low, the situation is reversed as shown in Figure 1. Analysis of the circuit for all digital inputs high is similar to Figure 1; however, in this case, I_{ref} would be switched to OUT1.

Interfacing the AD7524M D/A converter to a microprocessor is accomplished via the data bus and the $\overline{CS}$ and $\overline{WR}$ control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, the AD7524M analog output responds to the data activity on the DB0-DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the $\overline{CS}$ signal or $\overline{WR}$ signal goes high, the data on the DB0-DB7 inputs are latched until the $\overline{CS}$ and $\overline{WR}$ signals go low again. When $\overline{CS}$ is high, the data inputs are disabled regardless of the state of the $\overline{WR}$ signal.

The AD7524M is capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant or 4-quadrant multiplication are shown in Figures 2 and 3. Input coding for unipolar and bipolar operation are summarized in Tables 1 and 2, respectively.

PRINCIPLES OF OPERATION

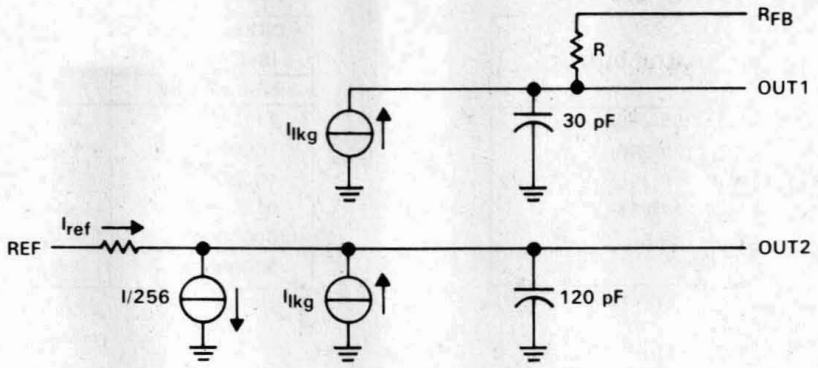


FIGURE 1. AD7524M EQUIVALENT CIRCUIT WITH ALL DIGITAL INPUTS LOW

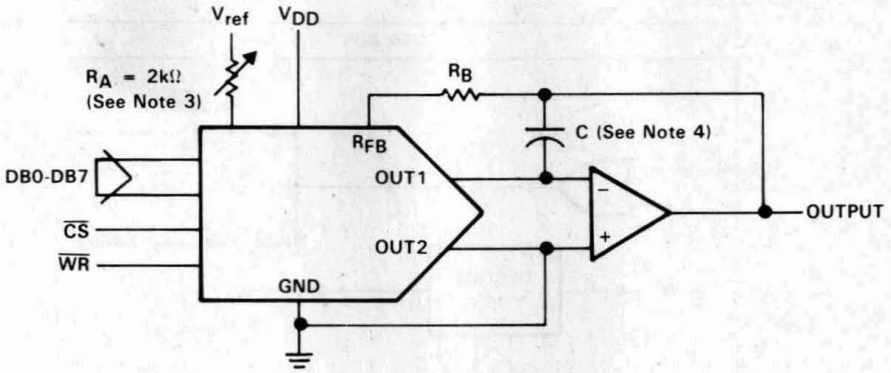


FIGURE 2. UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)

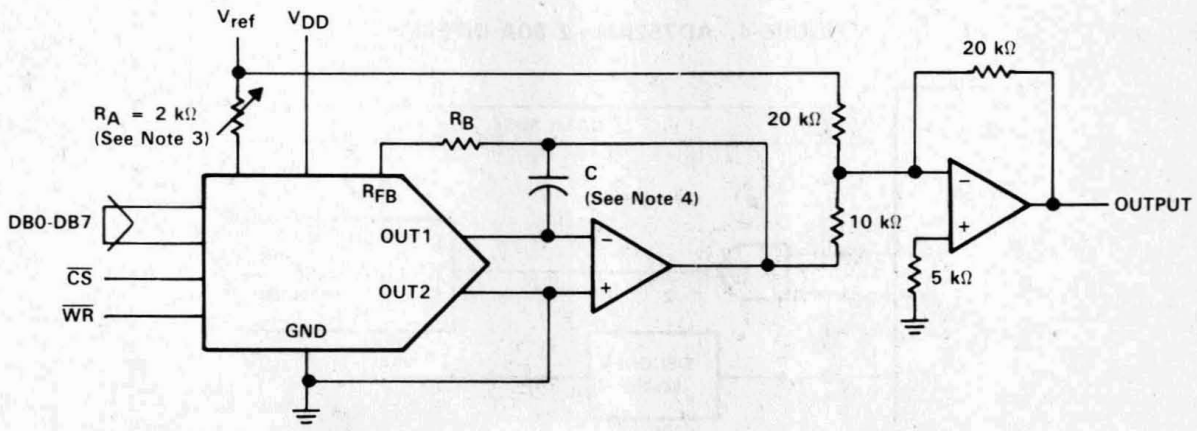


FIGURE 3. BIPOLAR OPERATION (4-QUADRANT OPERATION)

NOTES: 3. R_A and R_B used only if gain adjustment is required.
4. C phase compensation (10-15 pF) is required when using high-speed amplifiers to prevent ringing or oscillation.

PRINCIPLES OF OPERATION

Table 1. Unipolar Binary Code

DIGITAL INPUT (SEE NOTE 5) MSB LSB	ANALOG OUTPUT
11111111	$-V_{ref}$ (255/256)
10000001	$-V_{ref}$ (129/256)
10000000	$-V_{ref}$ (128/256) = $-V_{ref}/2$
01111111	$-V_{ref}$ (127/256)
00000001	$-V_{ref}$ (1/256)
00000000	0

Table 2. Bipolar (Offset Binary) Code

DIGITAL INPUT (SEE NOTE 6) MSB LSB	ANALOG OUTPUT
11111111	V_{ref} (127/128)
10000001	V_{ref} (1/128)
10000000	0
01111111	$-V_{ref}$ (1/128)
00000001	$-V_{ref}$ (127/128)
00000000	$-V_{ref}$

NOTES: 5. LSB = 1/256 (V_{ref}).
6. LSB = 1/128 (V_{ref}).

microprocessor interfaces

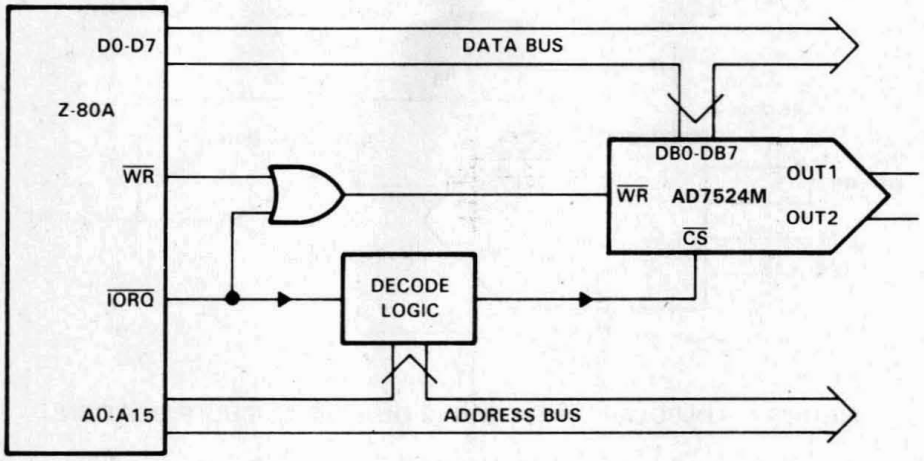


FIGURE 4. AD7524M—Z-80A INTERFACE

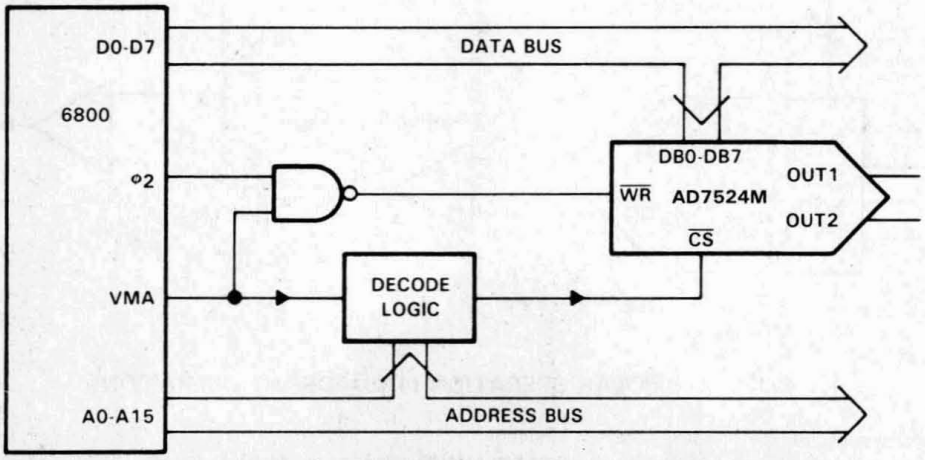


FIGURE 5. AD7524M—6800 INTERFACE

microprocessor interfaces (continued)

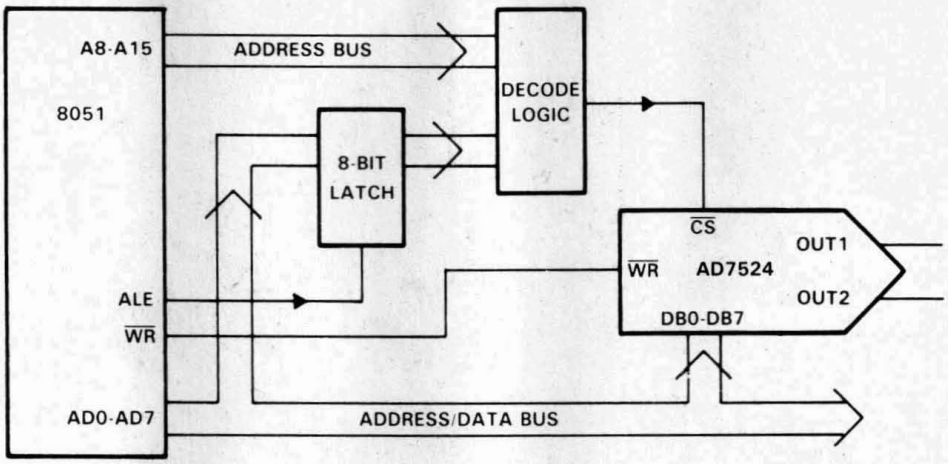


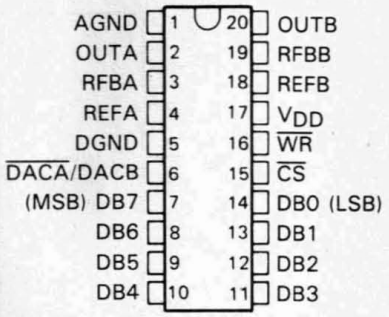
FIGURE 6. AD7524M–8051 INTERFACE

AD7528
Advanced LinCMOS™ DUAL 8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

D3112, JULY 1988

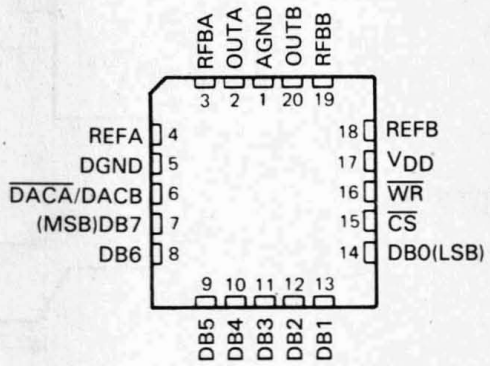
- **Advanced LinCMOS™ Silicon-Gate Technology**
- **Easily Interfaced to Microprocessors**
- **On-Chip Data Latches**
- **Monotonic Over the Entire A/D Conversion Range**
- **Designed to be Interchangeable with Analog Devices AD7528 and PMI PM-7528**
- **Fast Control Signaling for Digital Signal Processor Applications Including Interface with TMS320**

N PACKAGE
(TOP VIEW)



KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 bits
Linearity Error	1/2 LSB
Power Dissipation at V_{DD} = 5 V	5 mW
Settling Time at V_{DD} = 5 V	100 ns
Propagation Delay at V_{DD} = 5 V	80 ns

FN PACKAGE
(TOP VIEW)



description

The AD7528 is a dual 8-bit digital-to-analog converter designed with separate on-chip data latches and featuring excellent DAC-to-DAC matching. Data is transferred to either of the two DAC data latches via a common 8-bit input port. Control input $\overline{\text{DACA}}$/DACB determines which DAC is to be loaded. The "load" cycle of the AD7528 is similar to the "write" cycle of a random-access memory, allowing easy interface to most popular microprocessor busses and output ports. Segmenting the high-order bits minimizes glitches during changes in the most significant bits, where glitch impulse is typically the strongest.

The AD7528 operates from a 5-V to 15-V power supply and dissipates less than 15 mW (typical). Excellent 2- or 4-quadrant multiplying makes the AD7528 a sound choice for many microprocessor-controlled gain-setting and signal-control applications.

The AD7528B is characterized for operation from −25°C to 85°C. The AD7528K is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING TEMPERATURE RANGE
DEVICE	PACKAGE SUFFIX	
AD7528B	FN, N	−25°C to 85°C
AD7528K	FN, N	0°C to 70°C

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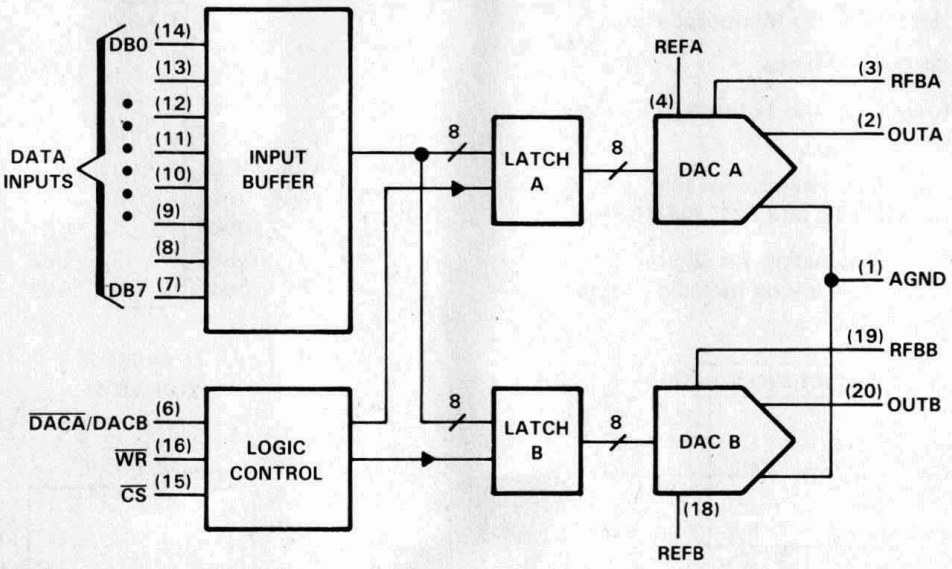
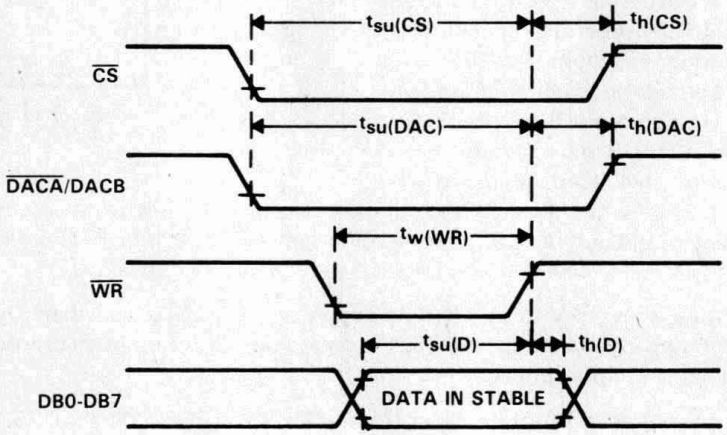
functional block diagram



operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (to AGND or DGND) . . . . . −0.3 V to 17 V
Voltage between AGND and DGND . . . . . ±V_{DD}
Input voltage, V_I (to DGND) . . . . . −0.3 V to V_{DD} +0.3 V
Reference voltage, V_{refA} or V_{refB} (to AGND) . . . . . ±25 V
Feedback voltage, V_{RFBA} or V_{RFBB} (to AGND) . . . . . ±25 V
Output voltage, V_{OA} or V_{OB} (to AGND) . . . . . ±25 V
Peak input current . . . . . 10 μA
Operating free-air temperature range: AD7528B . . . . . −25°C to 85°C
AD7528K . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

recommended operating conditions

		V_{DD} = 4.75 V to 5.25 V			V_{DD} = 14.5 V to 15.5 V			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Reference voltage, V_{refA} or V_{refB}			±10			±10		V
High-level input voltage, V_{IH}		2.4			13.5			V
Low-level input voltage, V_{IL}				0.8			1.5	V
$\overline{CS}$ setup time, $t_{su(CS)}$		50			50			ns
$\overline{CS}$ hold time, $t_{h(CS)}$		0			0			ns
DAC select setup time, $t_{su(DAC)}$		50			50			ns
DAC select hold time, $t_{h(DAC)}$		10			10			ns
Data bus input setup time $t_{su(D)}$		25			25			ns
Data bus input hold time $t_{h(D)}$		0			0			ns
Pulse duration, $\overline{WR}$ low, $t_{w(WR)}$		50			50			ns
Operating free-air temperature, T_A	AD7528B	−25		85	−25		85	°C
	AD7528K	0		70	0		70	

electrical characteristics over recommended operating temperature range, V_{refA} = V_{refB} = 10 V, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		V_{DD} = 5 V		V_{DD} = 15 V		UNIT
					MIN	MAX	MIN	MAX	
I_{IH}	High-level input current		$V_I = V_{DD}$	Full Range		10		10	μA
				25°C		1		1	
I_{IL}	Low-level input current		V_I = 0	Full Range		−10		−10	μA
				25°C		−1		−1	
	Reference input impedance (Pin 15 to GND)				8	15	8	15	kΩ
I_{lkg}	Output leakage current	OUTA	DAC data latch loaded with 00000000, V_{refA} = ±10 V	Full Range		±400		±200	nA
				25°C		±50		±50	
		OUTB	DAC data latch loaded with 00000000, V_{refB} = ±10 V	Full Range		±400		±200	
				25°C		±50		±50	
	Input resistance match (REFA to REFB)					±1%		±1%	
	DC supply sensitivity $\Delta gain/\Delta V_{DD}$		V_{DD} = ±10%	Full Range		0.04		0.02	%/%
				25°C		0.02		0.01	
I_{DD}	Supply current	Quiescent	DB0-DB7 at V_{IH}min or V_{IL}max			1		1	mA
		Standby	DB0-DB7 at 0 V or V_{DD}	Full Range		0.5		0.5	
				25°C		0.1		0.1	
C_i	Input capacitance	DB0-DB7	V_I = 0 or V_{DD}			10		10	pF
		$\overline{WR}$, $\overline{CS}$, $\overline{DACA}$/DACB				15		15	
C_o	Output capacitance (OUTA, OUTB)		DAC Data latches loaded with 00000000			50		50	pF
			DAC Data latches loaded with 11111111			120		120	

operating characteristics over recommended operating free-air temperature range, V_{refA} = V_{refB} = 10 V, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 15 V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Linearity error						±1/2			±1/2	LSB
Setting time (to 1/2 LSB)		See Note 1				100			100	ns
Gain error		See Note 2	Full Range			±4			±3	LSB
			25°C			±2			±2	
AC feedthrough	REFA to OUTA	See Note 3	Full Range			−65			−65	dB
	REFB to OUTB		25°C			−70			−70	
Temperature coefficient of gain						0.007			0.0035	%FSR/°C
Propagation delay (from digital input to 90% of final analog output current)		See Note 4				80			80	ns
Channel-to-channel isolation	REFA to OUTB	See Note 5	25°C		77			77		dB
	REFB to OUTA	See Note 6	25°C		77			77		
Digital-to-analog glitch impulse area		Measured for code transition from 00000000 to 11111111, T_A = 25°C			160			440		nVs
Digital crosstalk glitch impulse area		Measured for code transition from 00000000 to 11111111, T_A = 25°C			30			60		nVs
Harmonic distortion		V_i = 6 V, f = 1 kHz, T_A = 25°C			−85			−85		dB

NOTES: 1. OUTA, OUTB load = 100 Ω, C_{ext} = 13 pF; $\overline{WR}$ and $\overline{CS}$ at 0 V; DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
2. Gain error is measured using an internal feedback resistor. Nominal Full Scale Range (FSR) = V_{ref} − 1 LSB.
3. V_{ref} = 20 V peak-to-peak, 100-kHz sine wave; DAC data latches loaded with 0000000.
4. V_{refA} = V_{refB} = 10 V; OUTA/OUTB load = 100 Ω, C_{ext} = 13 pF; $\overline{WR}$ and $\overline{CS}$ at 0 V; DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
5. Both DAC latches loaded with 11111111; V_{refA} = 20 V peak-to-peak, 100-kHz sine wave; V_{refB} = 0.
6. Both DAC latches loaded with 11111111; V_{refB} = 20 V peak-to-peak, 100-kHz sine wave; V_{refA} = 0.

principles of operation

The AD7528 contains two identical 8-bit multiplying D/A converters, DACA and DACB. Each DAC consists of an inverted R-2R ladder, analog switches, and input data latches. Binary-weighted currents are switched between DAC output and AGND, thus maintaining a constant current in each ladder leg independent of the switch state. Most applications require only the addition of an external operational amplifier and voltage reference. A simplified D/A circuit for DACA with all digital inputs low is shown in Figure 1.

Figure 2 shows the DACA equivalent circuit. A similar equivalent circuit can be drawn for DACB. Both DACs share the analog ground pin 1 (AGND). With all digital inputs high, the entire reference current flows to OUTA. A small leakage current (I_{lkg}) flows across internal junctions, and as with most semiconductor devices, doubles every 10°C. C_O is due to the parallel combination of the NMOS switches and has a value that depends on the number of switches connected to the output. The range of C_O is 50 pF to 120 pF maximum. The equivalent output resistance r_O varies with the input code from 0.8R to 3R where R is the nominal value of the ladder resistor in the R-2R network.

Interfacing the AD7528 to a microprocessor is accomplished via the data bus, $\overline{CS}$, $\overline{WR}$, and $\overline{DACA}$/DACB control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, the AD7528 analog output, specified by the $\overline{DACA}$/DACB control line, responds to the activity on the DB0-DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the $\overline{CS}$ signal or $\overline{WR}$ signal goes high, the data on the DB0-DB7 inputs is latched until the $\overline{CS}$ and $\overline{WR}$ signals go low again. When $\overline{CS}$ is high, the data inputs are disabled regardless of the state of the $\overline{WR}$ signal.

The digital inputs of the AD7528 provide TTL compatibility when operated from a supply voltage of 5 V. The AD7528 may be operated with any supply voltage in the range from 5 V to 15 V, however, input logic levels are not TTL compatible above 5 V.

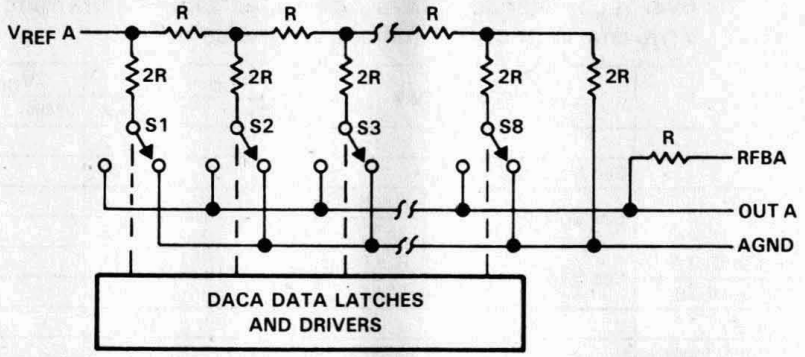


FIGURE 1. SIMPLIFIED FUNCTIONAL CIRCUIT FOR DACA

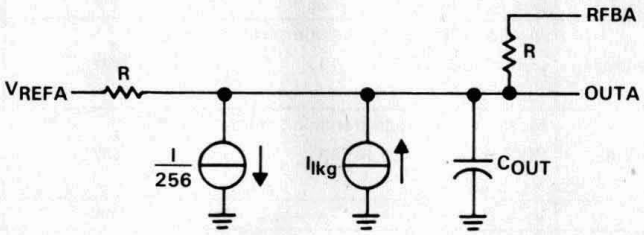


FIGURE 2. AD7528 EQUIVALENT CIRCUIT, DACA LATCH LOADED WITH 11111111.

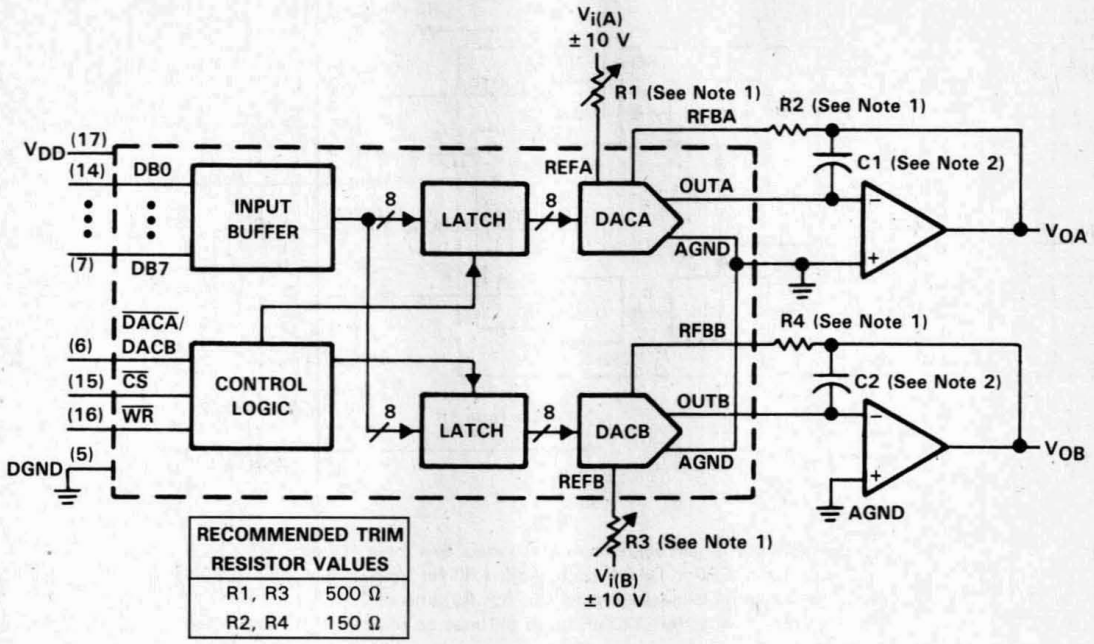
MODE SELECTION TABLE

$\overline{DACA}$/DACB	$\overline{CS}$	$\overline{WR}$	DACA	DACB
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = low level, H = high level, X = don't care

TYPICAL APPLICATION DATA

The AD7528 is capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant and 4-quadrant multiplication are shown in Figures 3 and 4. Input coding for unipolar and bipolar operation are summarized in Tables 1 and 2, respectively.

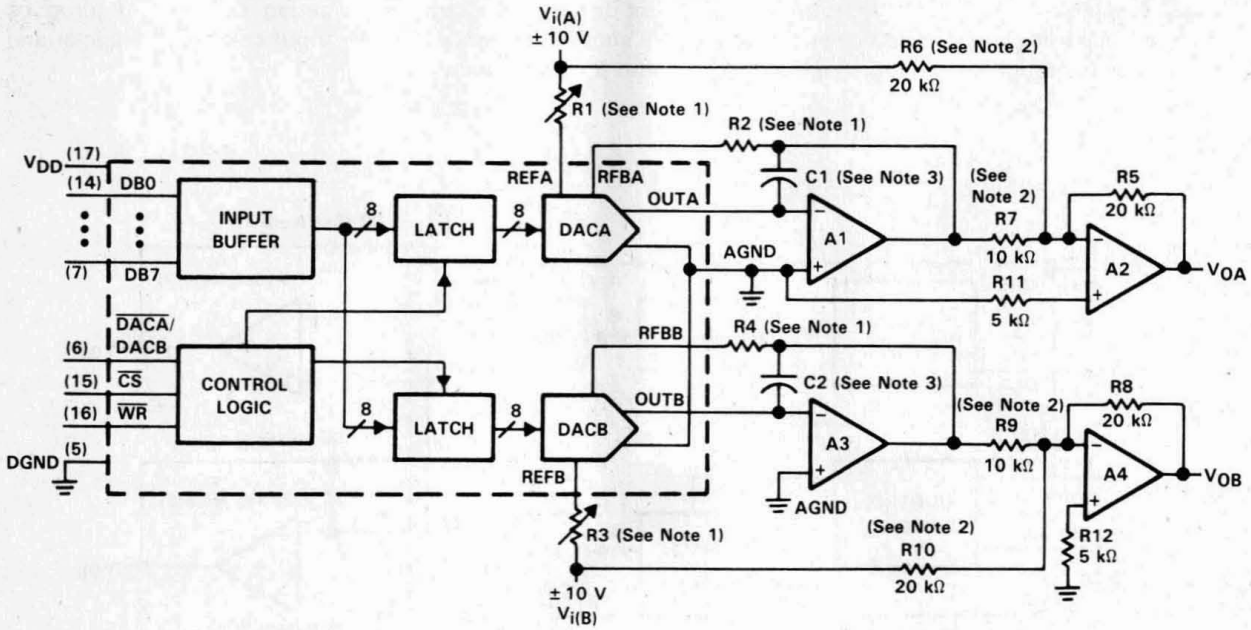


RECOMMENDED TRIM RESISTOR VALUES	
R1, R3	500 Ω
R2, R4	150 Ω

NOTES: 1. R1, R2, R3, and R4 are used only if gain adjustment is required. See table for recommended values. Make gain adjustment with digital input of 255.
2. C1 and C2 phase compensation capacitors (10 pF to 15 pF) are required when using high-speed amplifiers to prevent ringing or oscillation.

FIGURE 3. UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)

TYPICAL APPLICATION DATA



NOTES: 1. R1, R2, R3, and R4 are used only if gain adjustment is required. See table in Figure 3 for recommended values. Adjust R1 for V_{OA} = 0 V with code 10000000 in DACA latch. Adjust R3 for V_{OB} = 0 V with 10000000 in DACB latch.
2. Matching and tracking are essential for resistor pairs R6, R7, R9, and R10.
3. C1 and C2 phase compensation capacitors (10 pF to 15 pF) may be required if A1 and A3 are high-speed amplifiers.

FIGURE 4. BIPOLAR OPERATION (4-QUADRANT OPERATION)

TABLE 1. UNIPOLAR BINARY CODE

DAC LATCH CONTENTS MSB LSB†	ANALOG OUTPUT
11111111	$-V_i$ (255/256)
10000001	$-V_i$ (129/256)
10000000	$-V_i$ (128/256) = $-V_i/2$
01111111	$-V_i$ (127/256)
00000001	$-V_i$ (1/256)
00000000	$-V_i$ (0/256) = 0

† 1 LSB = $(2^{-8})V_i$

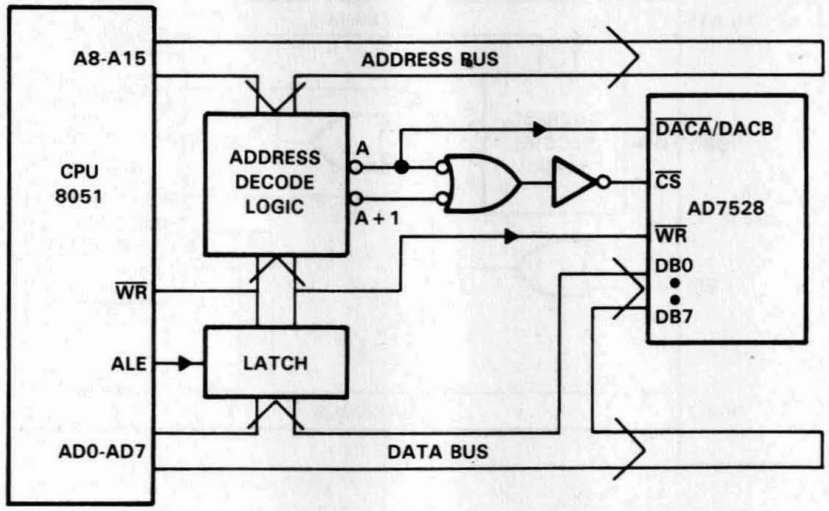
TABLE 2. BIPOLAR (OFFSET BINARY) CODE

DAC LATCH CONTENTS MSB LSB‡	ANALOG OUTPUT
11111111	V_i (127/128)
10000001	V_i (1/128)
10000000	0 V
01111111	$-V_i$ (1/128)
00000001	$-V_i$ (127/128)
00000000	$-V_i$ (128/128)

‡ 1 LSB = $(2^{-7})V_i$

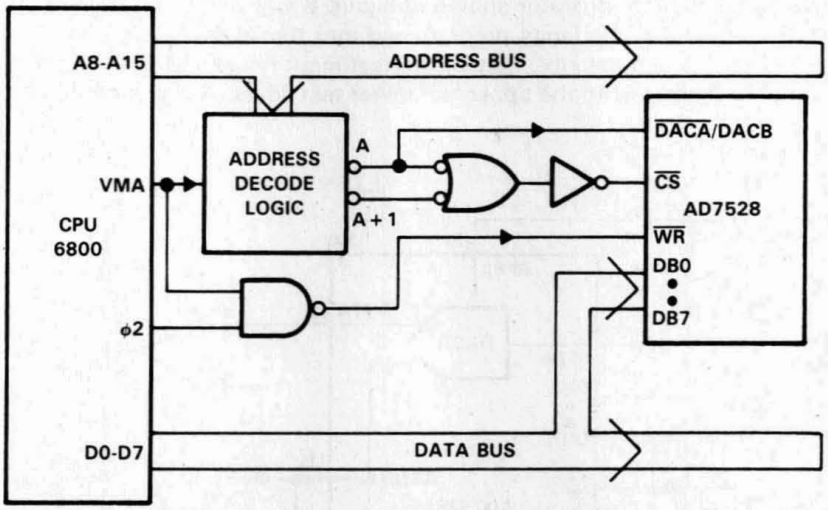
TYPICAL APPLICATION DATA

microprocessor interface information



NOTE: A = decoded address for AD7528 DACA.
A+1 = decoded address for AD7528 DACB.

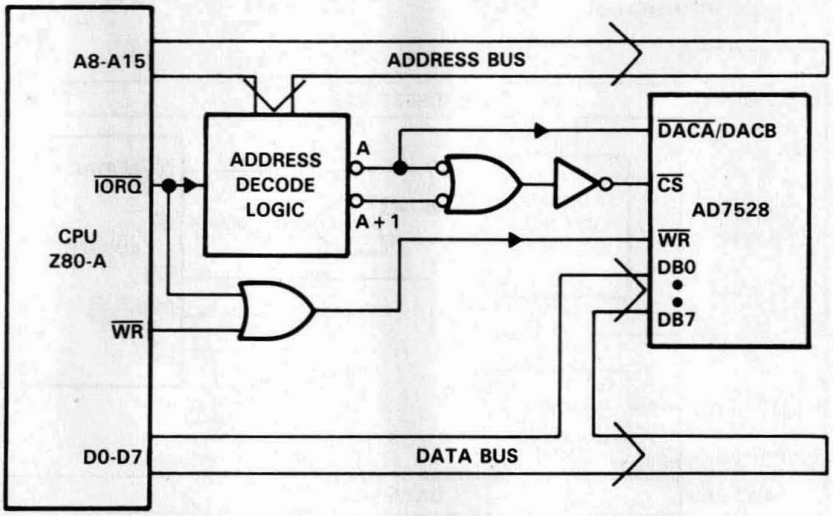
FIGURE 5. AD7528 – INTEL 8051 INTERFACE



NOTE: A = decoded address for AD7528 DACA.
A+1 = decoded address for AD7528 DACB.

FIGURE 6. AD7528 – 6800 INTERFACE

TYPICAL APPLICATION DATA



NOTE: A = decoded address for AD7528 DACA.
A+1 = decoded address for AD7528 DACB.

FIGURE 7. AD7528 TO Z-80A INTERFACE

programmable window detector

The programmable window comparator shown in Figure 8 will determine if voltage applied to the DAC feedback resistors are within the limits programmed into the AD7528 data latches. Input signal range depends on the reference and polarity, that is, the test input range is 0 to $-V_{ref}$. The DACA and DACB data latches are programmed with the upper and lower test limits. A signal within the programmed limits will drive the output high.

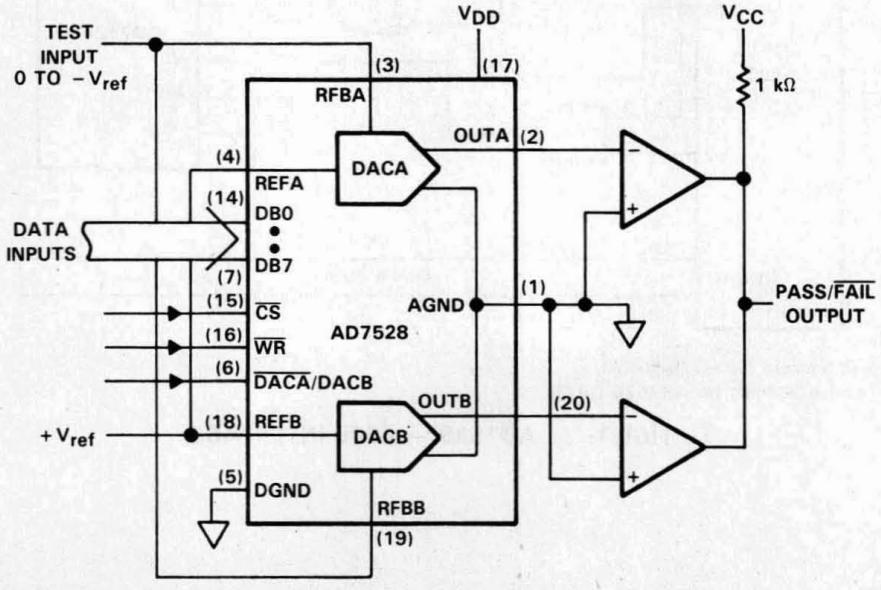


FIGURE 8. DIGITALLY PROGRAMMABLE WINDOW COMPARATOR (UPPER- AND LOWER-LIMIT TESTER)

TYPICAL APPLICATION DATA

digitally controlled signal attenuator

Figure 9 shows the AD7528 configured as a two-channel programmable attenuator. Applications include stereo audio and telephone signal level control. Table 3 shows input codes vs attenuation for a 0 to 15.5 dB range.

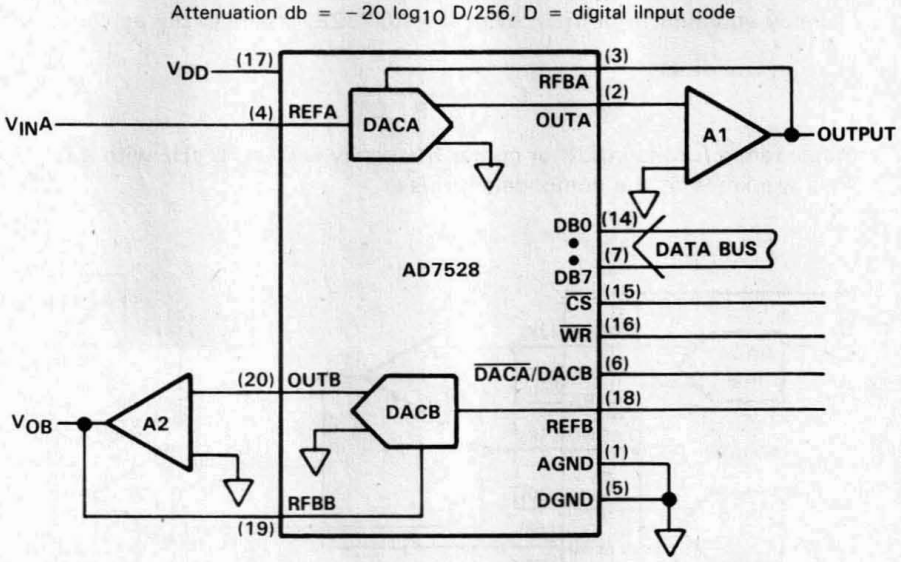


FIGURE 9. DIGITALLY CONTROLLED DUAL TELEPHONE ATTENUATOR

TABLE 3. ATTENUATION vs DACA, DACB CODE

ATTN(dB)	DAC INPUT CODE	CODE IN DECIMAL	ATTN(dB)	DAC INPUT CODE	CODE IN DECIMAL
0	11111111	255	8.0	01100110	102
0.5	11110010	242	8.5	01100000	96
1.0	11100100	228	9.0	01011011	91
1.5	11010111	215	9.5	01010110	86
2.0	11001011	203	10.0	01010001	81
2.5	11000000	192	10.5	01001100	76
3.0	10110101	181	11.0	01001000	72
3.5	10101011	171	11.5	01000100	68
4.0	10100010	162	12.0	01000000	64
4.5	10011000	152	12.5	00111101	61
5.0	10010000	144	13.0	00111001	57
5.5	10001000	136	13.5	00110110	54
6.0	10000000	128	14.0	00110011	51
6.5	01111001	121	14.5	00110000	48
7.0	01110010	114	15.0	00101110	46
7.5	01101100	108	15.5	00101011	43

TYPICAL APPLICATION DATA

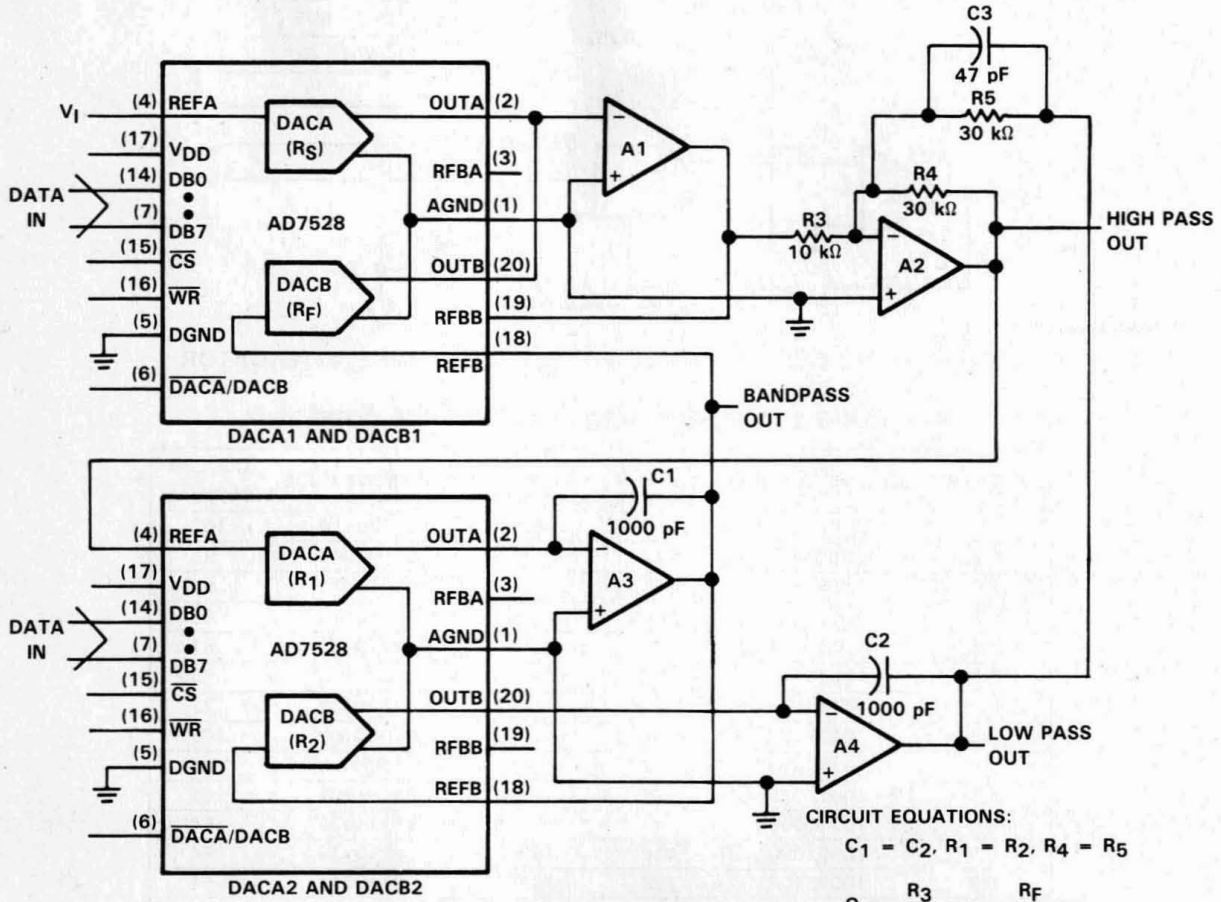
programmable state-variable filter

This programmable state-variable or universal filter configuration provides low-pass, high-pass, and band-pass outputs, and is suitable for applications in which microprocessor control of filter parameters is required.

As shown in Figure 10, DACA1 and DACB1 control the gain and Q of the filter while DACA2 and DACB2 control the cutoff frequency. Both halves of the DACA2 and DACB2 must track accurately in order for the cutoff-frequency equation to be true. With the AD7528, this is easily achieved.

$$f_C = \frac{1}{2\pi\ R1\ C1}$$

The programmable range for the cutoff or center frequency is 0 to 15 kHz with a Q ranging from 0.3 to 4.5. This defines the limits of the component values.



NOTES: A. Op-amps A1, A2, A3, and A4 are TL287.

B. C3 compensates for the op-amp gain-bandwidth limitations.

C. DAC equivalent resistance equals $\frac{256 \times \text{(DAC ladder resistance)}}{\text{DAC digital code}}$

FIGURE 10. DIGITALLY CONTROLLED STATE-VARIABLE FILTER

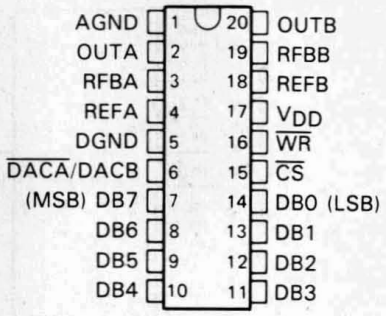
AD7528M
Advanced LinCMOS™ DUAL 8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

D3321, SEPTEMBER 1989

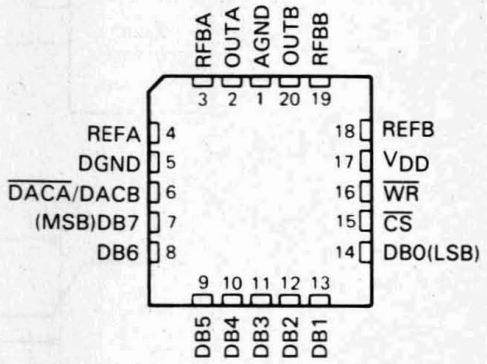
- **Advanced LinCMOS™ Silicon-Gate Technology**
- **Easily Interfaced to Microprocessors**
- **On-Chip Data Latches**
- **Monotonic Over the Entire A/D Conversion Range**
- **Designed to be Interchangeable with Analog Devices AD7528 and PMI PM-7528**
- **Fast Control Signaling for Digital Signal Processor Applications Including Interface with SMJ320**

KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 bits
Linearity Error	1/2 LSB
Power Dissipation at V_{DD} = 5 V	5 mW
Settling Time at V_{DD} = 5 V	100 ns
Propagation Delay at V_{DD} = 5 V	80 ns

J PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



description

The AD7528M is a dual 8-bit digital-to-analog converter designed with separate on-chip data latches and featuring excellent DAC-to-DAC matching. Data is transferred to either of the two DAC data latches via a common 8-bit input port. Control input $\overline{\text{DACA}}$/DACB determines which DAC is to be loaded. The ''load'' cycle of the AD7528M is similar to the ''write'' cycle of a random-access memory, allowing easy interface to most popular microprocessor buses and output ports. Segmenting the high-order bits minimizes glitches during changes in the most significant bits, where glitch impulse is typically the strongest.

The AD7528M operates from a 5-V to 15-V power supply and dissipates less than 15 mW (typical). Excellent 2- or 4-quadrant multiplying makes the AD7528M a sound choice for many microprocessor-controlled gain-setting and signal-control applications.

The AD7528M is characterized for operation from −55°C to 125°C.

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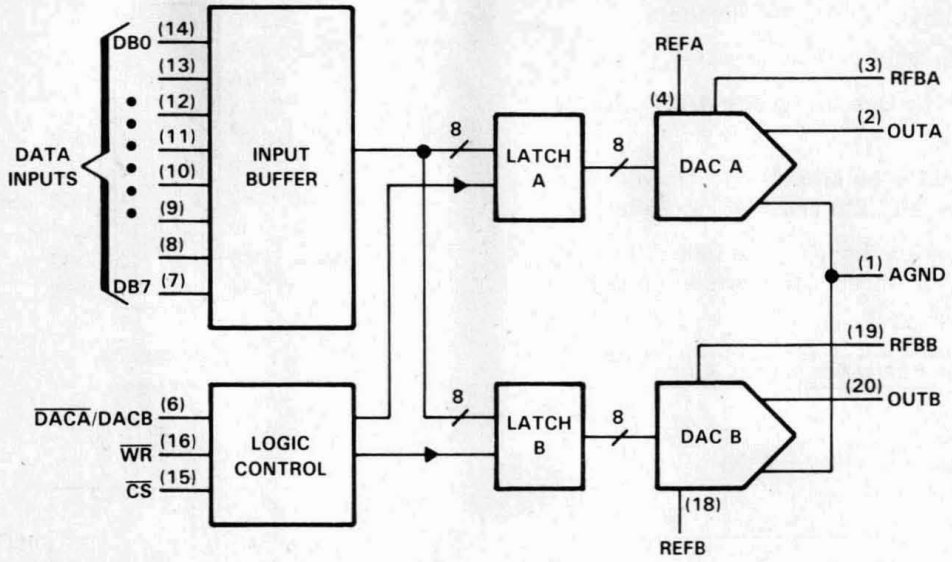
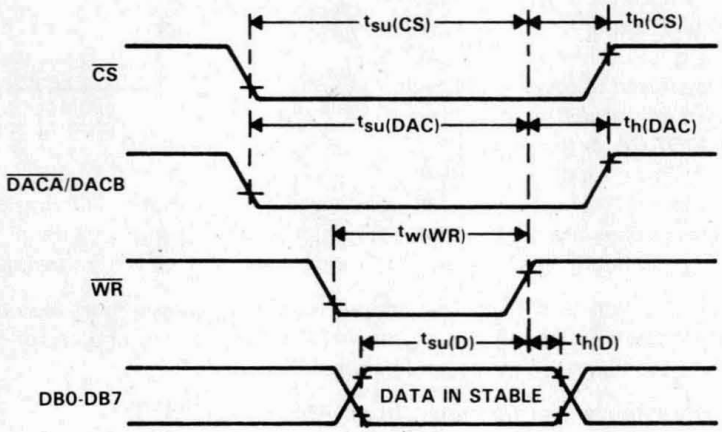
functional block diagram



operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (to AGND or DGND) . . . . . −0.3 V to 17 V
Voltage between AGND and DGND . . . . . ±V_{DD}
Input voltage, V_I (to DGND) . . . . . −0.3 V to V_{DD} +0.3 V
Reference voltage, V_{refA} or V_{refB} (to AGND) . . . . . ±25 V
Feedback voltage, V_{RFBA} or V_{RFBB} (to AGND) . . . . . ±25 V
Output voltage, V_{OA} or V_{OB} (to AGND) . . . . . ±25 V
Peak input current . . . . . 10 μA
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

recommended operating conditions

	V_{DD} = 4.75 V to 5.25 V			V_{DD} = 14.5 V to 15.5 V			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Reference voltage, V_{refA} or V_{refB}		±10			±10		V
High-level input voltage, V_{IH}	2.4			13.5			V
Low-level input voltage, V_{IL}			0.8			1.5	V
$\overline{CS}$ setup time, $t_{su(CS)}$	50			50			ns
$\overline{CS}$ hold time, $t_{h(CS)}$	0			0			ns
DAC select setup time, $t_{su(DAC)}$	50			50			ns
DAC select hold time, $t_{h(DAC)}$	10			10			ns
Data bus input setup time $t_{su(D)}$	25			25			ns
Data bus input hold time $t_{h(D)}$	0			0			ns
Pulse duration, $\overline{WR}$ low, $t_{w(WR)}$	50			50			ns
Operating free-air temperature, T_A	−55		125	−55		125	°C

electrical characteristics over recommended operating temperature range, V_{refA} = V_{refB} = 10 V, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		V_{DD} = 5 V MIN	V_{DD} = 5 V MAX	V_{DD} = 15 V MIN	V_{DD} = 15 V MAX	UNIT
I_{IH}	High-level input current		$V_I = V_{DD}$	Full Range		10		10	μA
				25°C		1		1	
I_{IL}	Low-level input current		V_I = 0	Full Range		−10		−10	μA
				25°C		−1		−1	
	Reference input impedance (Pin 15 to GND)				8	15	8	15	kΩ
I_{lkg}	Output leakage current	OUTA	DAC data latch loaded with 00000000, V_{refA} = ±10 V	Full Range		±400		±200	nA
				25°C		±50		±50	
		OUTB	DAC data latch loaded with 00000000, V_{refB} = ±10 V	Full Range		±400		±200	
				25°C		±50		±50	
	Input resistance match (REFA to REFB)					±1%		±1%	
	DC supply sensitivity Δgain/ΔV_{DD}		V_{DD} = ±10%	Full Range		0.04		0.02	%/%
				25°C		0.02		0.01	
I_{DD}	Supply current	Quiescent	DB0-DB7 at V_{IH}min or V_{IL}max			1		1	mA
		Standby	DB0-DB7 at 0 V or V_{DD}	Full Range		0.5		0.5	
				25°C		0.1		0.1	
C_i	Input capacitance	DB0-DB7	V_I = 0 or V_{DD}			10		10	pF
		$\overline{WR}$, $\overline{CS}$, $\overline{DACA}$/DACB				15		15	
C_o	Output capacitance (OUTA, OUTB)		DAC Data latches loaded with 00000000			50		50	pF
			DAC Data latches loaded with 11111111			120		120	

operating characteristics over recommended operating free-air temperature range, V_{refA} = V_{refB} = 10 V, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 15 V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Linearity error						±1/2			±1/2	LSB
Setting time (to 1/2 LSB)		See Note 1				100			100	ns
Gain error		See Note 2	Full Range			±4			±3	LSB
			25°C			±2			±2	
AC feedthrough	REFA to OUTA	See Note 3	Full Range			−65			−65	dB
	REFB to OUTB		25°C			−70			−70	
Temperature coefficient of gain						0.007			0.0035	%FSR/°C
Propagation delay (from digital input to 90% of final analog output current)		See Note 4				80			80	ns
Channel-to-channel isolation	REFA to OUTB	See Note 5	25°C		77			77		dB
	REFB to OUTA	See Note 6	25°C		77			77		
Digital-to-analog glitch impulse area		Measured for code transition from 00000000 to 11111111, T_A = 25°C			160			440		nVs
Digital crosstalk glitch impulse area		Measured for code transition from 00000000 to 11111111, T_A = 25°C			30			60		nVs
Harmonic distortion		V_i = 6 V, f = 1 kHz, T_A = 25°C			−85			−85		dB

NOTES: 1. OUTA, OUTB load = 100 Ω, C_{ext} = 13 pF; $\overline{WR}$ and $\overline{CS}$ at 0 V; DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
2. Gain error is measured using an internal feedback resistor. Nominal Full Scale Range (FSR) = V_{ref} − 1 LSB.
3. V_{ref} = 20 V peak-to-peak, 100-kHz sine wave; DAC data latches loaded with 0000000.
4. V_{refA} = V_{refB} = 10 V; OUTA/OUTB load = 100 Ω, C_{ext} = 13 pF; $\overline{WR}$ and $\overline{CS}$ at 0 V; DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
5. Both DAC latches loaded with 11111111; V_{refA} = 20 V peak-to-peak, 100-kHz sine wave; V_{refB} = 0.
6. Both DAC latches loaded with 11111111; V_{refB} = 20 V peak-to-peak, 100-kHz sine wave; V_{refA} = 0.

principles of operation

The AD7528M contains two identical 8-bit multiplying D/A converters, DACA and DACB. Each DAC consists of an inverted R-2R ladder, analog switches, and input data latches. Binary-weighted currents are switched between DAC output and AGND, thus maintaining a constant current in each ladder leg independent of the switch state. Most applications require only the addition of an external operational amplifier and voltage reference. A simplified D/A circuit for DACA with all digital inputs low is shown in Figure 1.

Figure 2 shows the DACA equivalent circuit. A similar equivalent circuit can be drawn for DACB. Both DACs share the analog ground pin 1 (AGND). With all digital inputs high, the entire reference current flows to OUTA. A small leakage current (I_{lkg}) flows across internal junctions, and as with most semiconductor devices, doubles every 10°C. C_o is due to the parallel combination of the NMOS switches and has a value that depends on the number of switches connected to the output. The range of C_o is 50 pF to 120 pF maximum. The equivalent output resistance r_o varies with the input code from 0.8R to 3R where R is the nominal value of the ladder resistor in the R-2R network.

Interfacing the AD7528M to a microprocessor is accomplished via the data bus, $\overline{CS}$, $\overline{WR}$, and $\overline{DACA}$/DACB control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, the AD7528M analog output, specified by the $\overline{DACA}$/DACB control line, responds to the activity on the DB0-DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the $\overline{CS}$ signal or $\overline{WR}$ signal goes high, the data on the DB0-DB7 inputs is latched until the $\overline{CS}$ and $\overline{WR}$ signals go low again. When $\overline{CS}$ is high, the data inputs are disabled regardless of the state of the $\overline{WR}$ signal.

The digital inputs of the AD7528M provide TTL compatibility when operated from a supply voltage of 5 V. The AD7528M may be operated with any supply voltage in the range from 5 V to 15 V, however, input logic levels are not TTL compatible above 5 V.

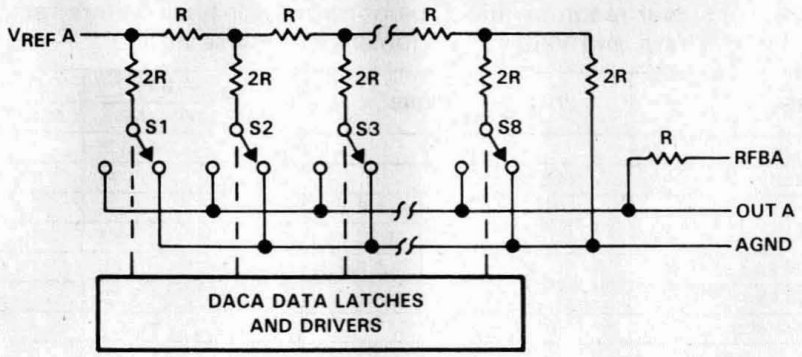


FIGURE 1. SIMPLIFIED FUNCTIONAL CIRCUIT FOR DACA

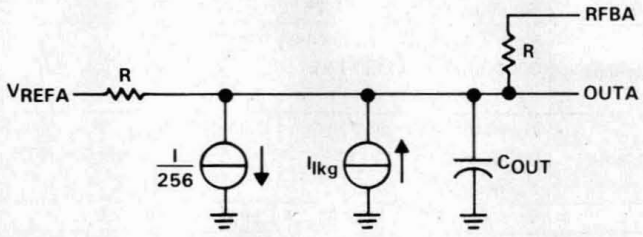


FIGURE 2. AD7528M EQUIVALENT CIRCUIT, DACA LATCH LOADED WITH 11111111

MODE SELECTION TABLE

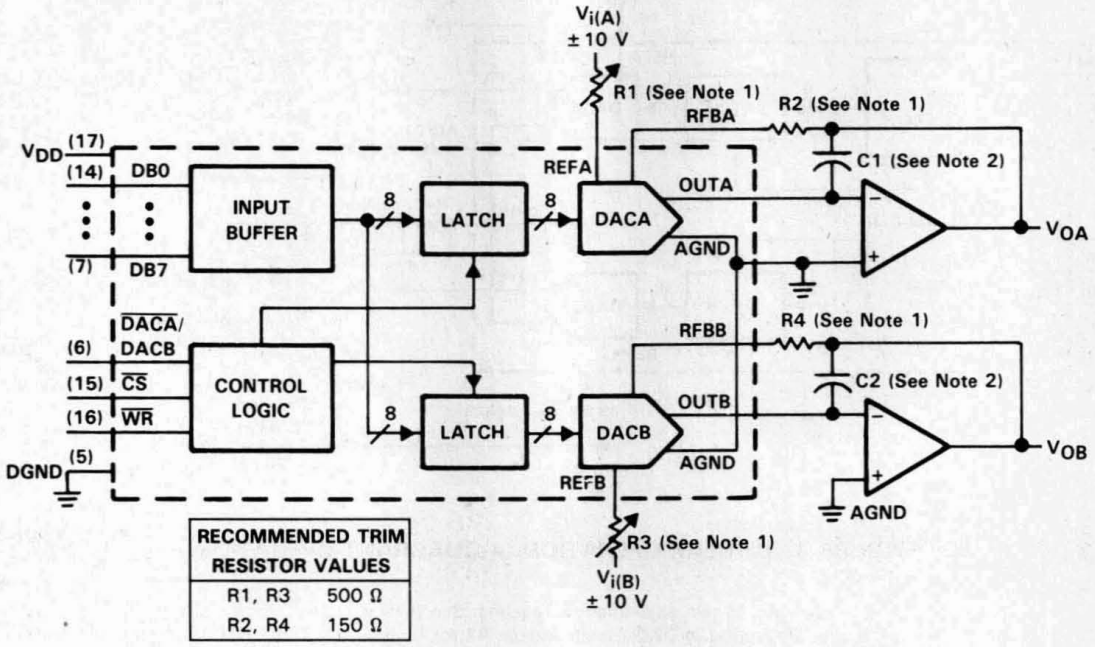
$\overline{DACA}$/DACB	$\overline{CS}$	$\overline{WR}$	DACA	DACB
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = low level, H = high level, X = don't care

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

APPLICATION DATA

The AD7528M is capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant and 4-quadrant multiplication are shown in Figures 3 and 4. Input coding for unipolar and bipolar operation are summarized in Tables 1 and 2, respectively.



RECOMMENDED TRIM RESISTOR VALUES	
R1, R3	500 Ω
R2, R4	150 Ω

NOTES: 1. R1, R2, R3, and R4 are used only if gain adjustment is required. See table for recommended values. Make gain adjustment with digital input of 255.
2. C1 and C2 phase compensation capacitors (10 pF to 15 pF) are required when using high-speed amplifiers to prevent ringing or oscillation.

FIGURE 3. UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)

APPLICATION DATA

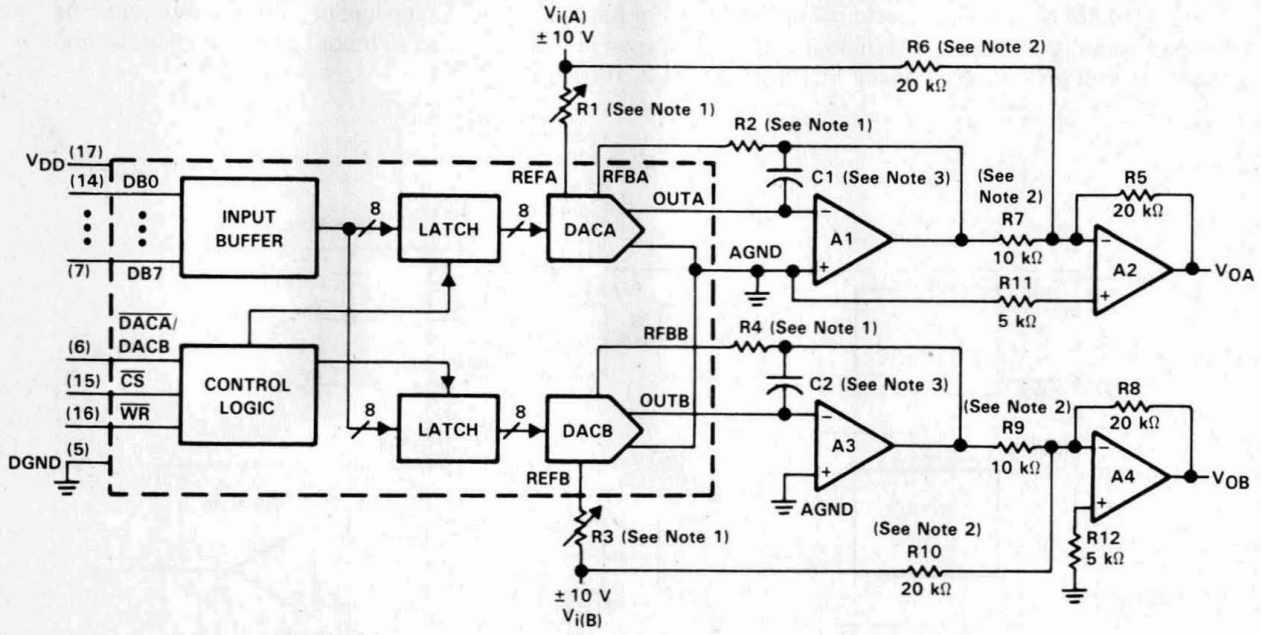


FIGURE 4. BIPOLAR OPERATION (4-QUADRANT OPERATION)

NOTES: 1. R1, R2, R3, and R4 are used only if gain adjustment is required. See table in Figure 3 for recommended values. Adjust R1 for V_{OA} = 0 V with code 10000000 in DACA latch. Adjust R3 for V_{OB} = 0 V with 10000000 in DACB latch.
2. Matching and tracking are essential for resistor pairs R6, R7, R9, and R10.
3. C1 and C2 phase compensation capacitors (10 pF to 15 pF) may be required if A1 and A3 are high-speed amplifiers.

TABLE 1. UNIPOLAR BINARY CODE

DAC LATCH CONTENTS MSB LSB†	ANALOG OUTPUT
11111111	$-V_i$ (255/256)
10000001	$-V_i$ (129/256)
10000000	$-V_i$ (128/256) = $-V_i/2$
01111111	$-V_i$ (127/256)
00000001	$-V_i$ (1/256)
00000000	$-V_i$ (0/256) = 0

† 1 LSB = $(2^{-8})V_i$

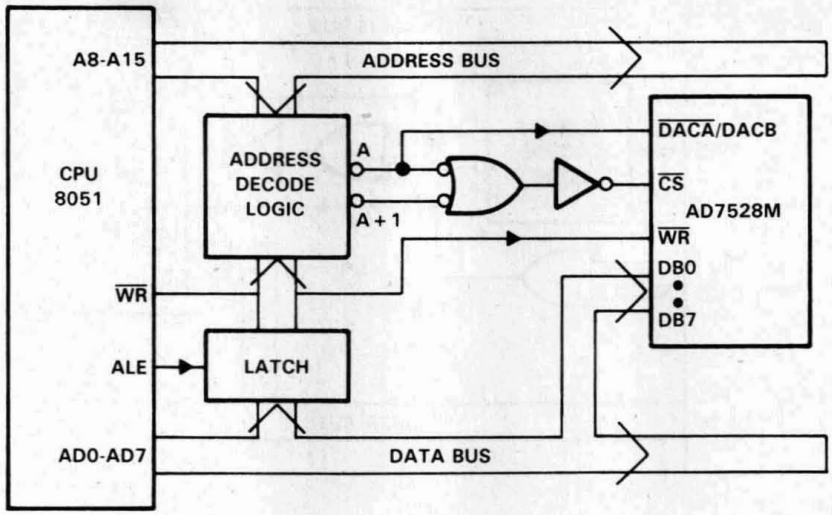
TABLE 2. BIPOLAR (OFFSET BINARY) CODE

DAC LATCH CONTENTS MSB LSB‡	ANALOG OUTPUT
11111111	V_i (127/128)
10000001	V_i (1/128)
10000000	0 V
01111111	$-V_i$ (1/128)
00000001	$-V_i$ (127/128)
00000000	$-V_i$ (128/128)

‡ 1 LSB = $(2^{-7})V_i$

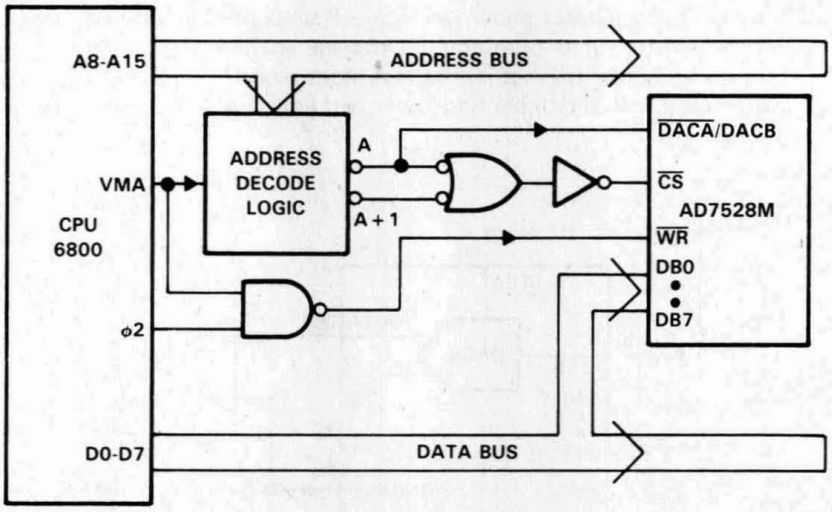
APPLICATION DATA

microprocessor interface information



NOTE: A = decoded address for AD7528M DACA.
A + 1 = decoded address for AD7528M DACB.

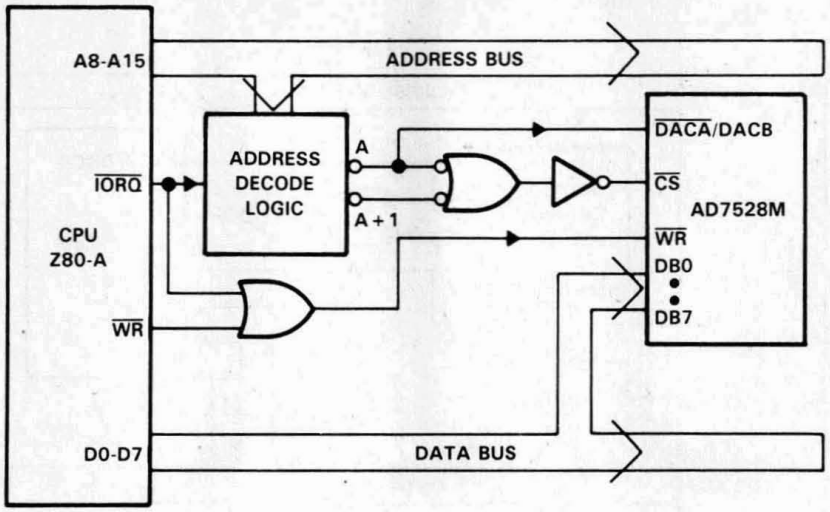
FIGURE 5. AD7528M – INTEL 8051 INTERFACE



NOTE: A = decoded address for AD7528M DACA.
A + 1 = decoded address for AD7528M DACB.

FIGURE 6. AD7528M – 6800 INTERFACE

APPLICATION DATA



NOTE: A = decoded address for AD7528M DACA.
A+1 = decoded address for AD7528M DACB.

FIGURE 7. AD7528M TO Z-80A INTERFACE

programmable window detector

The programmable window comparator shown in Figure 8 will determine if voltage applied to the DAC feedback resistors are within the limits programmed into the AD7528M data latches. Input signal range depends on the reference and polarity, that is, the test input range is 0 to $-V_{ref}$. The DACA and DACB data latches are programmed with the upper and lower test limits. A signal within the programmed limits will drive the output high.

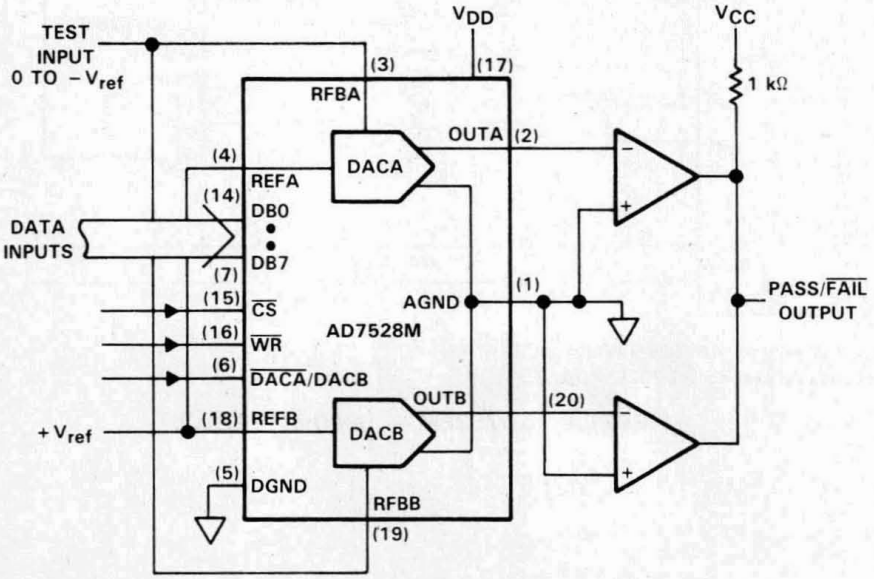


FIGURE 8. DIGITALLY PROGRAMMABLE WINDOW COMPARATOR (UPPER- AND LOWER-LIMIT TESTER)

APPLICATION DATA

digitally controlled signal attenuator

Figure 9 shows the AD7528M configured as a two-channel programmable attenuator. Applications include stereo audio and telephone signal level control. Table 3 shows input codes vs attenuation for a 0 to 15.5 dB range.

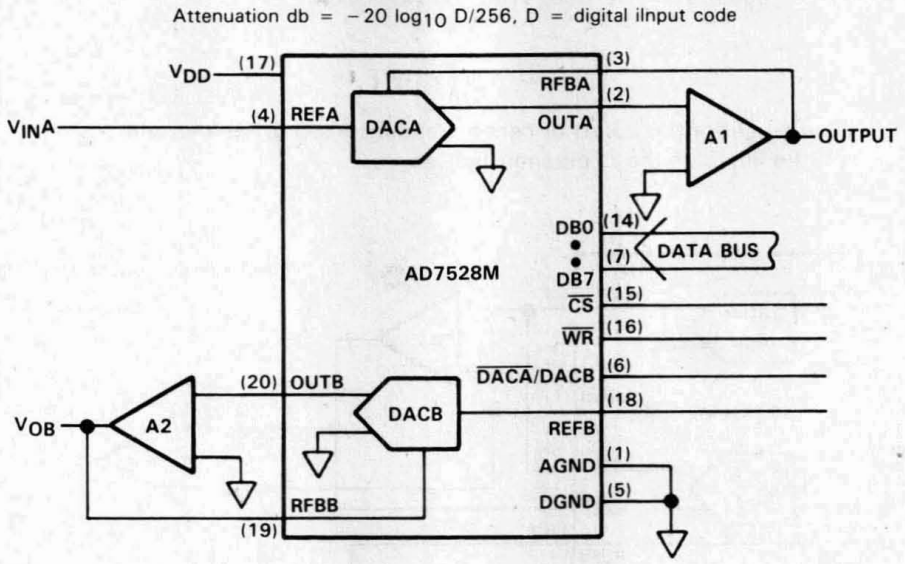


FIGURE 9. DIGITALLY CONTROLLED DUAL TELEPHONE ATTENUATOR

TABLE 3. ATTENUATION vs DACA, DACB CODE

ATTN(dB)	DAC INPUT CODE	CODE IN DECIMAL	ATTN(dB)	DAC INPUT CODE	CODE IN DECIMAL
0	11111111	255	8.0	01100110	102
0.5	11110010	242	8.5	01100000	96
1.0	11100100	228	9.0	01011011	91
1.5	11010111	215	9.5	01010110	86
2.0	11001011	203	10.0	01010001	81
2.5	11000000	192	10.5	01001100	76
3.0	10110101	181	11.0	01001000	72
3.5	10101011	171	11.5	01000100	68
4.0	10100010	162	12.0	01000000	64
4.5	10011000	152	12.5	00111101	61
5.0	10010000	144	13.0	00111001	57
5.5	10001000	136	13.5	00110110	54
6.0	10000000	128	14.0	00110011	51
6.5	01111001	121	14.5	00110000	48
7.0	01110010	114	15.0	00101110	46
7.5	01101100	108	15.5	00101011	43

APPLICATION DATA

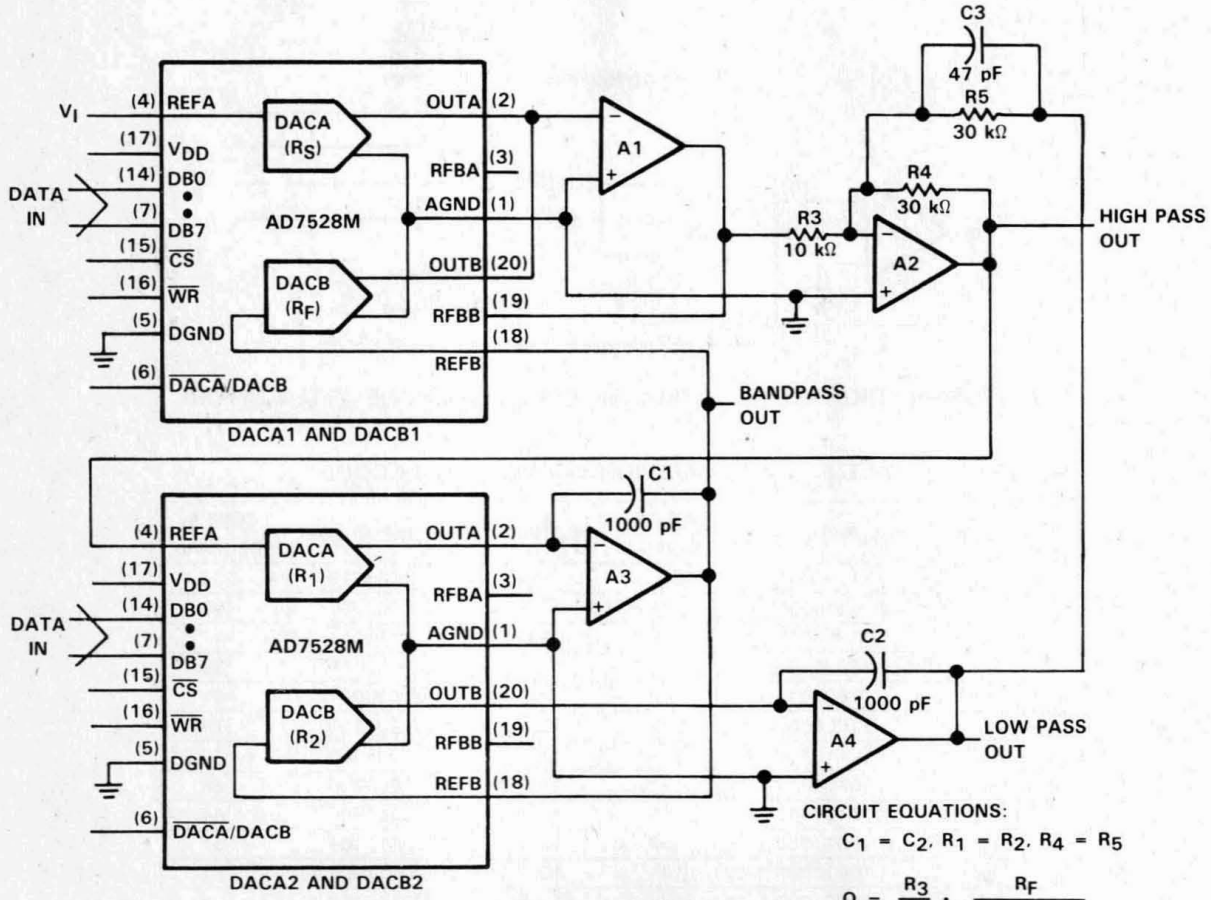
programmable state-variable filter

This programmable state-variable or universal filter configuration provides low-pass, high-pass, and band-pass outputs, and is suitable for applications in which microprocessor control of filter parameters is required.

As shown in Figure 10, DACA1 and DACB1 control the gain and Q of the filter while DACA2 and DACB2 control the cutoff frequency. Both halves of the DACA2 and DACB2 must track accurately in order for the cutoff-frequency equation to be true. With the AD7528M, this is easily achieved.

$$f_C = \frac{1}{2\pi\ R1\ C1}$$

The programmable range for the cutoff or center frequency is 0 to 15 kHz with a Q ranging from 0.3 to 4.5. This defines the limits of the component values.



NOTES: A. Op-amps A1, A2, A3, and A4 are TL287.

B. C3 compensates for the op-amp gain-bandwidth limitations.

C. DAC equivalent resistance equals $\frac{256 \times \text{(DAC ladder resistance)}}{\text{DAC digital code}}$

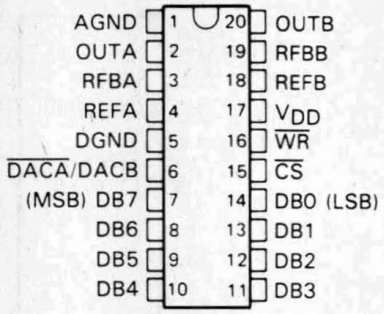
FIGURE 10. DIGITALLY CONTROLLED STATE-VARIABLE FILTER

AD7628
Advanced LinCMOS™ DUAL 8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

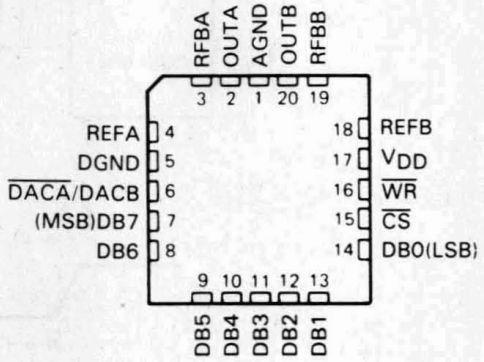
D3198, JANUARY 1989 – REVISED FEBRUARY 1990

- **Advanced LinCMOS™ Silicon-Gate Technology**
- **Easy Microprocessor Interface**
- **On-Chip Data Latches**
- **Digital Inputs are TTL-Compatible with 10.8-V to 15.75-V Power Supply**
- **Monotonic Over the Entire A/D Conversion Range**
- **Designed to be Interchangeable with Analog Devices AD7628**
- **Fast Control Signaling for Digital Signal Processor Applications Including Interface with TMS320**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The AD7628 is a dual 8-bit digital-to-analog converter designed with separate on-chip data latches and featuring excellent DAC-to-DAC matching. Data is transferred to either of the two DAC data latches via a common 8-bit input port. Control input $\overline{\text{DACA}}$/DACB determines which DAC is loaded. The ''load'' cycle of the AD7628 is similar to the ''write'' cycle of a random-access memory, allowing easy interface to most popular microprocessor buses and output ports. Segmenting the high-order bits minimizes glitches during changes in the most significant bits, where glitch impulse is typically the strongest.

The AD7628 operates from a 10.8-V to 15.75-V power supply and is TTL-compatible over this range. Excellent 2- or 4-quadrant multiplying makes the AD7628 a sound choice for many microprocessor-controlled gain-setting and signal-control applications.

The AD7628B is characterized for operation from −25°C to 85°C. The AD7628K is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING TEMPERATURE RANGE
DEVICE	PACKAGE SUFFIX	
AD7628B	FN, N	−25°C to 85°C
AD7628K	FN, N	0°C to 70°C

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage.

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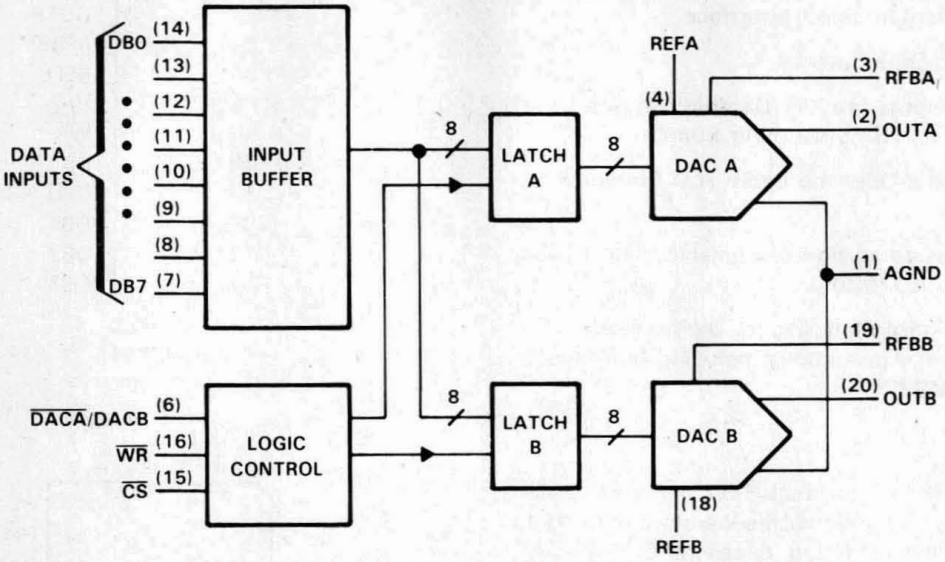
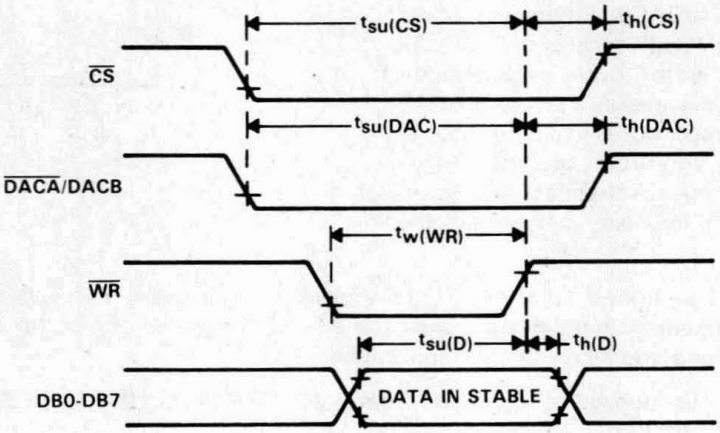
functional block diagram



operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{DD} (to AGND or DGND) . . . . . −0.3 V to 17 V
Voltage between AGND and DGND . . . . . $\pm V_{DD}$
Input voltage range, V_I (to DGND) . . . . . −0.3 V to V_{DD} +0.3 V
Reference voltage, V_{refA} or V_{refB} (to AGND) . . . . . ±25 V
Feedback voltage, V_{RFBA} or V_{RFBB} (to AGND) . . . . . ±25 V
Output voltage, V_{OA} or V_{OB} (to AGND) . . . . . ±25 V
Peak input current . . . . . 10 μA
Operating free-air temperature range: AD7628B . . . . . −25°C to 85°C
AD7628K . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		10.8		15.75	V
Reference voltage, V_{refA} or V_{refB}			±10		V
High-level input voltage, V_{IH}		2.4			V
Low-level input voltage, V_{IL}				0.8	V
$\overline{CS}$ setup time, $t_{su(CS)}$		50			ns
$\overline{CS}$ hold time, $t_{h(CS)}$		10			ns
DAC select setup time, $t_{su(DAC)}$		60			ns
DAC select hold time, $t_{h(DAC)}$		10			ns
Data bus input setup time $t_{su(D)}$		25			ns
Data bus input hold time $t_{h(D)}$		10			ns
Pulse duration, $\overline{WR}$ low, $t_{w(WR)}$		50			ns
Operating free-air temperature, T_A	AD7628B	−25		85	°C
	AD7628K	0		70	

electrical characteristics over recommended ranges of operating free-air temperature and V_{DD}, $V_{refA} = V_{refB} = 10$ V, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
I_{IH}	High-level input current		$V_I = V_{DD}$	Full Range		10	μA
				25°C		1	
I_{IL}	Low-level input current		$V_I = 0$	Full Range		−10	μA
				25°C		−1	
	Reference input impedance (Pin 15 to GND)				8	15	kΩ
I_{lkg}	Output leakage current	OUTA	DAC data latch loaded with 00000000, $V_{refA} = \pm 10$ V	Full Range		±200	nA
				25°C		±50	
		OUTB	DAC data latch loaded with 00000000, $V_{refB} = \pm 10$ V	Full Range		±200	
				25°C		±50	
	Input resistance match (REFA to REFB)					±1%	
	DC supply sensitivity $\Delta gain/\Delta V_{DD}$		$\Delta V_{DD} = \pm 5\%$	Full Range		0.02	%/%
				25°C		0.01	
I_{DD}	Supply current	Quiescent	DB0-DB7 at V_{IH}min or V_{IL}max			2	mA
		Standby	DB0-DB7 at 0 V or V_{DD}	Full Range		0.5	
				25°C		0.1	
C_i	Input capacitance	DB0-DB7	$V_I = 0$ or V_{DD}			10	pF
		$\overline{WR}$, $\overline{CS}$, $\overline{DACA}$/DACB				15	
C_o	Output capacitance (OUTA, OUTB)		DAC Data latches loaded with 00000000			25	pF
			DAC Data latches loaded with 11111111			60	

operating characteristics over recommended ranges of operating free-air temperature and V_{DD}, $V_{refA} = V_{refB} = 10$ V, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Linearity error						±1/2	LSB
Setting time (to 1/2 LSB)		See Note 1				100	ns
Gain error		See Note 2	Full Range			±3	LSB
			25°C			±2	
AC feedthrough	REFA to OUTA	See Note 3	Full Range			−65	dB
	REFB to OUTB		25°C			−70	
Temperature coefficient of gain						0.0035	%FSR/°C
Propagation delay (from digital input to 90% of final analog output current)		See Note 4				80	ns
Channel-to-channel isolation	REFA to OUTB	See Note 5	25°C		80		dB
	REFB to OUTA	See Note 6	25°C		80		
Digital-to-analog glitch impulse area		Measured for code transition from 00000000 to 11111111, T_A = 25°C			330		nV•s
Digital crosstalk glitch impulse area		Measured for code transition from 00000000 to 11111111, T_A = 25°C			60		nV•s
Harmonic distortion		V_i = 6 V, f = 1 kHz, T_A = 25°C			−85		dB

NOTES: 1. OUTA, OUTB load = 100 Ω, C_{ext} = 13 pF; $\overline{WR}$ and $\overline{CS}$ at 0 V; DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
2. Gain error is measured using an internal feedback resistor. Nominal Full Scale Range (FSR) = V_{ref} − 1 LSB. Both DAC latches are loaded with 11111111.
3. V_{ref} = 20 V peak-to-peak, 10-kHz sine wave.
4. $V_{refA} = V_{refB}$ = 10 V; OUTA/OUTB load = 100 Ω, C_{ext} = 13 pF; $\overline{WR}$ and $\overline{CS}$ at 0 V; DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
5. V_{refA} = 20 V peak-to-peak, 10-kHz sine wave; V_{refB} = 0.
6. V_{refB} = 20 V peak-to-peak, 10-kHz sine wave; V_{refA} = 0.

principles of operation

The AD7628 contains two identical 8-bit multiplying D/A converters, DACA and DACB. Each DAC consists of an inverted R-2R ladder, analog switches, and input data latches. Binary-weighted currents are switched between DAC output and AGND, thus maintaining a constant current in each ladder leg independent of the switch state. Most applications require only the addition of an external operational amplifier and voltage reference. A simplified D/A circuit for DACA with all digital inputs low is shown in Figure 1.

Figure 2 shows the DACA equivalent circuit. A similar equivalent circuit can be drawn for DACB. Both DACs share the analog ground pin 1 (AGND). With all digital inputs high, the entire reference current flows to OUTA. A small leakage current (I_{lkg}) flows across internal junctions, and as with most semiconductor devices, doubles every 10°C. C_O is due to the parallel combination of the NMOS switches and has a value that depends on the number of switches connected to the output. The range of C_O is 25 pF to 60 pF maximum. The equivalent output resistance r_O varies with the input code from 0.8R to 3R where R is the nominal value of the ladder resistor in the R-2R network.

Interfacing the AD7628 to a microprocessor is accomplished via the data bus, $\overline{CS}$, $\overline{WR}$, and $\overline{DACA}$/DACB control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, the AD7628 analog output, specified by the $\overline{DACA}$/DACB control line, responds to the activity on the DB0-DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the $\overline{CS}$ signal or $\overline{WR}$ signal goes high, the data on the DB0-DB7 inputs is latched until the $\overline{CS}$ and $\overline{WR}$ signals go low again. When $\overline{CS}$ is high, the data inputs are disabled, regardless of the state of the $\overline{WR}$ signal.

The digital inputs of the AD7628 provide TTL compatibility when operated from a supply voltage of 10.8 V to 15.75 V.

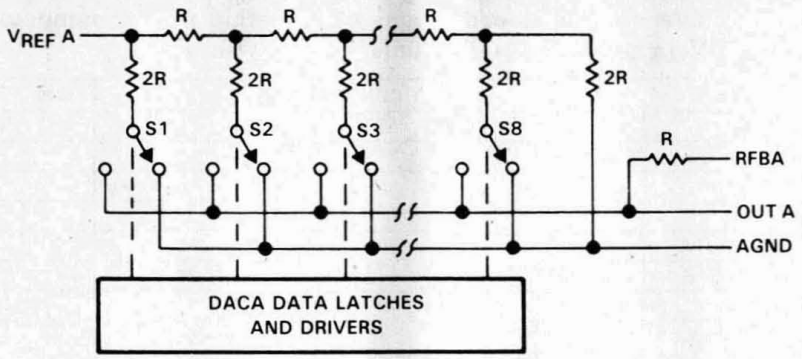


FIGURE 1. SIMPLIFIED FUNCTIONAL CIRCUIT FOR DACA

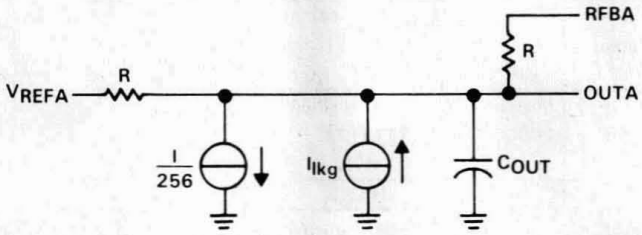


FIGURE 2. AD7628 EQUIVALENT CIRCUIT, DACA LATCH LOADED WITH 11111111.

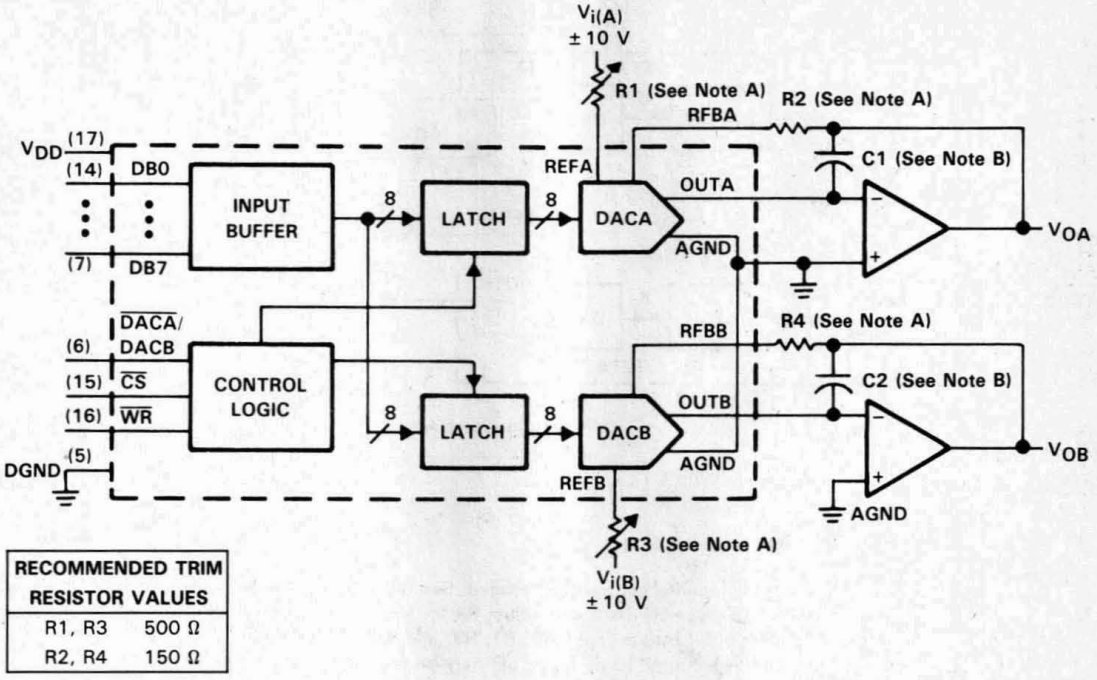
MODE SELECTION TABLE

$\overline{DACA}$/DACB	$\overline{CS}$	$\overline{WR}$	DACA	DACB
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = low level, H = high level, X = don't care

TYPICAL APPLICATION DATA

The AD7628 is capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant and 4-quadrant multiplication are shown in Figures 3 and 4. Input coding for unipolar and bipolar operation are summarized in Tables 1 and 2, respectively.



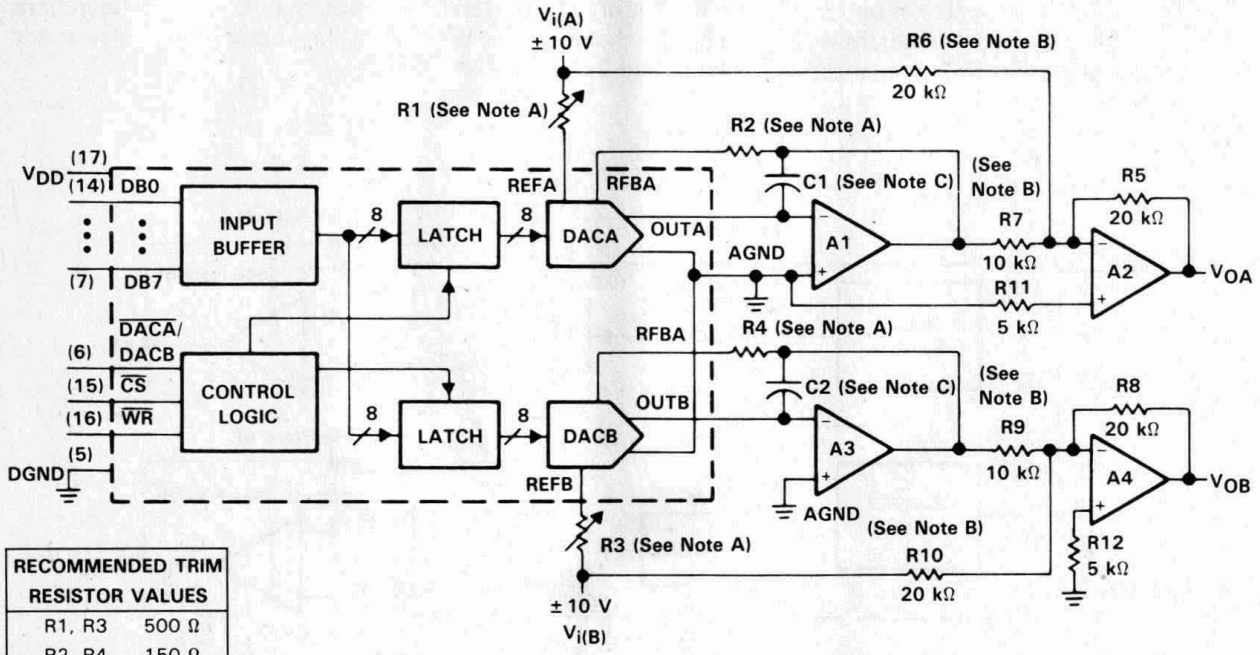
RECOMMENDED TRIM RESISTOR VALUES	
R1, R3	500 Ω
R2, R4	150 Ω

NOTES: A. R1, R2, R3, and R4 are used only if gain adjustment is required. See table for recommended values. Make gain adjustment with digital input of 255.

B. C1 and C2 phase compensation capacitors (10 pF to 15 pF) are required when using high-speed amplifiers to prevent ringing or oscillation.

FIGURE 3. UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)

TYPICAL APPLICATION DATA



RECOMMENDED TRIM RESISTOR VALUES	
R1, R3	500 Ω
R2, R4	150 Ω

NOTES: A. R1, R2, R3, and R4 are used only if gain adjustment is required. See table in Figure 3 for recommended values. Adjust R1 for V_{OA} = 0 V with code 10000000 in DACA latch. Adjust R3 for V_{OB} = 0 V with 10000000 in DACB latch.
B. Matching and tracking are essential for resistor pairs R6, R7, R9, and R10.
C. C1 and C2 phase compensation capacitors (10 pF to 15 pF) may be required if A1 and A3 are high-speed amplifiers.

FIGURE 4. BIPOLAR OPERATION (4-QUADRANT OPERATION)

TABLE 1. UNIPOLAR BINARY CODE

DAC LATCH CONTENTS MSB LSB†	ANALOG OUTPUT
11111111	$-V_i$ (255/256)
10000001	$-V_i$ (129/256)
10000000	$-V_i$ (128/256) = $-V_i/2$
01111111	$-V_i$ (127/256)
00000001	$-V_i$ (1/256)
00000000	$-V_i$ (0/256) = 0

† 1 LSB = $(2^{-8})V_i$

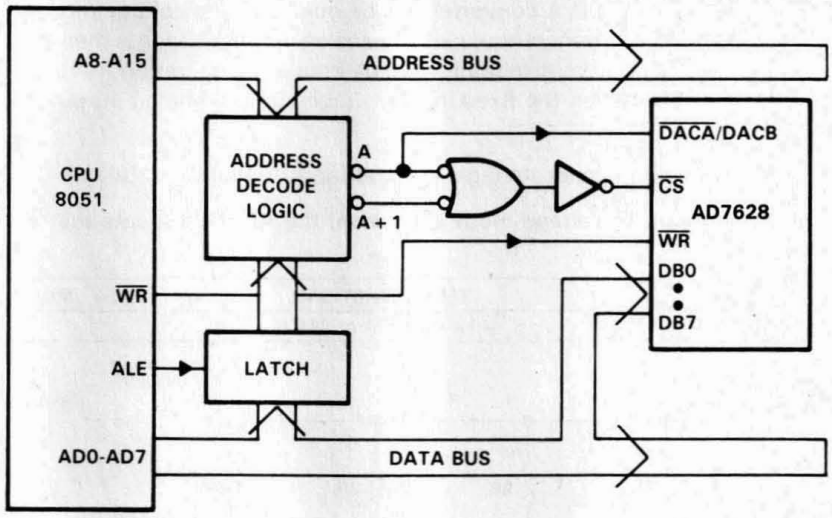
TABLE 2. BIPOLAR (OFFSET BINARY) CODE

DAC LATCH CONTENTS MSB LSB‡	ANALOG OUTPUT
11111111	V_i (127/128)
10000001	V_i (1/128)
10000000	0 V
01111111	$-V_i$ (1/128)
00000001	$-V_i$ (127/128)
00000000	$-V_i$ (128/128)

‡ 1 LSB = $(2^{-7})V_i$

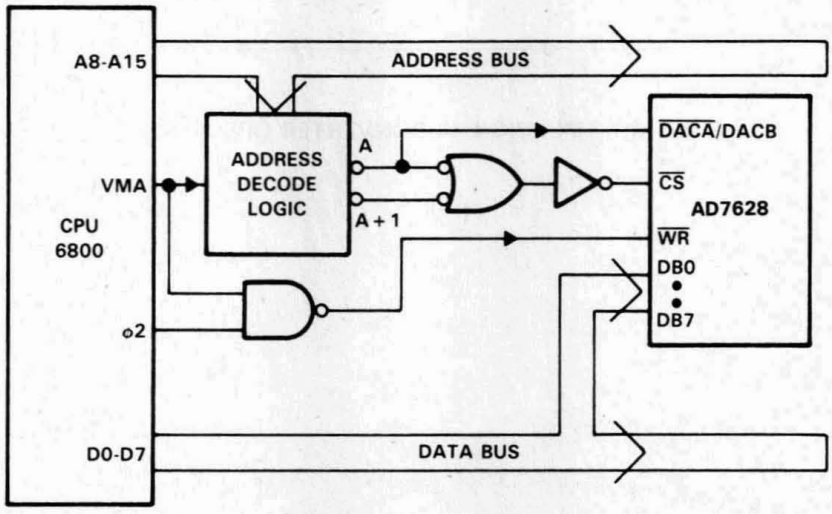
TYPICAL APPLICATION DATA

microprocessor interface information



NOTE: A = decoded address for AD7628 DACA.
A+1 = decoded address for AD7628 DACB.

FIGURE 5. AD7628 – INTEL 8051 INTERFACE



NOTE: A = decoded address for AD7628 DACA.
A+1 = decoded address for AD7628 DACB.

FIGURE 6. AD7628 – 6800 INTERFACE

TYPICAL APPLICATION DATA

voltage-mode operation

The AD7628 current-multiplying D/A converter can be operated in a voltage mode. In the voltage mode, a fixed voltage is placed on the current output pin. The analog output voltage is then available at the reference voltage pin. An example of a current-multiplying D/A converter operating in voltage mode is shown in Figure 7. The relationship between the fixed input voltage and the analog output voltage is given by the following equation:

$$\text{Analog output voltage} = \text{fixed input voltage } (D/256)$$

where D = the digital input. In voltage-mode operation, the AD7628 meets the following specification:

LINEARITY ERROR	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog output voltage for REFA, B	V_{DD} = 12 V, OUTA or OUTB = 5 V			1	LSB

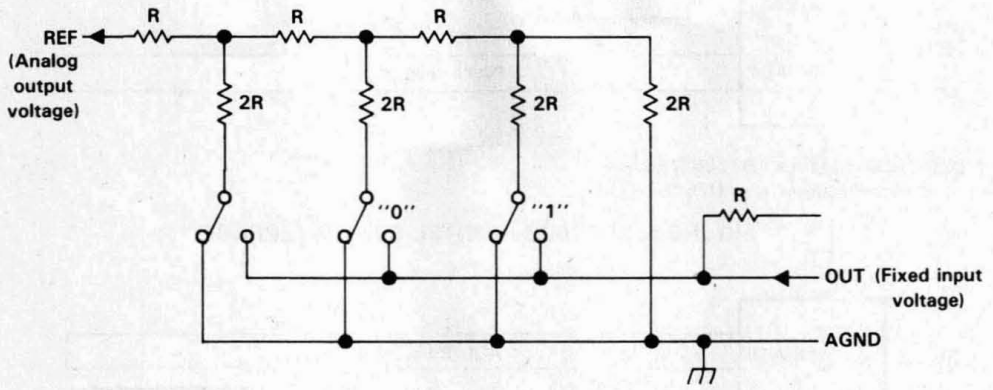


FIGURE 7. CURRENT-MULTIPLYING D/A CONVERTER OPERATING IN VOLTAGE MODE

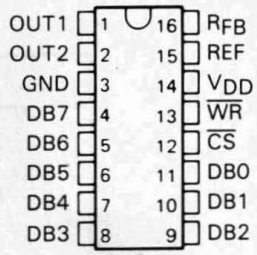
TLC7524
Advanced LinCMOS™ 8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

D3008, SEPTEMBER 1986—REVISED AUGUST 1991

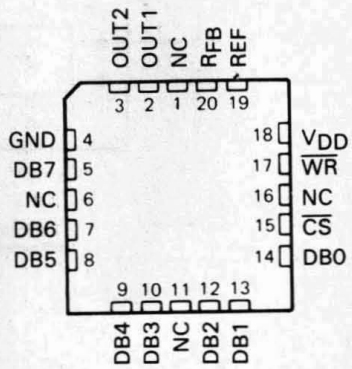
- **Advanced LinCMOS™ Silicon-Gate Technology**
- **Easily Interfaced to Microprocessors**
- **On-Chip Data Latches**
- **Monotonic over the Entire A/D Conversion Range**
- **Segmented High-Order Bits Ensure Low-Glitch Output**
- **Designed to be Interchangeable with Analog Devices AD7524, PMI PM-7524, and Micro Power Systems MP7524**
- **Fast Control Signaling for Digital Signal Processor Applications Including Interface with TMS320**

KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 Bits
Linearity error	½ LSB Max
Power dissipation at V_{DD} = 5 V	5 mW Max
Settling time	100 ns Max
Propagation delay	80 ns Max

D OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

The TLC7524 is an Advanced LinCMOS™ 8-bit digital-to-analog converter (DAC) designed for easy interface to most popular microprocessors.

The TLC7524 is an 8-bit multiplying DAC with input latches and with a load cycle similar to the "write" cycle of a random access memory. Segmenting the high-order bits minimizes glitches during changes in the most-significant bits, which produce the highest glitch impulse. The TLC7524 provides accuracy to ½ LSB without the need for thin-film resistors or laser trimming, while dissipating less than 5 milliwatts typically.

Featuring operation from a 5-V to 15-V single supply, the TLC7524 interfaces easily to most microprocessor buses or output ports. Excellent multiplying (2 or 4 quadrant) makes the TLC7524 an ideal choice for many microprocessor-controlled gain-setting and signal-control applications.

The TLC7524C is characterized for operation from 0°C to 70°C. The TLC7524I is characterized for operation from −25°C to 85°C. The TLC7524 E is characterized for operation from −40°C to 85°C.

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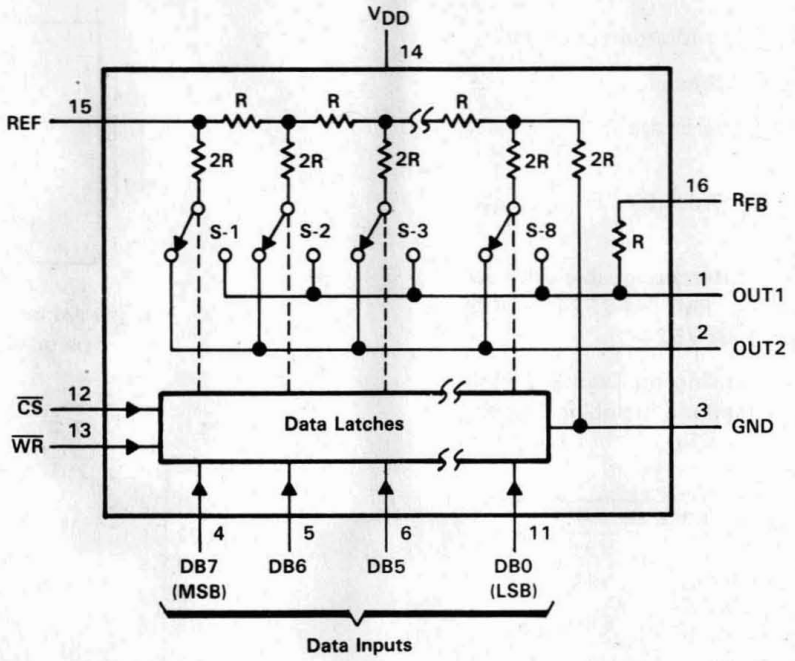
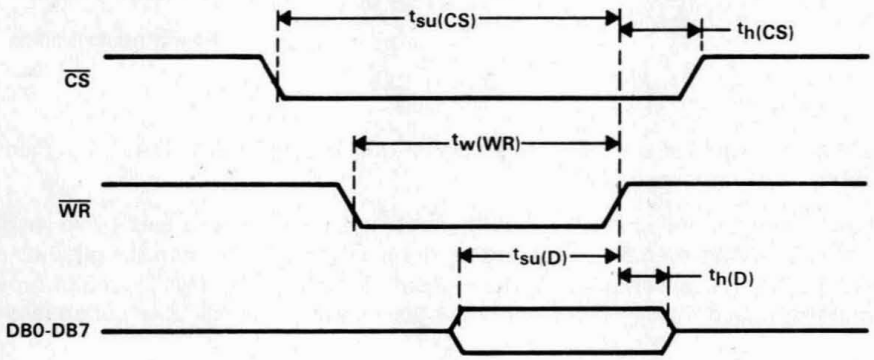
functional block diagram



operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{DD} . . . . . −0.3 V to 16.5 V
Digital input voltage range, V_I . . . . . −0.3 V to V_{DD} +0.3 V
Reference voltage, V_{ref} . . . . . ±25 V
Peak digital input current, I_I . . . . . 10 μA
Operating free-air temperature range: TLC7524C . . . . . 0°C to 70°C
TLC7524I . . . . . −25°C to 85°C
TLC7524E . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

recommended operating conditions

		V_{DD} = 5 V			V_{DD} = 15 V			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4.75	5	5.25	14.5	15	15.5	V
Reference voltage, V_{ref}			±10			±10		V
High-level input voltage, V_{IH}		2.4			13.5			V
Low-level input voltage, V_{IL}				0.8			1.5	V
CS setup time, $t_{su(CS)}$		40			40			ns
CS hold time, $t_{h(CS)}$		0			0			ns
Data bus input setup time, $t_{su(D)}$		25			25			ns
Data bus input hold time, $t_{h(D)}$		10			10			ns
Pulse duration, $\overline{WR}$ low, $t_{w(WR)}$		40			40			ns
Operating free-air temperature, T_A	TLC7524C	0		70	0		70	°C
	TLC7524I	−25		85	−25		85	
	TLC7524E	−40		85	−40		85	

electrical characteristics over recommended operating free-air temperature range, V_{ref} = ±10 V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{DD} = 5 V			V_{DD} = 15 V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{IH}	High-level input current		$V_I = V_{DD}$			10			10	μA
I_{IL}	Low-level input current		V_I = 0			−10			−10	μA
I_{lkg}	Output leakage current	OUT1	DB0-DB7 at 0 V, $\overline{WR}$, $\overline{CS}$ at 0 V, V_{ref} = ±10 V			±400			±200	nA
		OUT2	DB0-DB7 at V_{DD}, $\overline{WR}$, $\overline{CS}$ at 0 V, V_{ref} = ±10 V			±400			±200	
I_{DD}	Supply current	Quiescent	DB0-DB7 at V_{IH}min or V_{IL}max			1			2	mA
		Standby	DB0-DB7 at 0 V or V_{DD}			500			500	μA
k_{SVS}	Supply voltage sensitivity, $\Delta gain/\Delta V_{DD}$		ΔV_{DD} = ±10%		0.01	0.16		0.005	0.04	%FSR/%
C_i	Input capacitance, DB0-DB7, $\overline{WR}$, $\overline{CS}$		V_I = 0			5			5	pF
C_o	Output capacitance	OUT1	DB0-DB7 at 0 V, $\overline{WR}$ and $\overline{CS}$ at 0 V			30			30	pF
		OUT2				120			120	
C_o	Output capacitance	OUT1	DB0-DB7 at V_{DD}, $\overline{WR}$ and $\overline{CS}$ at 0 V			120			120	pF
		OUT2				30			30	
	Reference input impedance (Pin 15 to GND)			5		20	5		20	kΩ

operating characteristics over recommended operating free-air temperature range, V_{ref} = ±10 V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{DD} = 5 V			V_{DD} = 15 V			UNIT
		MIN	TYP	MAX	MIN	TYP†	MAX	
Linearity error				±0.5			±0.5	LSB
Gain error	See Note 1			±2.5			±2.5	LSB
Settling time (to ½ LSB)	See Note 2			100			100	ns
Propagation delay from digital input to 90% of final analog output current	See Note 2			80			80	ns
Feedthrough at OUT1 or OUT2	V_{ref} = ±10 V (100-kHz sinewave) $\overline{WR}$ and $\overline{CS}$ at 0 V, DB0-DB7 at 0 V			0.5			0.5	%FSR
Temperature coefficient of gain	T_A = 25°C to MAX		±0.004			±0.001		%FSR/°C

NOTES: 1. Gain error is measured using the internal feedback resistor. Nominal Full Scale Range (FSR) = V_{ref} − 1 LSB.
2. OUT1 load = 100 Ω, C_{ext} = 13 pF, $\overline{WR}$ at 0 V, $\overline{CS}$ at 0 V, DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.

principles of operation

The TLC7524 is an 8-bit multiplying D/A converter consisting of an inverted R-2R ladder, analog switches, and data input latches. Binary weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state. The high-order bits are decoded and these decoded bits, through a modification in the R-2R ladder, control three equally weighted current sources. Most applications only require the addition of an external operational amplifier and a voltage reference.

The equivalent circuit for all digital inputs low is seen in Figure 1. With all digital inputs low, the entire reference current, I_{ref}, is switched to OUT2. The current source I/256 represents the constant current flowing through the termination resistor of the R-2R ladder, while the current source I_{lkg} represents leakage currents to the substrate. The capacitances appearing at OUT1 and OUT2 are dependent upon the digital input code. With all digital inputs high, the off-state switch capacitance (30 pF maximum) appears at OUT2 and the on-state switch capacitance (120 pF maximum) appears at OUT1. With all digital inputs low, the situation is reversed as shown in Figure 1. Analysis of the circuit for all digital inputs high is similar to Figure 1; however, in this case, I_{ref} would be switched to OUT1.

Interfacing the TLC7524 D/A converter to a microprocessor is accomplished via the data bus and the $\overline{CS}$ and $\overline{WR}$ control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, the TLC7524 analog output responds to the data activity on the DB0-DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the $\overline{CS}$ signal or $\overline{WR}$ signal goes high, the data on the DB0-DB7 inputs are latched until the $\overline{CS}$ and $\overline{WR}$ signals go low again. When $\overline{CS}$ is high, the data inputs are disabled regardless of the state of the $\overline{WR}$ signal.

The TLC7524 is capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant or 4-quadrant multiplication are shown in Figures 2 and 3. Input coding for unipolar and bipolar operation are summarized in Tables 1 and 2, respectively.

principles of operation (continued)

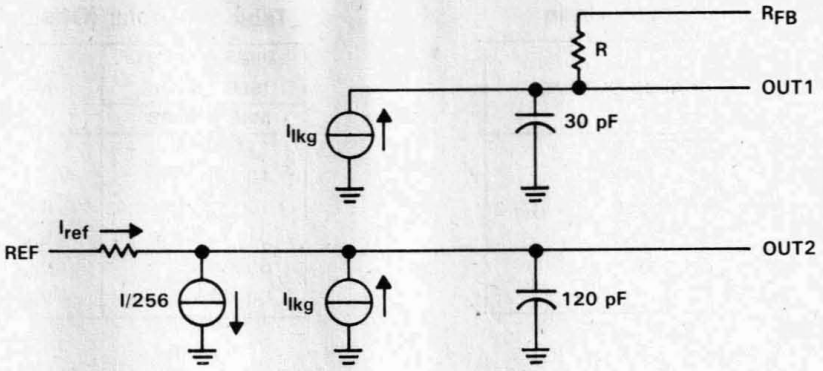


Figure 1. TLC7524 Equivalent Circuit With All Digital Inputs Low

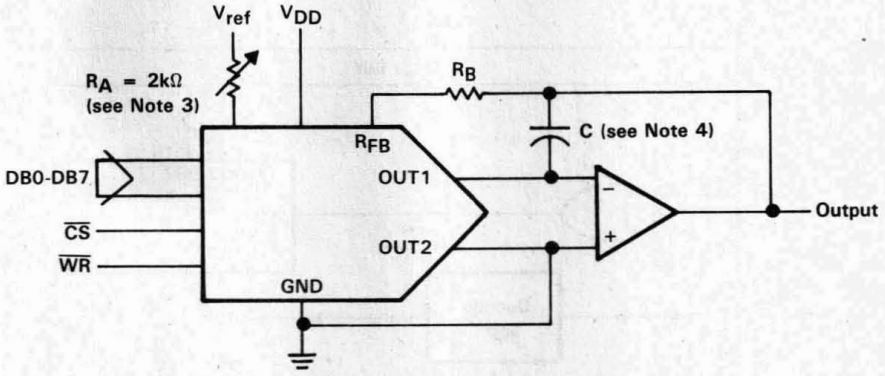


Figure 2. Unipolar Operation (2-Quadrant Multiplication)

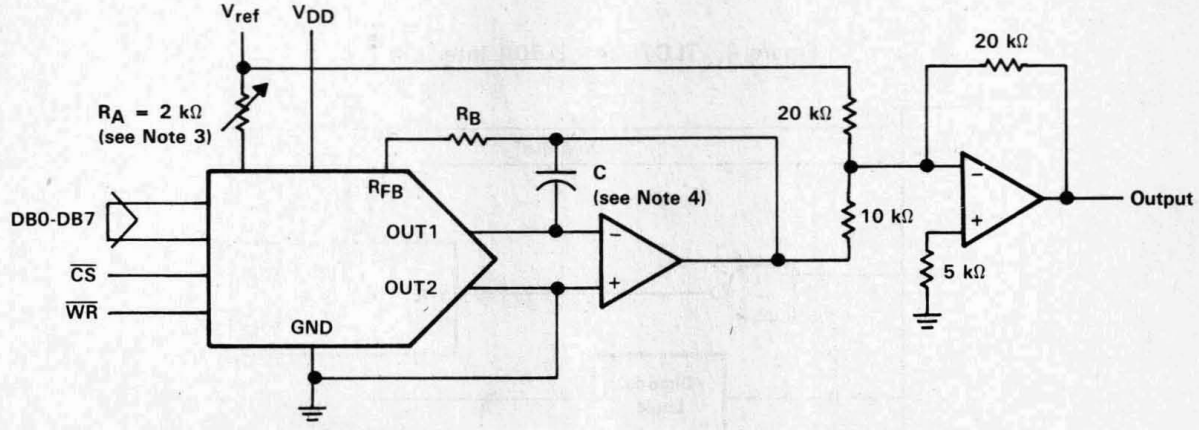


Figure 3. Bipolar Operation (4-Quadrant Operation)

NOTES: 3. R_A and R_B used only if gain adjustment is required.
4. C phase compensation (10-15 pF) is required when using high-speed amplifiers to prevent ringing or oscillation.

principles of operation (continued)

Table 1. Unipolar Binary Code

DIGITAL INPUT (SEE NOTE 5) MSB LSB	ANALOG OUTPUT
11111111	$-V_{ref}$ (255/256)
10000001	$-V_{ref}$ (129/256)
10000000	$-V_{ref}$ (128/256) = $-V_{ref}/2$
01111111	$-V_{ref}$ (127/256)
00000001	$-V_{ref}$ (1/256)
00000000	0

Table 2. Bipolar (Offset Binary) Code

DIGITAL INPUT (SEE NOTE 6) MSB LSB	ANALOG OUTPUT
11111111	V_{ref} (127/128)
10000001	V_{ref} (1/128)
10000000	0
01111111	$-V_{ref}$ (1/128)
00000001	$-V_{ref}$ (127/128)
00000000	$-V_{ref}$

NOTES: 5. LSB = 1/256 (V_{ref}).
6. LSB = 1/128 (V_{ref}).

microprocessor interfaces

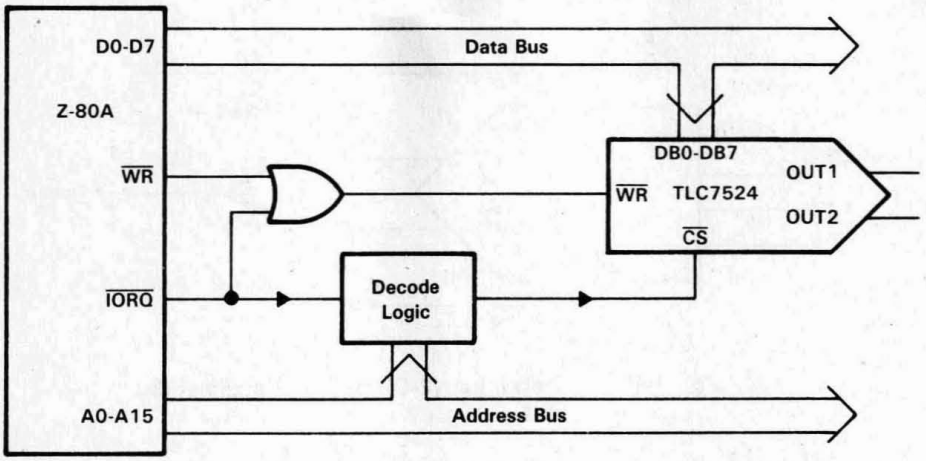


Figure 4. TLC7524—Z-80A Interface

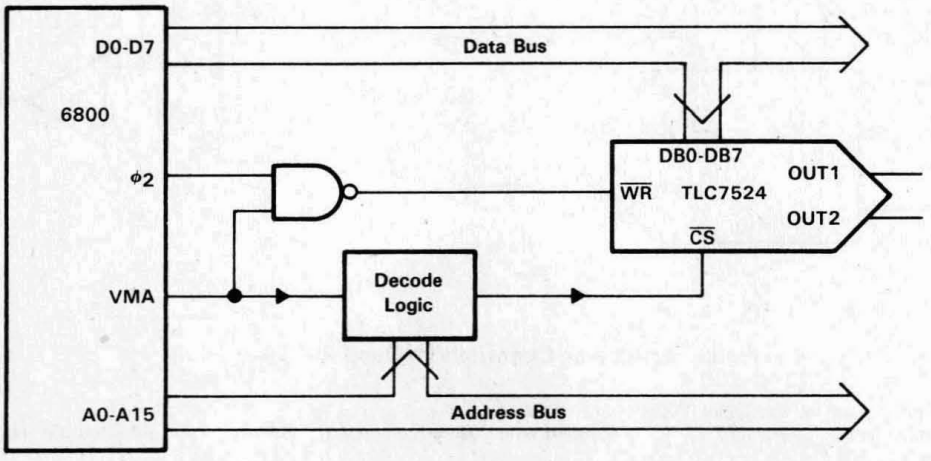


Figure 5. TLC7524—6800 Interface

microprocessor interfaces (continued)

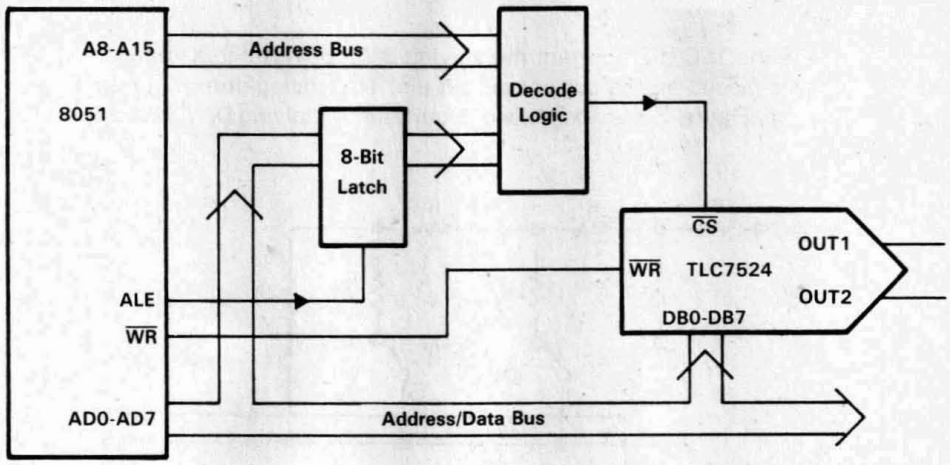


Figure 6. TLC7524—8051 Interface

APPLICATION INFORMATION

voltage-mode operation

It is possible to operate the TLC7524 current multiplying D/A converter in a voltage mode. In the voltage mode, a fixed voltage is placed on the current output pin. The analog output voltage is then available at the reference voltage pin. Figure 7 is an example of a current multiplying D/A, which is operated in voltage mode.

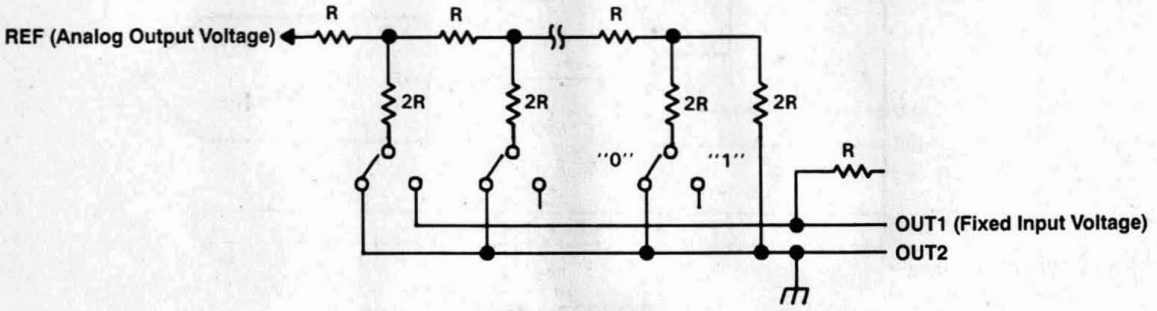


Figure 7. Voltage Mode Operation

The relationship between the fixed input voltage and the analog output voltage is given by the following equation:

$$V_O = V_I (D/256)$$

where

V_O = analog output voltage
V_I = fixed input voltage
D = digital input code converted to decimal

In voltage-mode operation, the TLC7524 will meet the following specification:

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Linearity error at REF	V_{DD} = 5 V, OUT1 = 2.5 V, OUT2 at GND, T_A = 0°C to 70°C		1	LSB

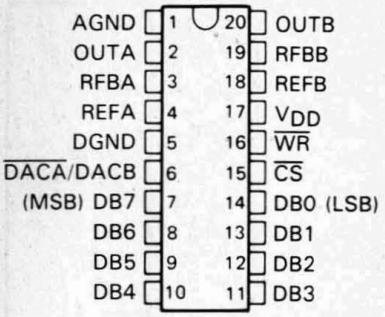
Advanced LinCMOS™ DUAL 8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

D2979, JANUARY 1987—REVISED AUGUST 1991

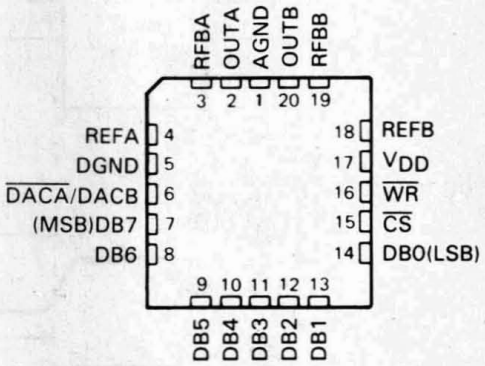
- **Advanced LinCMOS™ Silicon-Gate Technology**
- **Easily Interfaced to Microprocessors**
- **On-Chip Data Latches**
- **Monotonic Over the Entire A/D Conversion Range**
- **Designed to be Interchangeable with Analog Devices AD7528 and PMI PM-7528**
- **Fast Control Signaling for Digital Signal Processor Applications Including Interface with TMS320**
- **Voltage-Mode Operation**

KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 bits
Linearity Error	1/2 LSB
Power Dissipation at V_{DD} = 5 V	5 mW
Settling Time at V_{DD} = 5 V	100 ns
Propagation Delay at V_{DD} = 5 V	80 ns

DW OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The TLC7528 is a dual 8-bit digital-to-analog converter designed with separate on-chip data latches and featuring excellent DAC-to-DAC matching. Data is transferred to either of the two DAC data latches via a common 8-bit input port. Control input $\overline{\text{DACA}}$/DACB determines which DAC is to be loaded. The "load" cycle of the TLC7528 is similar to the "write" cycle of a random-access memory, allowing easy interface to most popular microprocessor busses and output ports. Segmenting the high-order bits minimizes glitches during changes in the most significant bits, where glitch impulse is typically the strongest.

The TLC7528 operates from a 5-V to 15-V power supply and dissipates less than 15 mW (typical). Excellent 2- or 4-quadrant multiplying makes the TLC7528 a sound choice for many microprocessor-controlled gain-setting and signal-control applications. It can be operated in voltage mode, which produces a voltage output rather than a current output. Refer to the typical application information in this data sheet.

The TLC7528C is characterized for operation from 0°C to 70°C. The TLC7528I is characterized for operation from −25°C to 85°C. The TLC7528E is characterized for operation from −40°C to 85°C.

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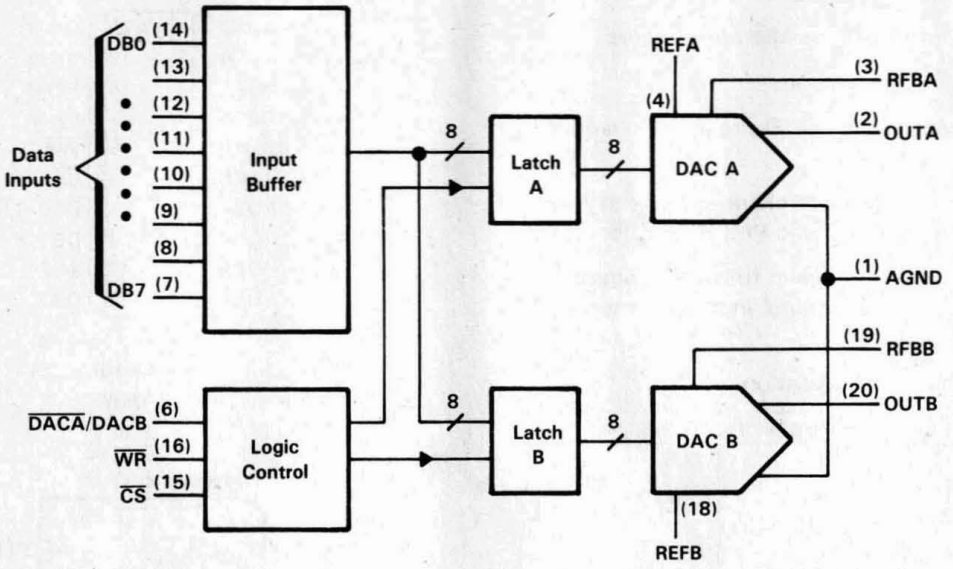
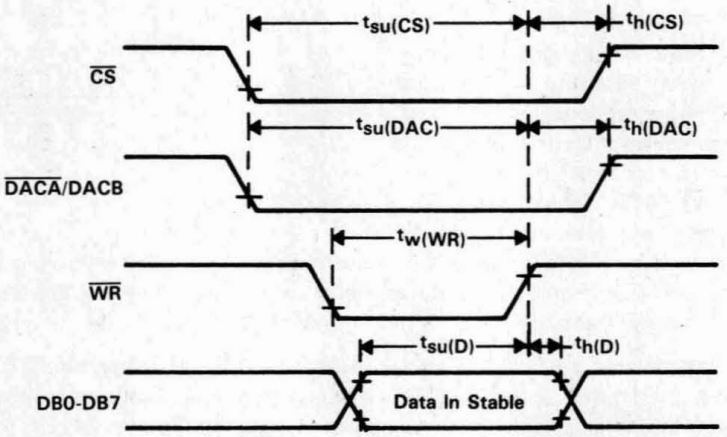
functional block diagram



operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{DD} (to AGND or DGND) . . . . . −0.3 V to 16.5 V
Voltage between AGND and DGND . . . . . ±V_{DD}
Input voltage range, V_I (to DGND) . . . . . −0.3 V to V_{DD} + 0.3
Reference voltage, V_{refA} or V_{refB} (to AGND) . . . . . ±25 V
Feedback voltage V_{RFBA} or V_{RFBB} (to AGND) . . . . . ±25 V
Output voltage, V_{OA} or V_{OB} (to AGND) . . . . . ±25 V
Peak input current . . . . . 10 μA
Operating free-air temperature range: TLC7528C . . . . . 0°C to 70°C
TLC7528I . . . . . −25°C to 85°C
TLC7528E . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package . . . . . 260°C

recommended operating conditions

		V_{DD} = 4.75 V to 5.25 V			V_{DD} = 14.5 V to 15.5 V			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Reference voltage, V_{refA} or V_{refB}			±10			±10		V
High-level input voltage, V_{IH}		2.4			13.5			V
Low-level input voltage, V_{IL}				0.8			1.5	V
$\overline{CS}$ setup time, $t_{su(CS)}$		50			50			ns
$\overline{CS}$ hold time, $t_{h(CS)}$		0			0			ns
DAC select setup time, $t_{su(DAC)}$		50			50			ns
DAC select hold time, $t_{h(DAC)}$		10			10			ns
Data bus input setup time $t_{su(D)}$		25			25			ns
Data bus input hold time $t_{h(D)}$		0			0			ns
Pulse duration, $\overline{WR}$ low, $t_{w(WR)}$		50			50			ns
Operating free-air temperature, T_A	TLC7528C	0		70	0		70	°C
	TLC7528I	−25		85	−25		85	
	TLC7528E	−40		85	−40		85	

electrical characteristics over recommended operating free-air temperature range, V_{refA} = V_{refB} = 10 V, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{DD} = 5 V			V_{DD} = 15 V			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{IH}	High-level input current		$V_I = V_{DD}$			10			10	μA
I_{IL}	Low-level input current		V_I = 0			−10			−10	μA
	Reference input impedance (Pin 15 to GND)			5	12	20	5	12	20	kΩ
I_{lkg}	Output leakage current	OUTA	DACA data latch loaded with 00000000, V_{refA} = ±10 V			±400			±200	nA
		OUTB	DACB data latch loaded with 00000000, V_{refB} = ±10 V			±400			±200	
	Input resistance match (REFA to REFB)					±1%			±1%	
	DC supply sensitivity, Δ gain/Δ V_{DD}		ΔV_{DD} = ±10%			0.04			0.02	%/%
I_{DD}	Supply current (quiescent)		DB0-DB7 at V_{IH}min or V_{IL}max			1			1	mA
I_{DD}	Supply current (standby)		DB0-DB7 at 0 V or V_{DD}			0.5			0.5	mA
C_i	Input capacitance	DB0-DB7				10			10	pF
		$\overline{WR}$, $\overline{CS}$ $\overline{DACA}$/DACB				15			15	
C_o	Output capacitance, (OUTA, OUTB)		DAC data latches loaded with 00000000			50			50	pF
			DAC data latches loaded with 11111111			120			120	

†All typical values are at T_A = 25°C.

operating characteristics over recommended operating free-air temperature range, V_{refA} = V_{refB} = 10 V, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{DD} = 5 V			V_{DD} = 15 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Linearity error					±1/2			±1/2	LSB
Settling time (to 1/2 LSB)		See Note 1			100			100	ns
Gain error		See Note 2			2.5			2.5	LSB
AC feedthrough	REFA to OUTA	See Note 3			−65			−65	dB
	REFB to OUTB				−65			−65	
Temperature coefficient of gain		See Note 4			0.007			0.0035	%FSR/°C
Propagation delay (from digital input to 90% of final analog output current)		See Note 5			80			80	ns
Channel-to-channel isolation	REFA to OUTB	See Note 6		77			77		dB
	REFB to OUTA	See Note 7		77			77		
Digital-to-analog glitch impulse area		Measured for code transition from 00000000 to 11111111, T_A = 25°C		160			440		nVs
Digital crosstalk glitch impulse area		Measured for code transition from 00000000 to 11111111, T_A = 25°C		30			60		nVs
Harmonic distortion		V_i = 6 V rms, f = 1 kHz, T_A = 25°C		−85			−85		dB

NOTES: 1. OUTA, OUTB load = 100 Ω, C_{ext} = 13 pF; $\overline{WR}$ and $\overline{CS}$ at 0 V; DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
2. Gain error is measured using an internal feedback resistor. Nominal Full Scale Range (FSR) = V_{ref} − 1 LSB.
3. V_{ref} = 20 V peak-to-peak, 100-kHz sine wave; DAC data latches loaded with 00000000.
4. Temperature coefficient of gain measured from 0°C to 25°C or from 25°C to 70°C.
5. V_{refA} = V_{refB} = 10 V; OUTA/OUTB load = 100 Ω, C_{ext} = 13 pF; $\overline{WR}$ and $\overline{CS}$ at 0 V; DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
6. Both DAC latches loaded with 11111111; V_{refA} = 20 V peak-to-peak, 100-kHz sine wave; V_{refB} = 0; T_A = 25°C.
7. Both DAC latches loaded with 11111111; V_{refB} = 20 V peak-to-peak, 100-kHz sine wave; V_{refA} = 0; T_A = 25°C.

principles of operation

The TLC7528 contains two identical 8-bit multiplying D/A converters, DACA and DACB. Each DAC consists of an inverted R-2R ladder, analog switches, and input data latches. Binary-weighted currents are switched between DAC output and AGND, thus maintaining a constant current in each ladder leg independent of the switch state. Most applications require only the addition of an external operational amplifier and voltage reference. A simplified D/A circuit for DACA with all digital inputs low is shown in Figure 1.

Figure 2 shows the DACA equivalent circuit. A similar equivalent circuit can be drawn for DACB. Both DACs share the analog ground pin 1 (AGND). With all digital inputs high, the entire reference current flows to OUTA. A small leakage current (I_{lkg}) flows across internal junctions, and as with most semiconductor devices, doubles every 10°C. C_O is due to the parallel combination of the NMOS switches and has a value that depends on the number of switches connected to the output. The range of C_O is 50 pF to 120 pF maximum. The equivalent output resistance r_O varies with the input code from 0.8R to 3R where R is the nominal value of the ladder resistor in the R-2R network.

Interfacing the TLC7528 to a microprocessor is accomplished via the data bus, $\overline{CS}$, $\overline{WR}$, and $\overline{DACA}$/DACB control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, the TLC7528 analog output, specified by the $\overline{DACA}$/DACB control line, responds to the activity on the DB0-DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the $\overline{CS}$ signal or $\overline{WR}$ signal goes high, the data on the DB0-DB7 inputs is latched until the $\overline{CS}$ and $\overline{WR}$ signals go low again. When $\overline{CS}$ is high, the data inputs are disabled regardless of the state of the $\overline{WR}$ signal.

The digital inputs of the TLC7528 provide TTL compatibility when operated from a supply voltage of 5 V. The TLC7528 may be operated with any supply voltage in the range from 5 V to 15 V, however, input logic levels are not TTL compatible above 5 V.

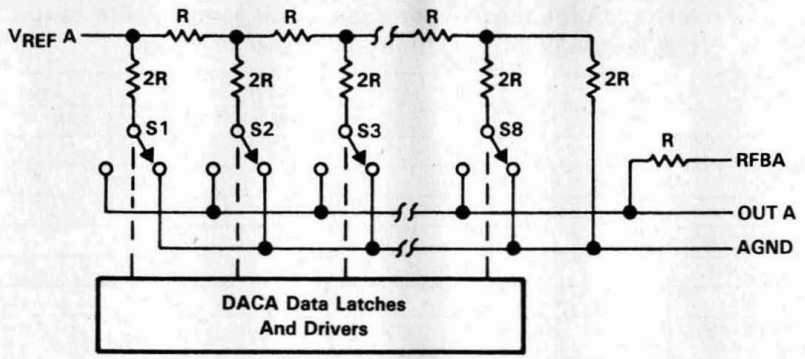


Figure 1. Simplified Functional Circuit for DACA

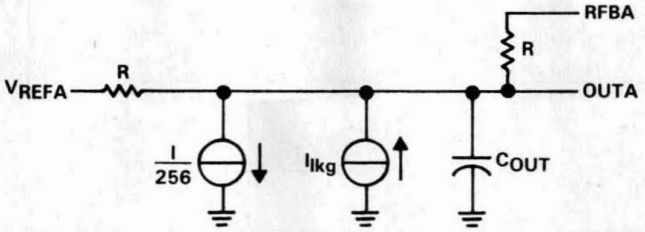


Figure 2. TLC7528 Equivalent Circuit, DACA Latch Loaded With 11111111.

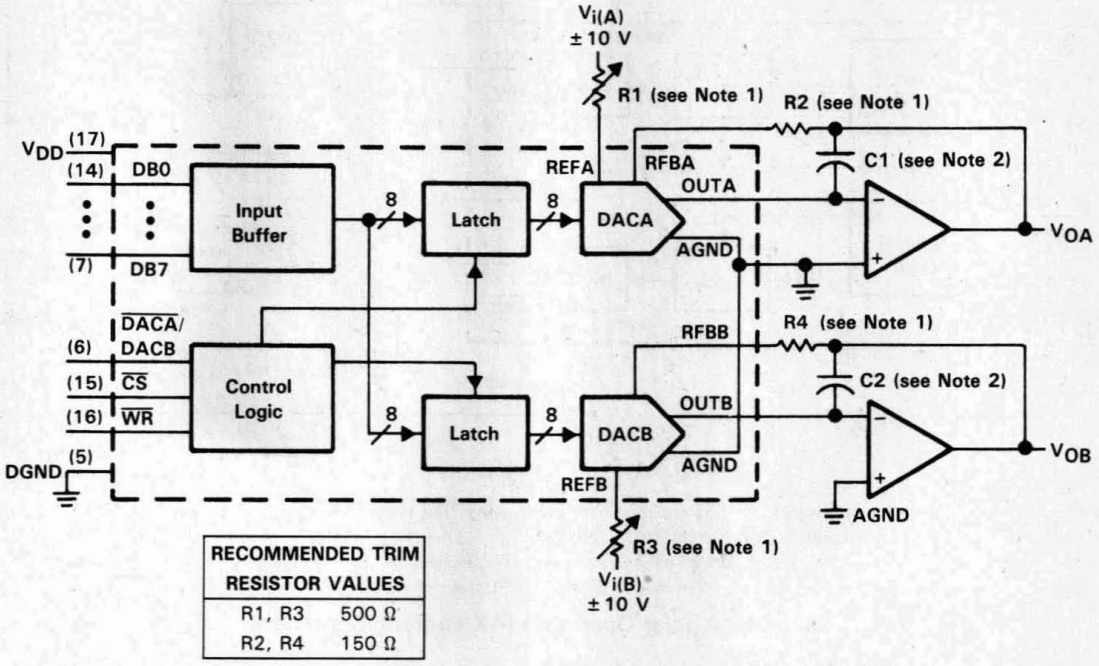
MODE SELECTION TABLE

$\overline{\text{DACA}}$/DACB	$\overline{\text{CS}}$	$\overline{\text{WR}}$	DACA	DACB
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = low level, H = high level, X = don't care

APPLICATION INFORMATION

The TLC7528 is capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant and 4-quadrant multiplication are shown in Figures 3 and 4. Input coding for unipolar and bipolar operation are summarized in Tables 1 and 2, respectively.

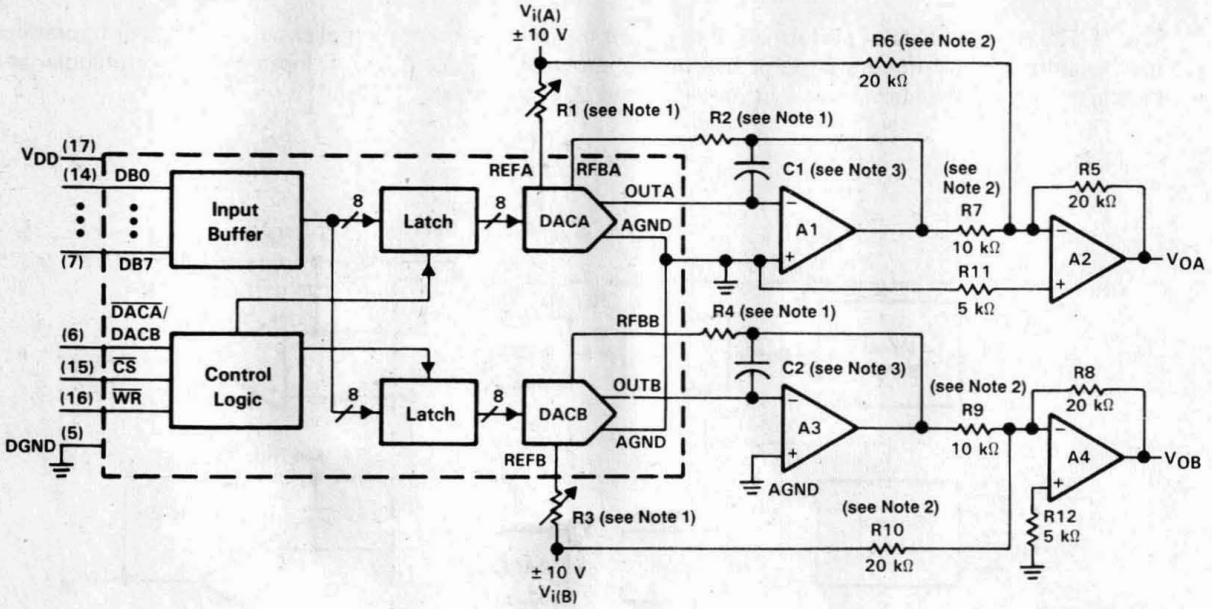


RECOMMENDED TRIM RESISTOR VALUES	
R1, R3	500 Ω
R2, R4	150 Ω

NOTES: 1. R1, R2, R3, and R4 are used only if gain adjustment is required. See table for recommended values. Make gain adjustment with digital input of 255.
2. C1 and C2 phase compensation capacitors (10 pF to 15 pF) are required when using high-speed amplifiers to prevent ringing or oscillation.

Figure 3. Unipolar Operation (2-Quadrant Multiplication)

APPLICATION INFORMATION



NOTES: 1. R1, R2, R3, and R4 are used only if gain adjustment is required. See table in Figure 3 for recommended values. Adjust R1 for V_{OA} = 0 V with code 10000000 in DACA latch. Adjust R3 for V_{OB} = 0 V with 10000000 in DACB latch.
2. Matching and tracking are essential for resistor pairs R6, R7, R9, and R10.
3. C1 and C2 phase compensation capacitors (10 pF to 15 pF) may be required if A1 and A3 are high-speed amplifiers.

Figure 4. Bipolar Operation (4-Quadrant Operation)

Table 1. Unipolar Binary Code

DAC LATCH CONTENTS MSB LSB†	ANALOG OUTPUT
11111111	$-V_i$ (255/256)
10000001	$-V_i$ (129/256)
10000000	$-V_i$ (128/256) = $-V_i/2$
01111111	$-V_i$ (127/256)
00000001	$-V_i$ (1/256)
00000000	$-V_i$ (0/256) = 0

† 1 LSB = $(2^{-8})V_i$

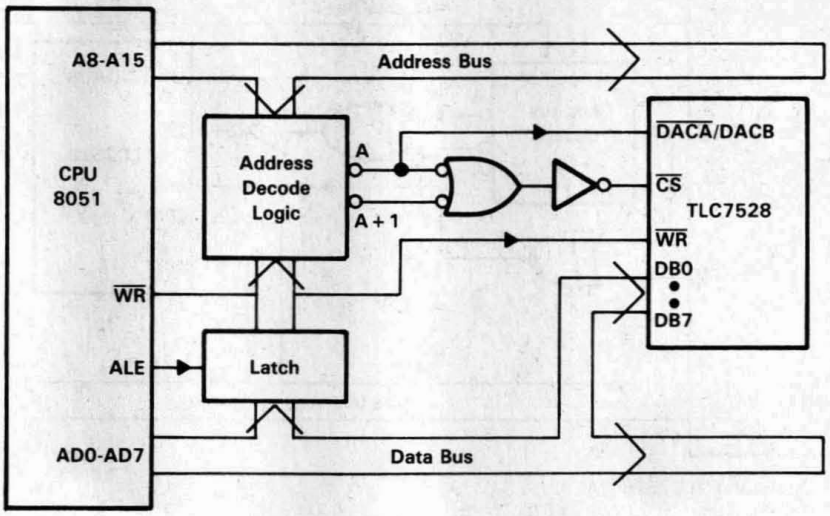
Table 2. Bipolar (Offset Binary) Code

DAC LATCH CONTENTS MSB LSB‡	ANALOG OUTPUT
11111111	V_i (127/128)
10000001	V_i (1/128)
10000000	0 V
01111111	$-V_i$ (1/128)
00000001	$-V_i$ (127/128)
00000000	$-V_i$ (128/128)

‡ 1 LSB = $(2^{-7})V_i$

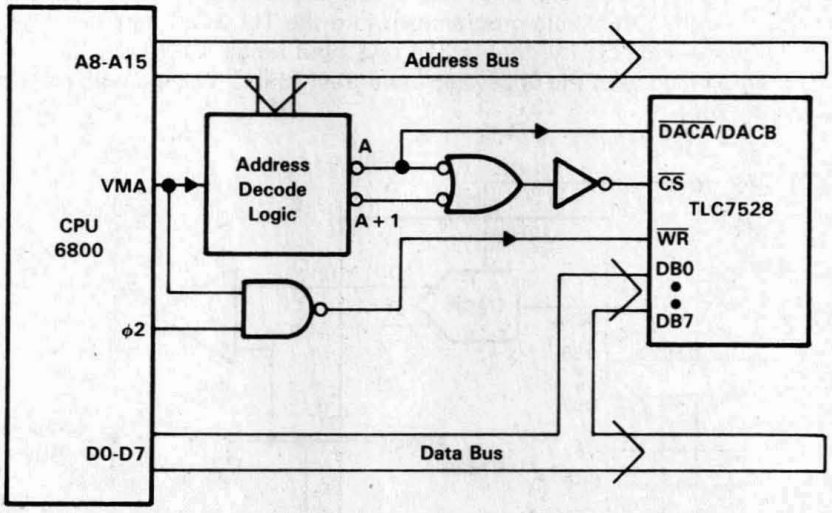
APPLICATION INFORMATION

microprocessor interface information



NOTE: A = decoded address for TLC7528 DACA.
A + 1 = decoded address for TLC7528 DACB.

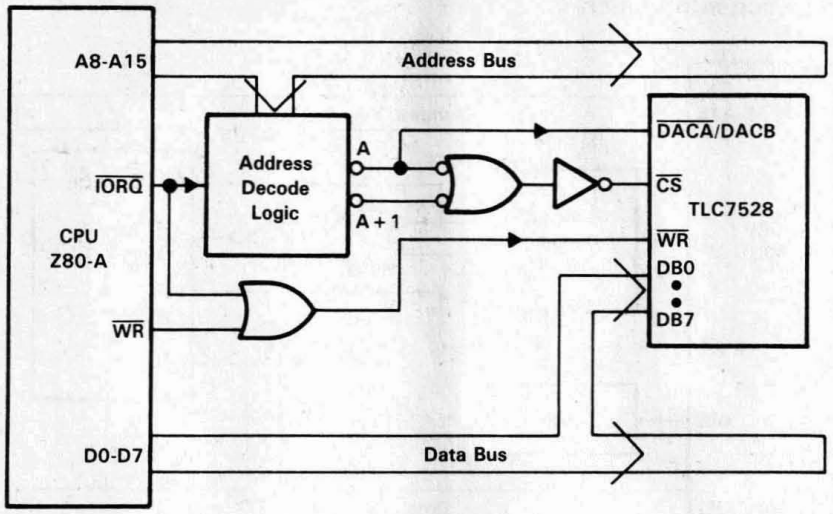
Figure 5. TLC7528 – INTEL 8051 Interface



NOTE: A = decoded address for TLC7528 DACA.
A + 1 = decoded address for TLC7528 DACB.

Figure 6. TLC7528 – 6800 Interface

APPLICATION INFORMATION



NOTE: A = decoded address for TLC7528 DACA.
A + 1 = decoded address for TLC7528 DACB.

Figure 7. TLC7528 TO Z-80A Interface

programmable window detector

The programmable window comparator shown in Figure 8 will determine if voltage applied to the DAC feedback resistors are within the limits programmed into the TLC7528 data latches. Input signal range depends on the reference and polarity, that is, the test input range is 0 to $-V_{ref}$. The DACA and DACB data latches are programmed with the upper and lower test limits. A signal within the programmed limits will drive the output high.

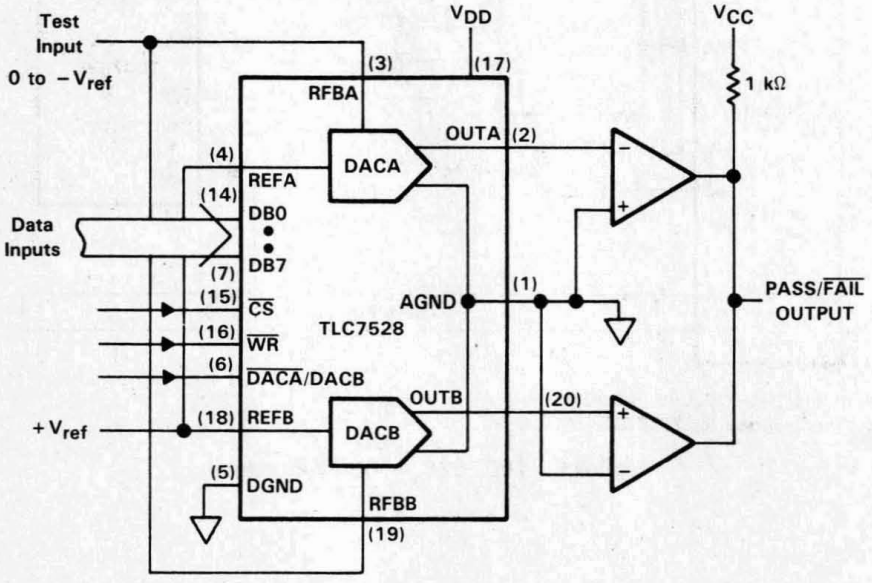


Figure 8. Digitally Programmable Window Comparator (Upper- and Lower-Limit Tester)

APPLICATION INFORMATION

digitally controlled signal attenuator

Figure 9 shows the TLC7528 configured as a two-channel programmable attenuator. Applications include stereo audio and telephone signal level control. Table 3 shows input codes vs attenuation for a 0 to 15.5 dB range.

Attenuation dB = $-20 \log_{10} D/256$, D = digital input code

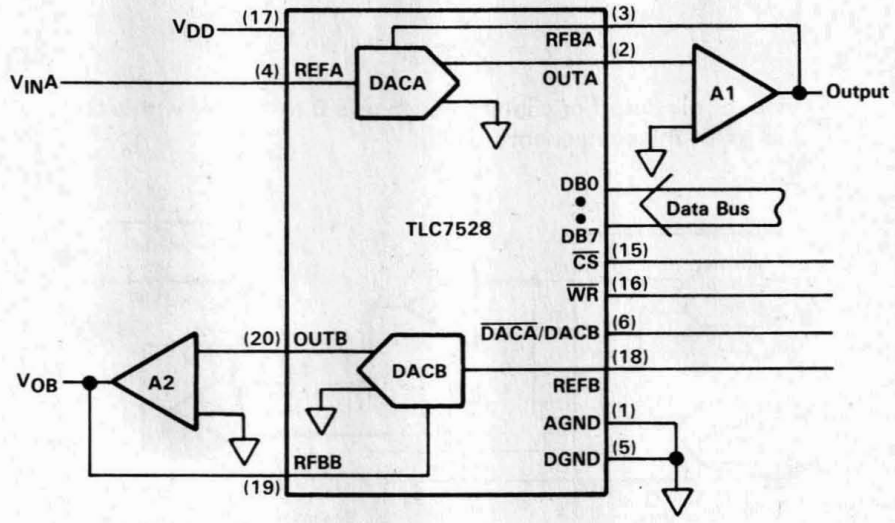


Figure 9. Digitally Controlled Dual Telephone Attenuator

Table 3. Attenuation vs DACA, DACB Code

ATTN(dB)	DAC INPUT CODE	CODE IN DECIMAL	ATTN(dB)	DAC INPUT CODE	CODE IN DECIMAL
0	11111111	255	8.0	01100110	102
0.5	11110010	242	8.5	01100000	96
1.0	11100100	228	9.0	01011011	91
1.5	11010111	215	9.5	01010110	86
2.0	11001011	203	10.0	01010001	81
2.5	11000000	192	10.5	01001100	76
3.0	10110101	181	11.0	01001000	72
3.5	10101011	171	11.5	01000100	68
4.0	10100010	162	12.0	01000000	64
4.5	10011000	152	12.5	00111101	61
5.0	10010000	144	13.0	00111001	57
5.5	10001000	136	13.5	00110110	54
6.0	10000000	128	14.0	00110011	51
6.5	01111001	121	14.5	00110000	48
7.0	01110010	114	15.0	00101110	46
7.5	01101100	108	15.5	00101011	43

APPLICATION INFORMATION

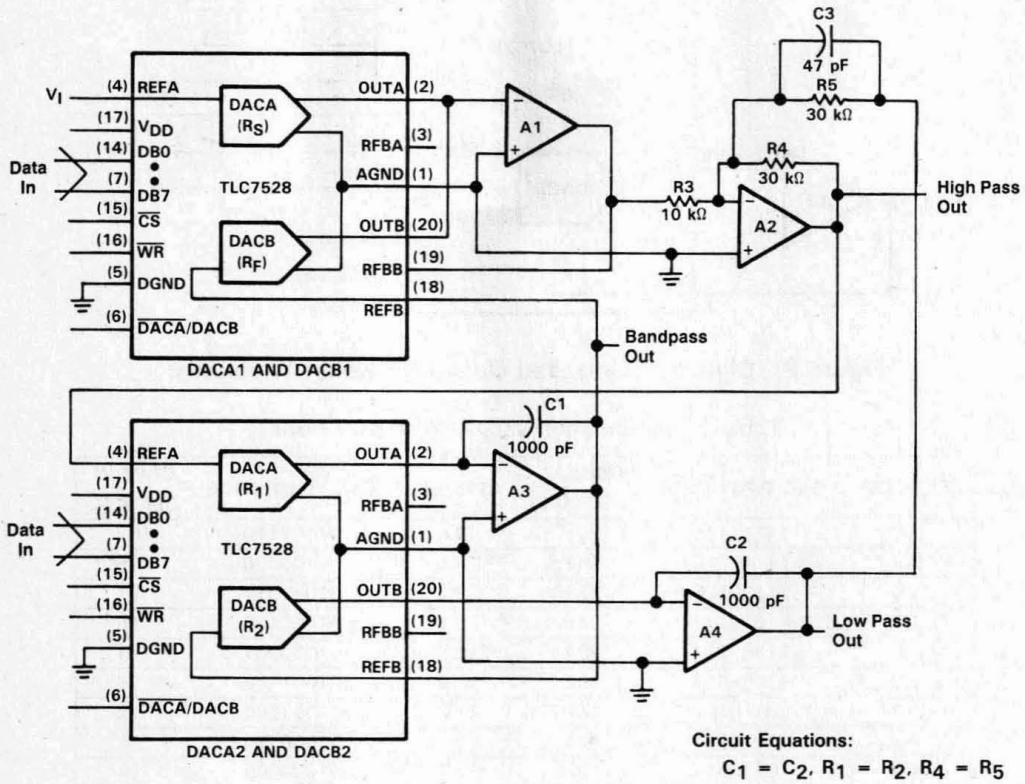
programmable state-variable filter

This programmable state-variable or universal filter configuration provides low-pass, high-pass, and band-pass outputs, and is suitable for applications in which microprocessor control of filter parameters is required.

As shown in Figure 10, DACA1 and DACB1 control the gain and Q of the filter while DACA2 and DACB2 control the cutoff frequency. Both halves of the DACA2 and DACB2 must track accurately in order for the cutoff-frequency equation to be true. With the TLC7528, this is easily achieved.

$$f_C = \frac{1}{2\pi\ R1\ C1}$$

The programmable range for the cutoff or center frequency is 0 to 15 kHz with a Q ranging from 0.3 to 4.5. This defines the limits of the component values.



Circuit Equations:

$$C_1 = C_2,\ R_1 = R_2,\ R_4 = R_5$$

$$Q = \frac{R_3}{R_4} \cdot \frac{R_F}{R_{fb(DACB1)}}$$

$$A_o = -\frac{R_F}{R_S}$$

NOTES: A. Op-amps A1, A2, A3, and A4 are TL287.

B. C3 compensates for the op-amp gain-bandwidth limitations.

C. DAC equivalent resistance equals $\frac{256 \times \text{(DAC ladder resistance)}}{\text{DAC digital code}}$

Figure 10. Digitally Controlled State-Variable Filter

APPLICATION INFORMATION

voltage-mode operation

It is possible to operate the TLC7528 current multiplying D/A converter in a voltage mode. In the voltage mode, a fixed voltage is placed on the current output pin. The analog output voltage is then available at the reference voltage pin. Figure 11 is an example of a current multiplying D/A, which is operated in voltage mode.

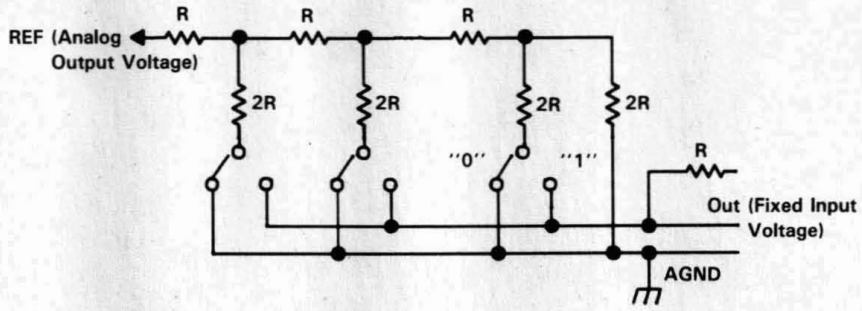


Figure 11. Voltage-Mode Operation

The relationship between the fixed input voltage and the analog output voltage is given by the following equation:

$$V_O = V_I (D/256)$$

where

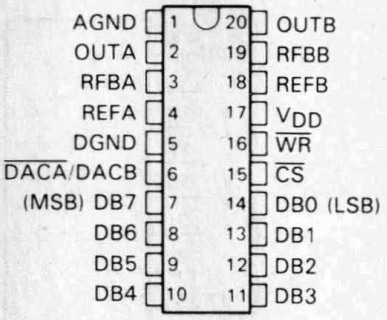
V_O = analog output voltage
V_I = fixed input voltage
D = digital input code converted to decimal

In voltage-mode operation, the TLC7528 will meet the following specification:

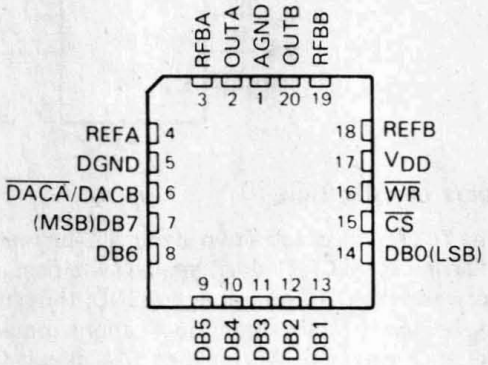
PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Linearity error at REFA or REFB	V_{DD} = 5 V, OUTA or OUTB at 2.5 V, T_A = 0°C to 70°C		1	LSB

- **Advanced LinCMOS™ Silicon-Gate Technology**
- **Easy Microprocessor Interface**
- **On-Chip Data Latches**
- **Digital Inputs are TTL-Compatible with 10.8-V to 15.75-V Power Supply**
- **Monotonic Over the Entire A/D Conversion Range**
- **Fast Control Signaling for Digital Signal Processor Applications Including Interface with TMS320**

DW OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 bits
Linearity Error	1/2 LSB
Power Dissipation	20 mW
Settling Time	100 ns
Propagation Delay	80 ns

description

The TLC7628 is a dual 8-bit digital-to-analog converter designed with separate on-chip data latches and featuring excellent DAC-to-DAC matching. Data is transferred to either of the two DAC data latches via a common 8-bit input port. Control input $\overline{\text{DACA}}$/DACB determines which DAC is loaded. The ''load'' cycle of the TLC7628 is similar to the ''write'' cycle of a random-access memory, allowing easy interface to most popular microprocessor buses and output ports. Segmenting the high-order bits minimizes glitches during changes in the most significant bits, where glitch impulse is typically the strongest.

The TLC7628 operates from a 10.8-V to 15.75-V power supply and is TTL-compatible over this range. Excellent 2- or 4-quadrant multiplying makes the TLC7628 a sound choice for many microprocessor-controlled gain-setting and signal-control applications.

The TLC7628C is characterized for operation from 0°C to 70°C. The TLC7628I is characterized for operation from −25°C to 85°C. The TLC7628E is characterized for operation from −40°C to 85°C.

Table 1. Unipolar Binary Code

DAC LATCH CONTENTS MSB LSB†	ANALOG OUTPUT
11111111	$-V_i$ (255/256)
10000001	$-V_i$ (129/256)
10000000	$-V_i$ (128/256) = $-V_i/2$
01111111	$-V_i$ (127/256)
00000001	$-V_i$ (1/256)
00000000	$-V_i$ (0/256) = 0

† 1 LSB = $(2^{-8})V_i$

Table 2. Bipolar (Offset Binary) Code

DAC LATCH CONTENTS MSB LSB‡	ANALOG OUTPUT
11111111	V_i (127/128)
10000001	V_i (1/128)
10000000	0 V
01111111	$-V_i$ (1/128)
00000001	$-V_i$ (127/128)
00000000	$-V_i$ (128/128)

‡ 1 LSB = $(2^{-7})V_i$

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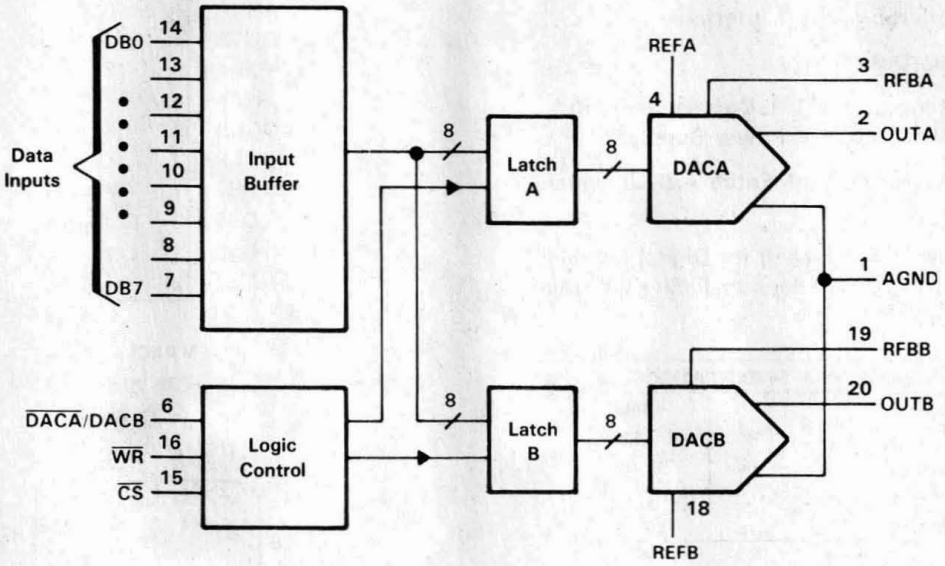
functional block diagram



principles of operation

The TLC7628 contains two identical 8-bit multiplying D/A converters, DACA and DACB. Each DAC consists of an inverted R-2R ladder, analog switches, and input data latches. Binary-weighted currents are switched between the DAC output and AGND, thus maintaining a constant current in each ladder leg independent of the switch state. Most applications require only the addition of an external operational amplifier and voltage reference. A simplified D/A circuit for DACA with all digital inputs low is shown in Figure 1.

Figure 2 shows the DACA equivalent circuit. A similar equivalent circuit can be drawn for DACB. Both DACs share the analog ground pin 1 (AGND). With all digital inputs high, the reference current flows to OUTA. A small leakage current (I_{lkg}) flows across internal junctions, and as with most semiconductor devices, doubles every 10°C. C_o is due to the parallel combination of the NMOS switches and has a value that depends on the number of switches connected to the output. The range of C_o is 25 pF to 60 pF maximum. The equivalent output resistance r_o varies with the input code from 0.8R to 3R where R is the nominal value of the ladder resistor in the R-2R network.

Interfacing the TLC7628 to a microprocessor is accomplished via the data bus, $\overline{CS}$, $\overline{WR}$, and $\overline{DACA}$/DACB control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, the TLC7628 analog output, specified by the $\overline{DACA}$/DACB control line, responds to the activity on the DB0-DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the $\overline{CS}$ signal or $\overline{WR}$ signal goes high, the data on the DB0-DB7 inputs is latched until the $\overline{CS}$ and $\overline{WR}$ signals go low again. When $\overline{CS}$ is high, the data inputs are disabled, regardless of the state of the $\overline{WR}$ signal.

The digital inputs of the TLC7628 provide TTL compatibility when operated from a supply voltage of 10.8 V to 15.75 V.

principles of operation (continued)

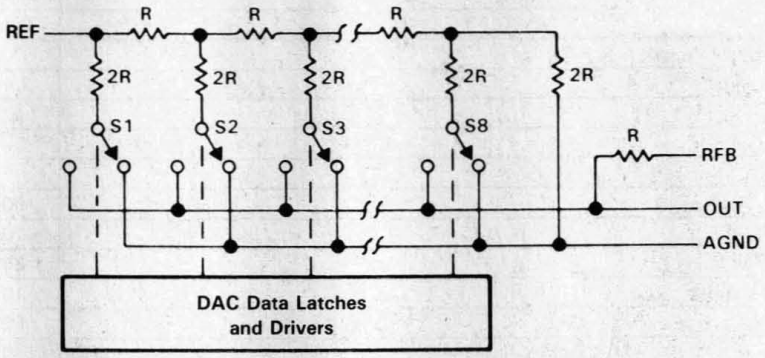
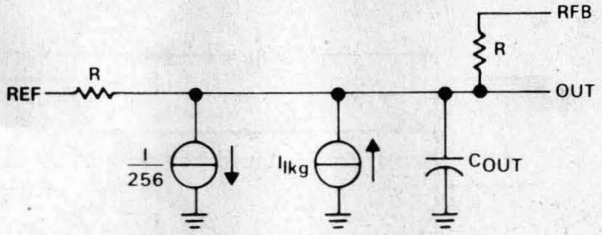


Figure 1. Simplified Functional CIrcuit for DACA or DACB



Latch A or Latch B
Loaded with 11111111.

Figure 2. TLC7628 Equivalent Circuit for DACA OR DACB

MODE SELECTION TABLE

$\overline{DACA}$/ DACB	$\overline{CS}$	$\overline{WR}$	DACA	DACB
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

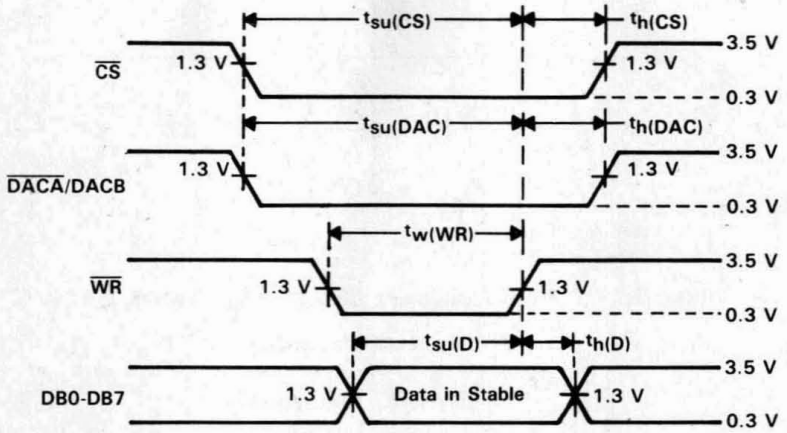
L = low level, H = high level, X = don't care

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (to AGND or DGND) . . . . . −0.3 V to 17 V
Voltage between AGND and DGND . . . . . V_{DD}
Input voltage, V_I (to DGND) . . . . . −0.3 V to V_{DD} +0.3 V
Reference voltage, V_{refA} or V_{refB} (to AGND) . . . . . ±25 V
Feedback voltage, V_{RFBA} or V_{RFBB} (to AGND) . . . . . ±25 V
Output voltage, V_{OA} or V_{OB} (to AGND) . . . . . ±25 V
Peak input current . . . . . 10 μA
Operating free-air temperature range: TLC7628C . . . . . 0°C to 70°C
TLC7628I . . . . . −25°C to 85°C
TLC7628E . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package . . . . . 260°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		10.8		15.75	V
Reference voltage, V_{refA} or V_{refB}			±10		V
High-level input voltage, V_{IH}		2.4			V
Low-level input voltage, V_{IL}				0.8	V
$\overline{CS}$ setup time, $t_{su(CS)}$		50			ns
$\overline{CS}$ hold time, $t_{h(CS)}$		0			ns
DAC select setup time, $t_{su(DAC)}$		60			ns
DAC select hold time, $t_{h(DAC)}$		10			ns
Data bus input setup time $t_{su(D)}$		25			ns
Data bus input hold time $t_{h(D)}$		10			ns
Pulse duration, $\overline{WR}$ low, $t_{w(WR)}$		50			ns
Operating free-air temperature, T_A	TLC7628C	0		70	°C
	TLC7628I	−25		85	
	TLC7628E	−40		85	



For all input signals, $t_r = t_f = 5$ ns (10% to 90% points).

Figure 3. Setup and Hold Times

electrical characteristics over recommended ranges of operating free-air temperature and V_{DD}, $V_{refA} = V_{refB} = 10$ V, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
I_{IH}	High-level input current		$V_I = V_{DD}$	Full Range		10	μA
				25°C		1	
I_{IL}	Low-level input current		$V_I = 0$	Full Range		−10	μA
				25°C		−1	
	Reference input impedance REFA or REFB to AGND				5	20	kΩ
I_{lkg}	Output leakage current	OUTA	DAC data latch loaded with 00000000, $V_{refA} = \pm 10$ V	Full Range		±200	nA
				25°C		±50	
		OUTB	DAC data latch loaded with 00000000, $V_{refB} = \pm 10$ V	Full Range		±200	
				25°C		±50	
	Input resistance match (REFA to REFB)					±1%	
	DC supply sensitivity $\Delta gain/\Delta V_{DD}$		$\Delta V_{DD} = \pm 5\%$	Full Range		0.02	%/%
				25°C		0.01	
I_{DD}	Supply current	Quiescent	All digital inputs at V_{IH}min or V_{IL}max			2	mA
		Standby	All digital inputs at 0 V or V_{DD}	Full Range		0.5	
				25°C		0.1	
C_i	Input capacitance	DB0-DB7				10	pF
		$\overline{WR}$, $\overline{CS}$, $\overline{DACA}$/DACB				15	
C_o	Output capacitance (OUTA, OUTB)		DAC Data latches loaded with 00000000			25	pF
			DAC Data latches loaded with 11111111			60	

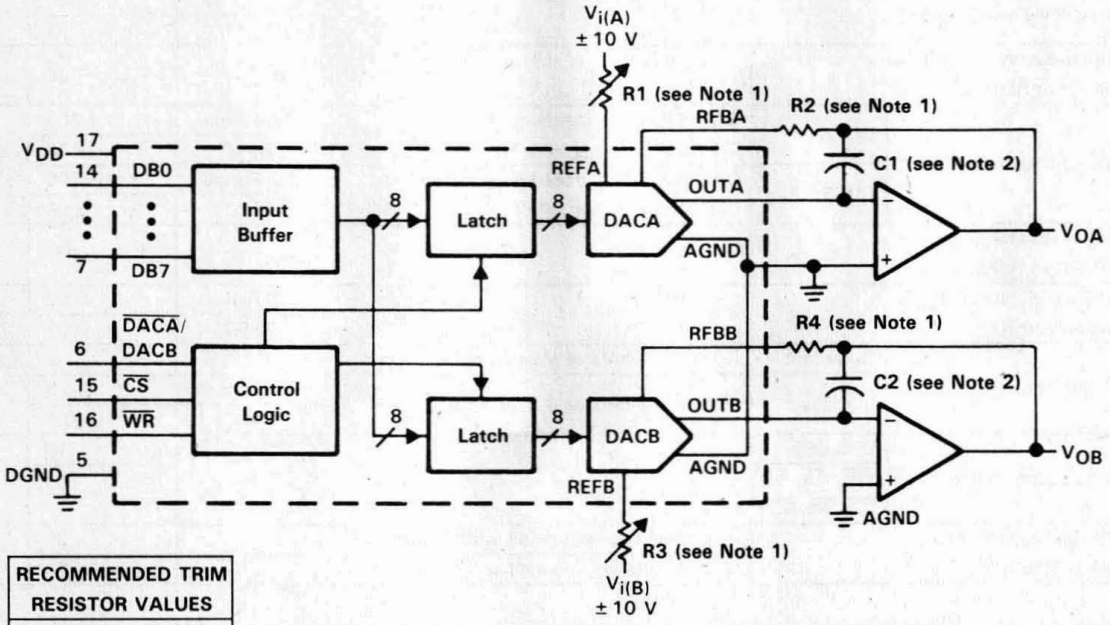
operating characteristics over recommended ranges of operating free-air temperature and V_{DD}, $V_{refA} = V_{refB} = 10$ V, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Linearity error						±1/2	LSB
Settling time (to 1/2 LSB)		See Note 1				100	ns
Gain error		See Note 2	Full Range			±3	LSB
			25°C			±2	
AC feedthrough	REFA to OUTA	See Note 3	Full Range			−65	dB
	REFB to OUTB		25°C			−70	
Temperature coefficient of gain						±0.0035	%FSR/°C
Propagation delay (from digital input to 90% of final analog output current)		See Note 4				80	ns
Channel-to-channel isolation	REFA to OUTB	See Note 5	25°C		80		dB
	REFB to OUTA	See Note 6	25°C		80		
Digital-to-analog glitch impulse area		Measured for code transition from 00000000 to 11111111, $T_A = 25$°C			330		nV•s
Digital crosstalk		Measured for code transition from 00000000 to 11111111, $T_A = 25$°C			60		nV•s
Harmonic distortion		$V_i = 6$ V, f = 1 kHz, $T_A = 25$°C			−85		dB

NOTES: 1. OUTA, OUTB load = 100 Ω, C_{ext} = 13 pF; $\overline{WR}$ and $\overline{CS}$ at 0 V; DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
2. Gain error is measured using an internal feedback resistor. Nominal Full Scale Range (FSR) = V_{ref} − 1 LSB. Both DAC latches are loaded with 11111111.
3. V_{ref} = 20 V peak-to-peak, 10-kHz sine wave.
4. $V_{refA} = V_{refB} = 10$ V; OUTA/OUTB load = 100 Ω, C_{ext} = 13 pF; $\overline{WR}$ and $\overline{CS}$ at 0 V; DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
5. V_{refA} = 20 V peak-to-peak, 10-kHz sine wave; V_{refB} = 0.
6. V_{refB} = 20 V peak-to-peak, 10-kHz sine wave; V_{refA} = 0.

APPLICATION INFORMATION

The TLC7628 is capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant and 4-quadrant multiplication are shown in Figures 4 and 5. Input coding for unipolar and bipolar operation are summarized in Tables 1 and 2, respectively.

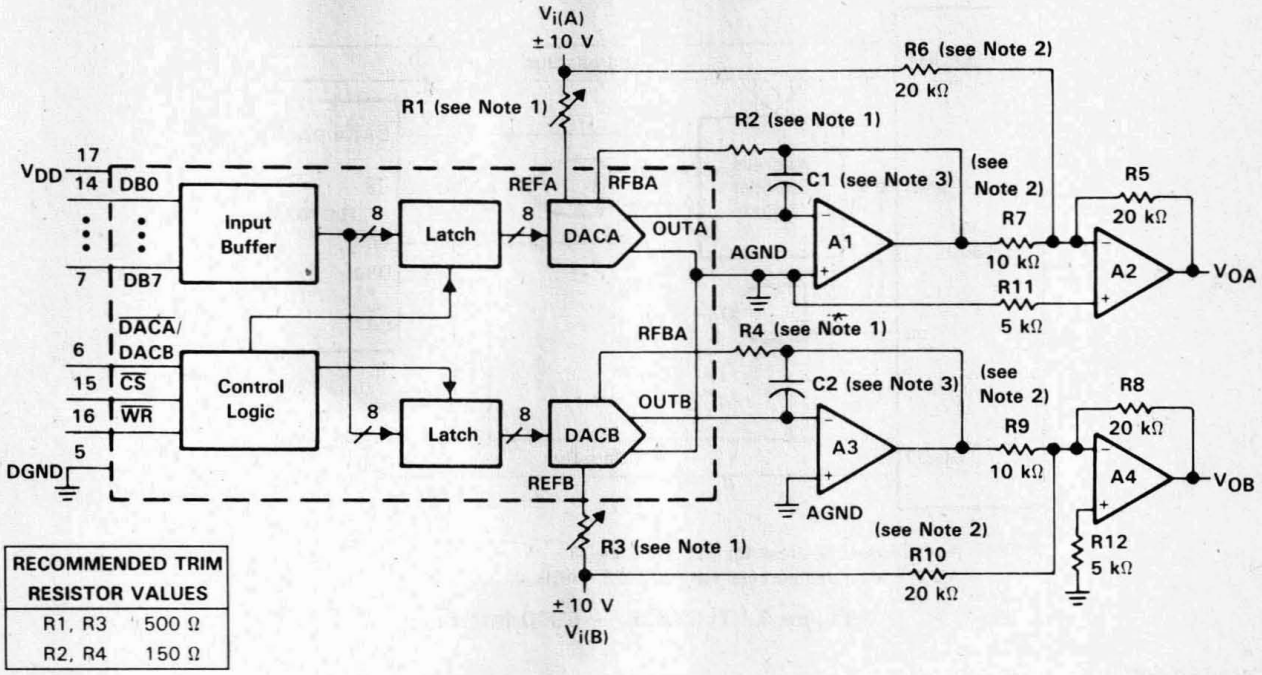


RECOMMENDED TRIM RESISTOR VALUES	
R1, R3	500 Ω
R2, R4	150 Ω

NOTES: 1. R1, R2, R3, and R4 are used only if gain adjustment is required. See table for recommended values. Make gain adjustment with digital input of 255.
2. C1 and C2 phase compensation capacitors (10 pF to 15 pF) are required when using high-speed amplifiers to prevent ringing or oscillation.

Figure 4. Unipolar Operation (2-Quadrant Multiplication)

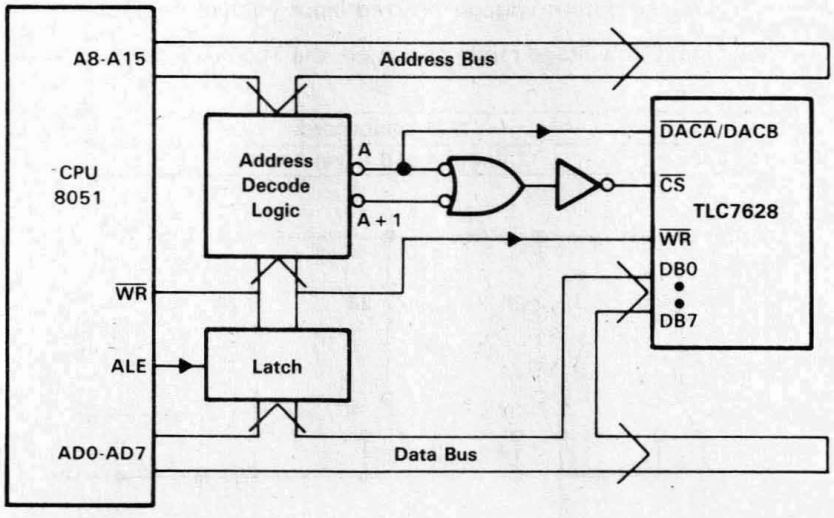
APPLICATION INFORMATION



RECOMMENDED TRIM RESISTOR VALUES	
R1, R3	500 Ω
R2, R4	150 Ω

NOTES: 1. R1, R2, R3, and R4 are used only if gain adjustment is required. See table for recommended values. Adjust R1 for V_{OA} = 0 V with code 10000000 in DACA latch. Adjust R3 for V_{OB} = 0 V with 10000000 in DACB latch.
2. Matching and tracking are essential for resistor pairs R6, R7, R9, and R10.
3. C1 and C2 phase compensation capacitors (10 pF to 15 pF) may be required if A1 and A3 are high-speed amplifiers.

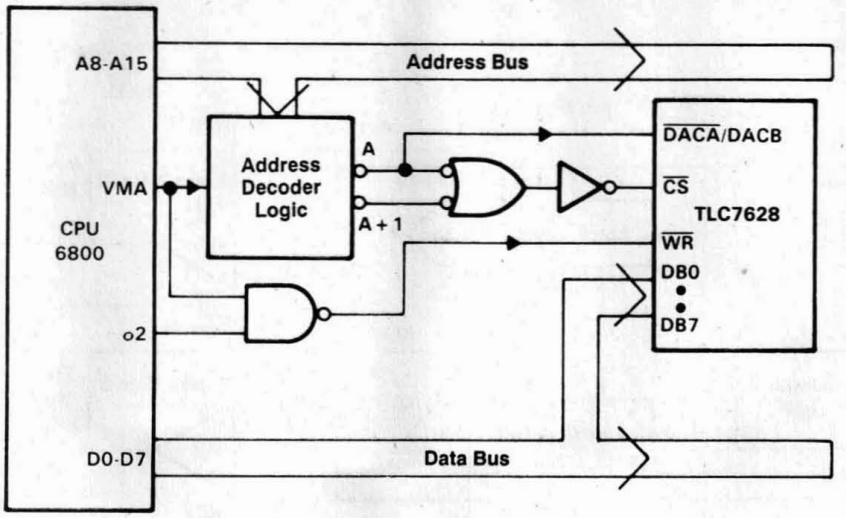
Figure 5. Bipolar Operation (4-Quadrant Operation)



NOTE: A = decoded address for TLC7628 DACA.
A + 1 = decoded address for TLC7628 DACB.

Figure 6. TLC7628 — INTEL 8051 Interface

APPLICATION INFORMATION



NOTE: A = decoded address for TLC7628 DACA.
A+1 = decoded address for TLC7628 DACB.

Figure 7. TLC7628 — 6800 Interface

voltage-mode operation

The TLC7628 current-multiplying D/A converter can be operated in a voltage mode. In the voltage mode, a fixed voltage is placed on the current output pin. The analog output voltage is then available at the reference voltage pin. An example of a current-multiplying D/A converter operating in voltage mode is shown in Figure 8. The relationship between the fixed input voltage and the analog output voltage is given by the following equation:

$$\text{Analog output voltage} = \text{fixed input voltage } (D/256)$$

where D = the digital input. In voltage-mode operation, the TLC7628 meets the following specification:

LINEARITY ERROR	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog output voltage for REFA, B	V_{DD} = 12 V, OUTA or OUTB at 5 V, T_A = 25°C			1	LSB

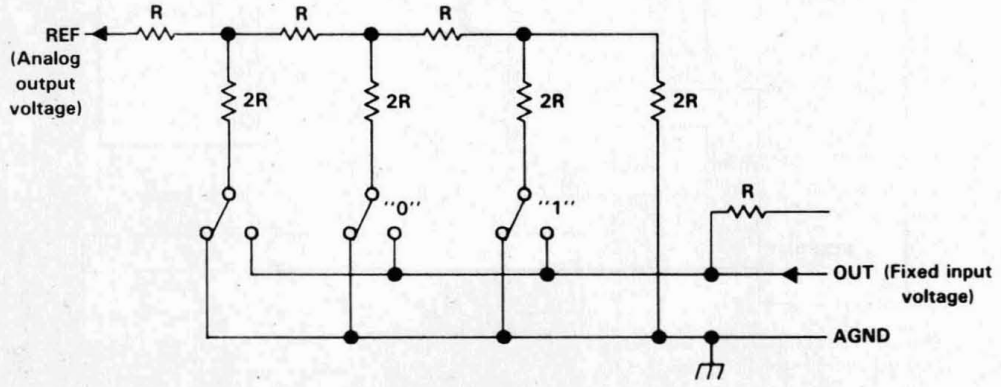


Figure 8. Current-Multiplying D/A Converter Operating in Voltage Mode

General Information 1
General Purpose ADCs 2
General Purpose DACs 3
Video and High-Speed ADCs and DACs 4
DSP Analog Interface and Conversion 5
Video Interface Palettes 6
Analog Switches 7
Filters 8
Data Manuals 9
Application Reports 10
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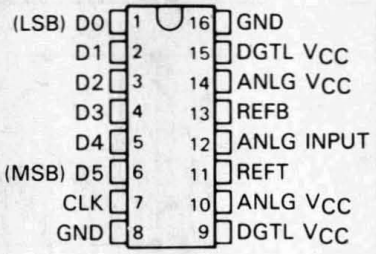
4 Video and High-Speed ADCs and DACs

D3163, OCTOBER 1988 – REVISED APRIL 1990

- 6-Bit Resolution
- Linearity Error . . . ±0.8%
- Maximum Conversion Rate . . . 30 MHz Typ
- Analog Input Voltage Range . . . V_{CC} to V_{CC} – 2 V
- Analog Input Dynamic Range . . . 1 V
- TTL Digital I/O Level
- Low Power Consumption . . . 200 mW Typ
- 5-V Single-Supply Operation
- Interchangeable with Fujitsu MB40576

N PACKAGE
(TOP VIEW)

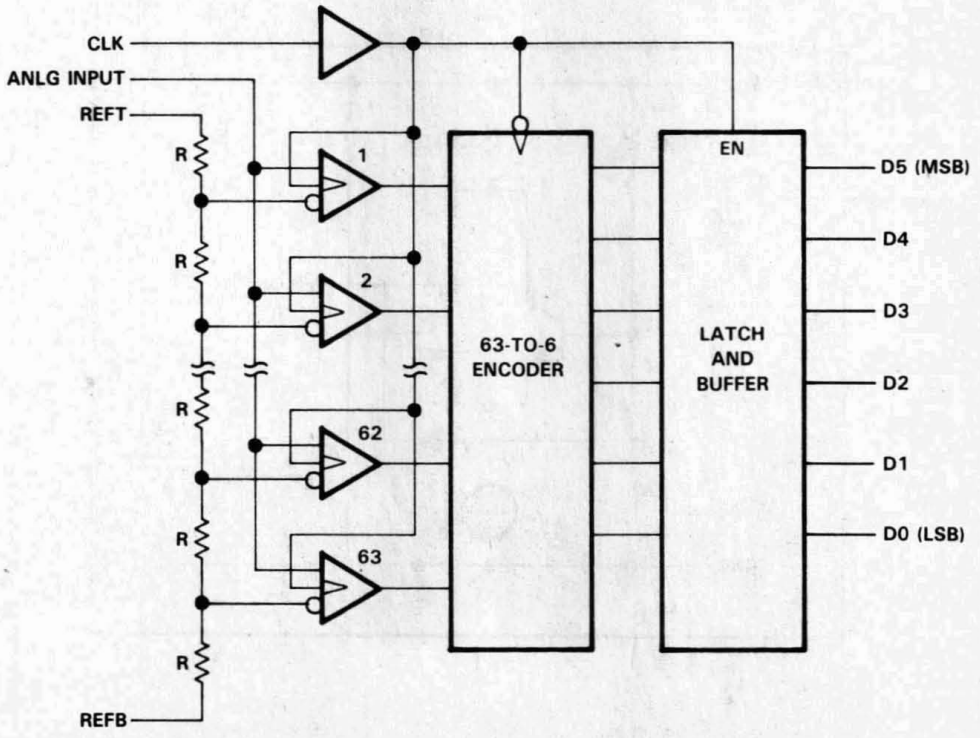


description

The TL5501 is a low-power ultra-high-speed video-band analog-to-digital converter that uses the Advanced Low-Power Schottky (ALS) process. It utilizes the full-parallel comparison (flash method) for high-speed conversion. It converts wide-band analog signals (such as a video signal) to a digital signal at a sampling rate of dc to 30 MHz. Because of this high-speed capability, the TL5501 is suitable for digital video applications such as digital TV, video processing with a computer, or radar signal processing.

The TL5501 is characterized for operation from 0°C to 70°C.

functional block diagram



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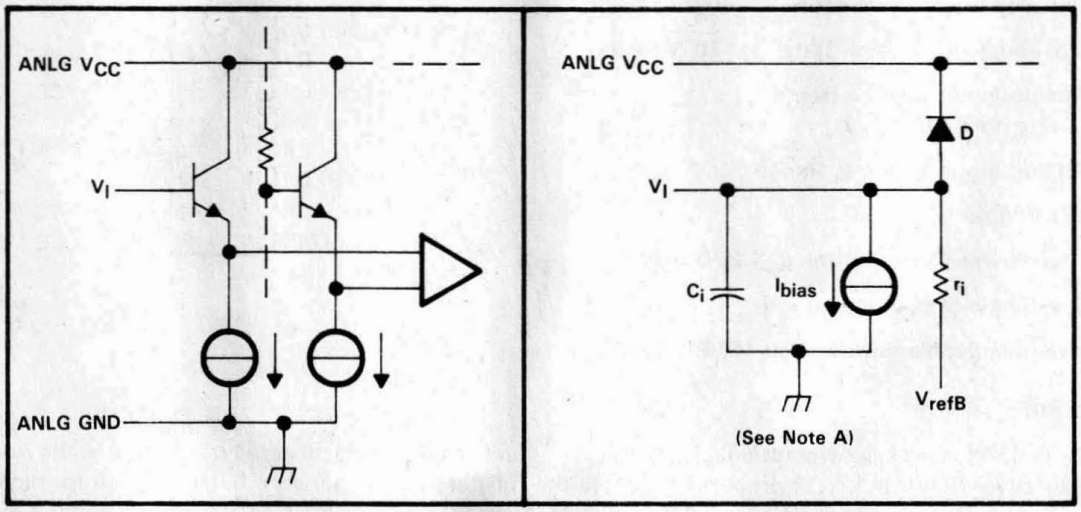
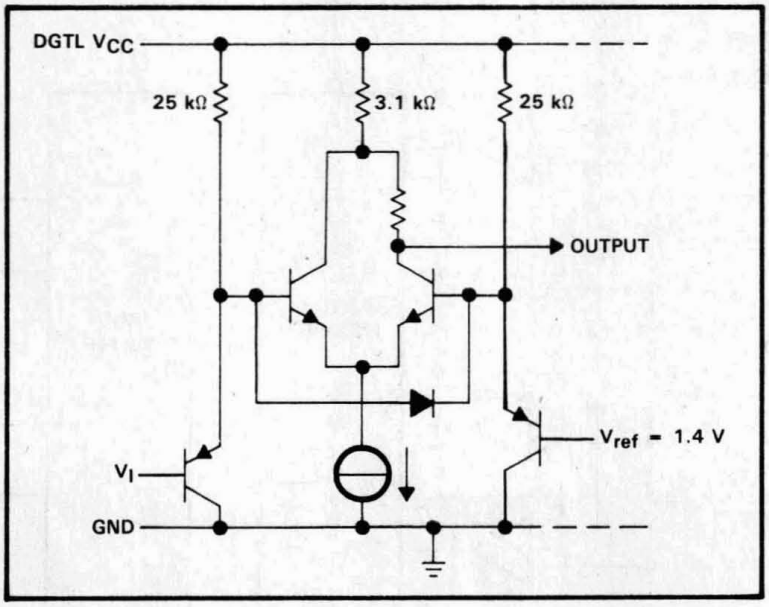
equivalents of analog input circuit



NOTE A: C_i — nonlinear emitter-follower junction capacitance
r_i — linear resistance model for input current transition caused by comparator switching. $V_I < V_{refB}$: Infinite; CLK high: Infinite.
V_{refB} — voltage at REFB terminal
I_{bias} — constant input bias current
D — base-collector junction diode of emitter-follower transistor

equivalent of digital input circuit



FUNCTION TABLE

STEP	ANALOG INPUT VOLTAGE†	DIGITAL OUTPUT CODE
0	3.992 V	L L L L L L
1	4.008 V	L L L L L H
⋮	⋮	⋮
31	4.488 V	L H H H H H
32	4.508 V	H L L L L L
33	4.520 V	H L L L L H
⋮	⋮	⋮
62	4.984 V	H H H H H L
63	5.000 V	H H H H H H

† These values are based on the assumption that V_{refB} and V_{refT} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 4.000 V and the transition to full scale (V_{FT}) is 4.992 V. 1 LSB = 16 mV.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, ANLG V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Supply voltage range, DGTL V_{CC} . . . . . −0.5 V to 7 V
Input voltage range at digital input, V_I . . . . . −0.5 V to 7 V
Input voltage range at analog input, V_I . . . . . −0.5 V to ANLG V_{CC} +0.5 V
Analog reference voltage range, V_{ref} . . . . . −0.5 V to ANLG V_{CC} +0.5 V
Storage temperature range . . . . . −55°C to 150°C
Operating free-air temperature range . . . . . 0°C to 70°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to the network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, ANLG V_{CC}	4.75	5	5.25	V
Supply voltage, DGTL V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Input voltage at analog input, V_I (see Note 2)	4		5	V
Analog reference voltage (top side), V_{refT} (see Note 2)	4	5	5.1	V
Analog reference voltage (bottom side), V_{refB} (see Note 2)	3	4	4.1	V
High-level output current, I_{OH}	−400			μA
Low-level output current, I_{OL}			4	mA
Clock pulse duration, high-level or low-level, t_w	25			ns
Operating free-air temperature, T_A	0		70	°C

NOTE 2: $V_{refB} < V_I < V_{refT}$, $V_{refT} - V_{refB} = 1\ V \pm 0.1\ V$.

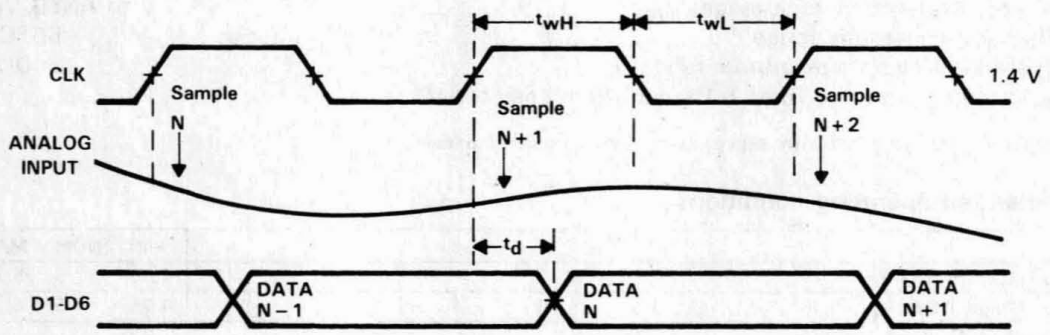
electrical characteristics over operating supply voltage range, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_I	Analog input current	V_I = 5 V			75	μA
		V_I = 4 V			73	
I_{IH}	Digital high-level input current	V_I = 2.7 V		0	20	μA
I_{IL}	Digital low-level input current	V_I = 0.4 V	−400	−40		μA
I_I	Digital input current	V_I = 7 V			100	μA
I_{refB}	Reference current	V_{refB} = 4 V		−4	−7.2	mA
I_{refT}	Reference current	V_{refT} = 5 V		4	7.2	mA
V_{OH}	High-level output voltage	I_{OH} = −400 μA	2.7			V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
r_i	Analog input resistance		100			kΩ
$1C_i$	Analog input capacitance			35	65	pF
I_{CC}	Supply current			40	60	mA

operating characteristics over operating supply voltage range, T_A = 25°C (unless otherwise noted)

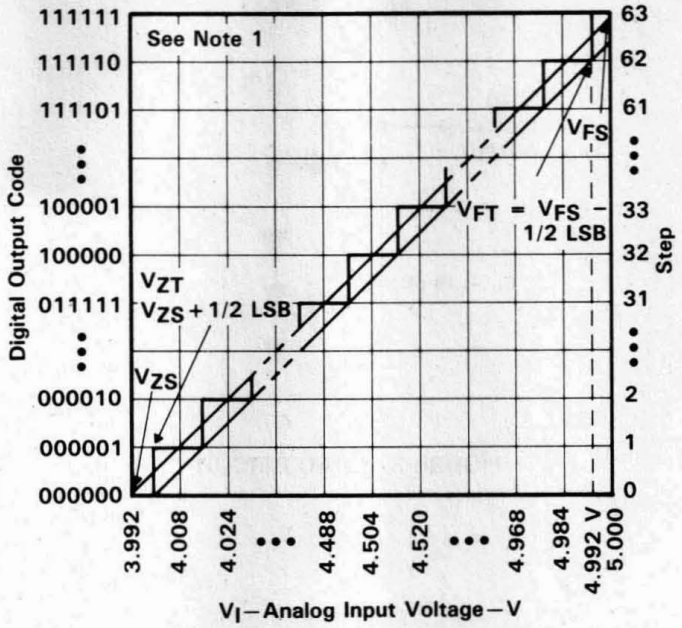
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
E_L	Linearity error				±0.8	%FSR
f_{max}	Maximum conversion rate		20	30		MHz
t_d	Digital output delay time	See Figure 3		15	30	ns

timing diagram



TYPICAL CHARACTERISTICS

IDEAL CONVERSION CHARACTERISTICS



NOTE 1: This curve is based on the assumption that V_{refB} and V_{refT} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 4.000 V and the transition to full scale (V_{FT}) is 4.992 V. 1 LSB = 16 mV.

FIGURE 1

END-POINT LINEARITY ERROR

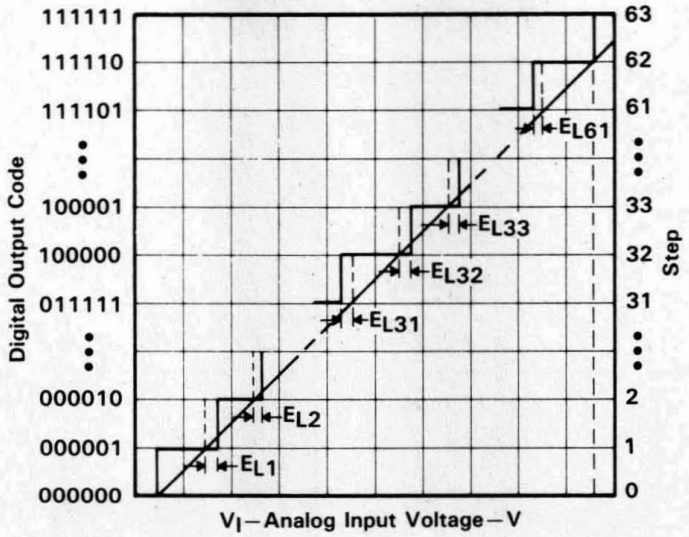


FIGURE 2

PARAMETER MEASUREMENT INFORMATION

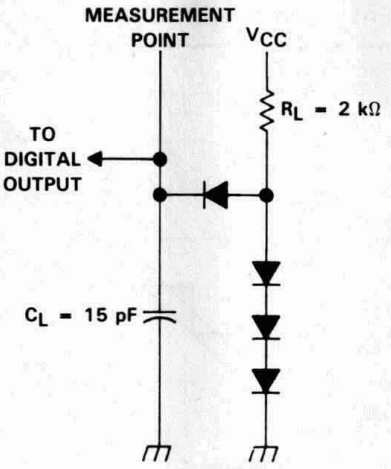
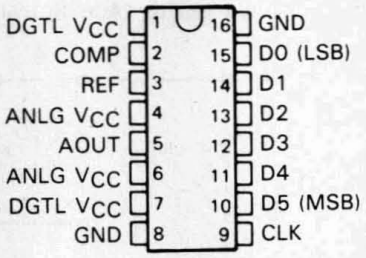


FIGURE 3. LOAD CIRCUIT

D3154, OCTOBER 1988–REVISED MAY 1990

- 6-Bit Resolution
- Linearity Error . . . ±0.8%
- Maximum Conversion Rate . . . 30 MHz Typ
  20 MHz Min
- Analog Output Voltage Range . . . V_{CC} to V_{CC} – 1 V
- TTL Digital Input Voltage
- Low Power Consumption . . . 240 mW Typ
- 5-V Single-Supply Operation
- Interchangeable with Fujitsu MB40776

N PACKAGE
(TOP VIEW)

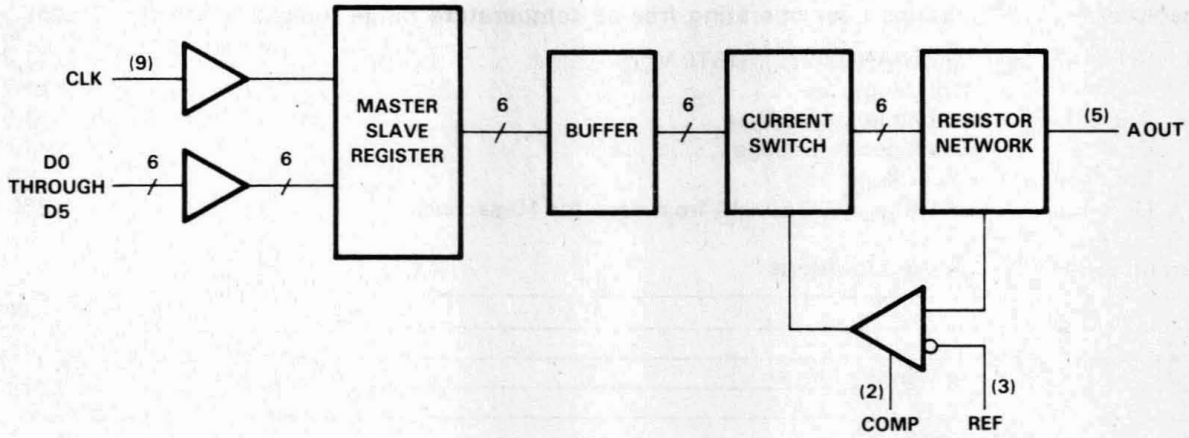


description

The TL5601 is a low-power ultra-high-speed video digital-to-analog converter that uses the Advanced Low-Power Schottky (ALS) process. It converts digital signals to analog signals at a sampling rate of dc to 30 MHz. Because of such high-speed capability, the TL5601 is suitable for digital video applications such as digital television, video processing with a computer, and radar signal processing.

The TL5601 is characterized for operation from 0°C to 70°C.

functional block diagram



FUNCTION TABLE

STEP	DIGITAL INPUTS						OUTPUT VOLTAGE†
	D5	D4	D3	D2	D1	D0	
0	L	L	L	L	L	L	3.992 V
1	L	L	L	L	L	H	4.008 V
⋮							⋮
31	L	H	H	H	H	H	4.488 V
32	H	L	L	L	L	L	4.504 V
33	H	L	L	L	L	H	4.520 V
⋮							⋮
62	H	H	H	H	H	L	4.984 V
63	H	H	H	H	H	H	5.000 V

†For V_{CC} = 5 V, V_{ref} = 3.976 V

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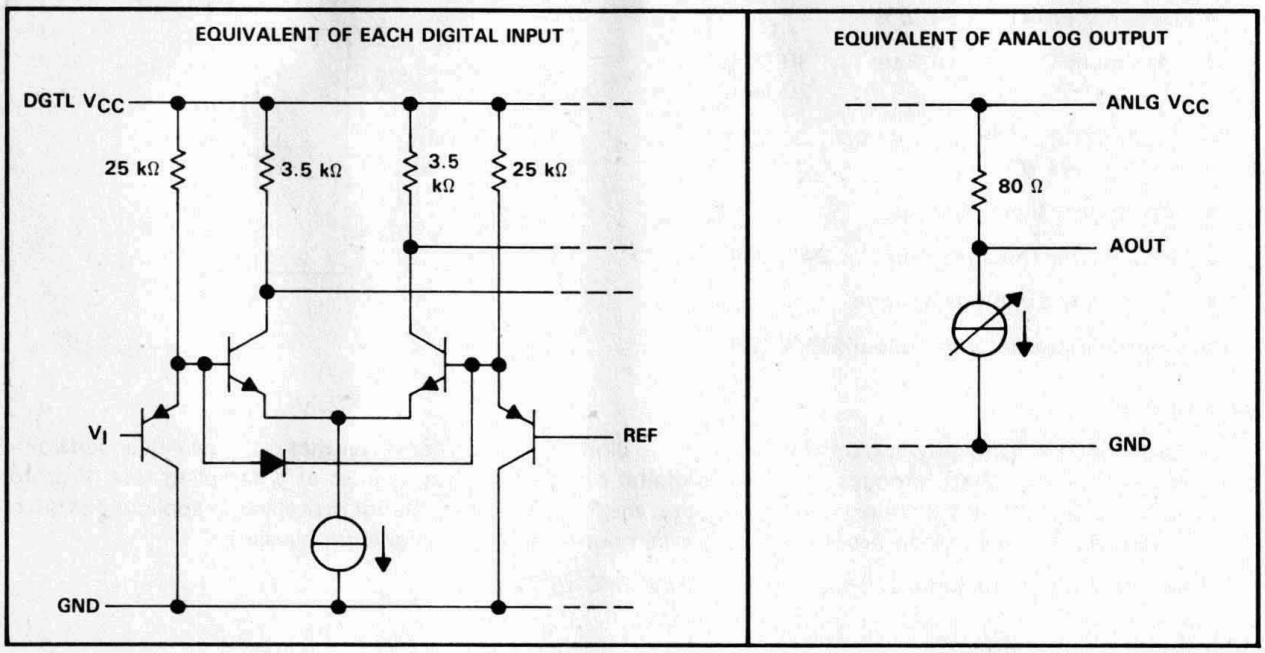
schematics of equivalent input and output circuits



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, ANLG V_{CC}, DGTL V_{CC} . . . . . −0.5 V to 7 V
Digital input voltage range, V_I . . . . . −0.5 V to 7 V
Analog reference voltage range, V_{ref} . . . . . 3.8 V to V_{CC} +0.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{ref}	Analog reference voltage (see Note 1)	3.8	4	4.2	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
t_w	Pulse duration, CLK high or low	25			ns
t_{su}	Setup time, data before CLK↑	12.5			ns
t_h	Hold time, data after CLK↑	12.5			ns
C_{comp}	Phase compensation capacitance (see Note 2)	1			μF
T_A	Operating free-air temperature	0		70	°C

NOTES: 1. V_{ref} must be within 1.2 V of V_{CC}.
2. This capacitor should be connected between COMP and GND.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_I	Input current at maximum input voltage	V_I = 7 V		0	100	μA
I_{IH}	High-level input current	V_I = 2.7 V		0	20	μA
I_{IL}	Low-level input current	V_I = 0.4 V	−400	−40		μA
I_{ref}	Input reference current	V_{ref} = 4 V			10	μA
V_{FS}	Full-scale analog output voltage	V_{CC} = 5 V, V_{ref} = 3.976 V,	V_{CC}−15	V_{CC}	V_{CC}+15	mV
V_{ZS}	Zero-scale analog output voltage	I_O = 0 (no load)	3.932	3.992	4.052	V
z_o	Output impedance	T_A = 25°C	70	80	90	Ω
I_{CC}	Supply current	V_{ref} = 4.05 V		48	65	mA

operating characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
E_L	Linearity error				±0.8	%FSR
f_{max}	Maximum conversion rate		20	30		MHz
	Resolution				6	BIT

†All typical values are at V_{CC} = 5 V, V_{ref} = 4 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

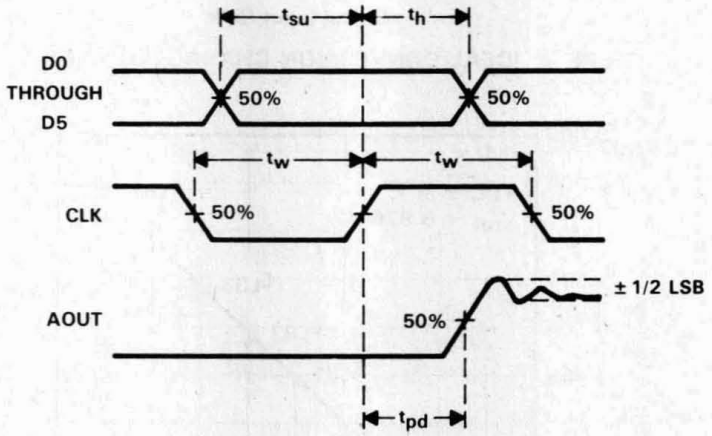


FIGURE 1. VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS

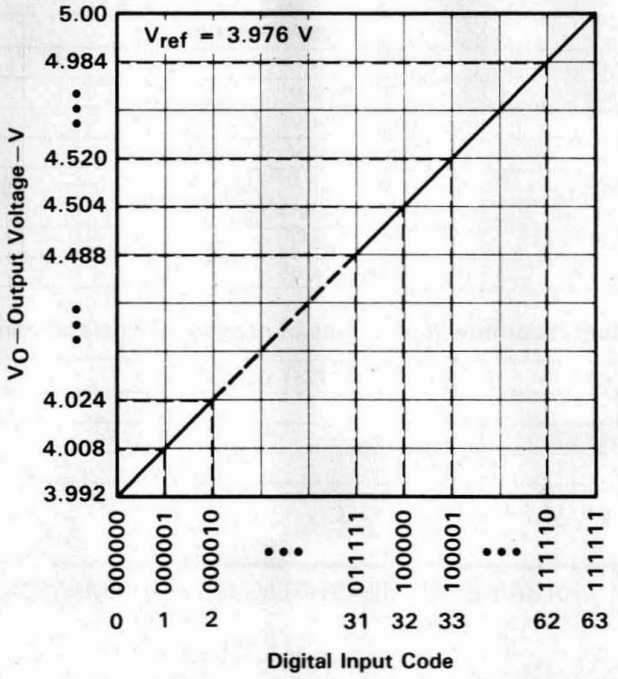


FIGURE 2. IDEAL CONVERSION CHARACTERISTICS

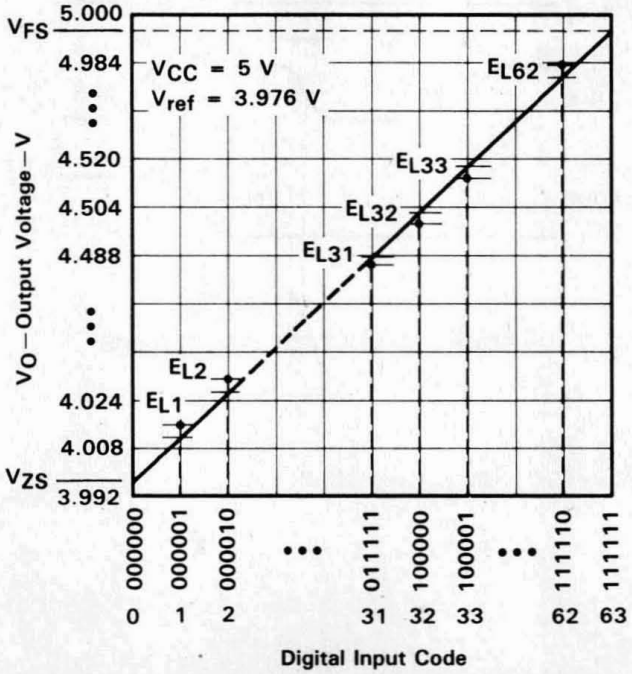
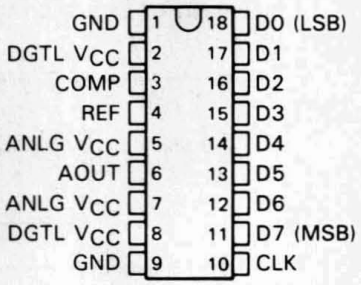


FIGURE 3. END-POINT LINEARITY ERROR

D3094, SEPTEMBER 1988 – REVISED OCTOBER 1990

- 8-Bit Resolution
- ±0.2% Linearity
- Maximum Conversion Rate . . . 30 MHz Typ
  20 MHz Min
- Analog Output Voltage Range . . . V_{CC} to V_{CC} – 1 V
- TTL Digital Input Voltage
- 5-V Single-Supply Operation
- Low Power Consumption . . . 250 mW Typ
- Interchangeable with Fujitsu MB40778

N PACKAGE
(TOP VIEW)

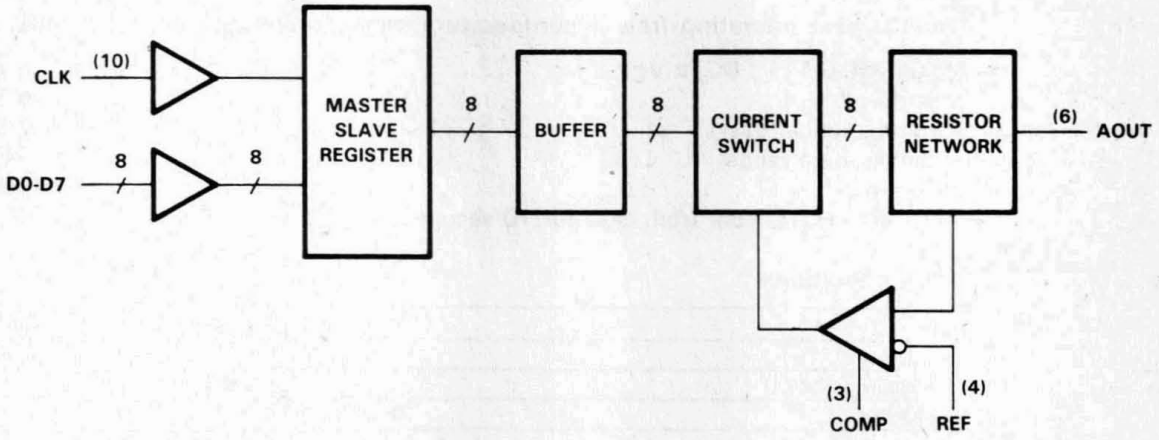


description

The TL5602 is a low-power ultra-high-speed video digital-to-analog converter that uses the Advanced Low-Power Schottky (ALS) process. It converts digital signals to analog signals at a sampling rate of dc to 20 MHz. Because of such high-speed capability, the TL5602 is suitable for digital video applications such as digital television, video processing with a computer, and radar signal processing.

The TL5602C is characterized for operation from 0°C to 70°C.

functional block diagram



FUNCTION TABLE

STEP	DIGITAL INPUTS								OUTPUT VOLTAGE†
	D7	D6	D5	D4	D3	D2	D1	D0	
0	L	L	L	L	L	L	L	L	3.980 V
1	L	L	L	L	L	L	L	L	3.984 V
⋮									⋮
127	L	H	H	H	H	H	H	H	4.488 V
128	H	L	L	L	L	L	L	L	4.492 V
129	H	L	L	L	L	L	L	H	4.496 V
⋮									⋮
254	H	H	H	H	H	H	H	L	4.996 V
255	H	H	H	H	H	H	H	H	5.000 V

†For V_{CC} = 5 V, V_{ref} = 3.976 V

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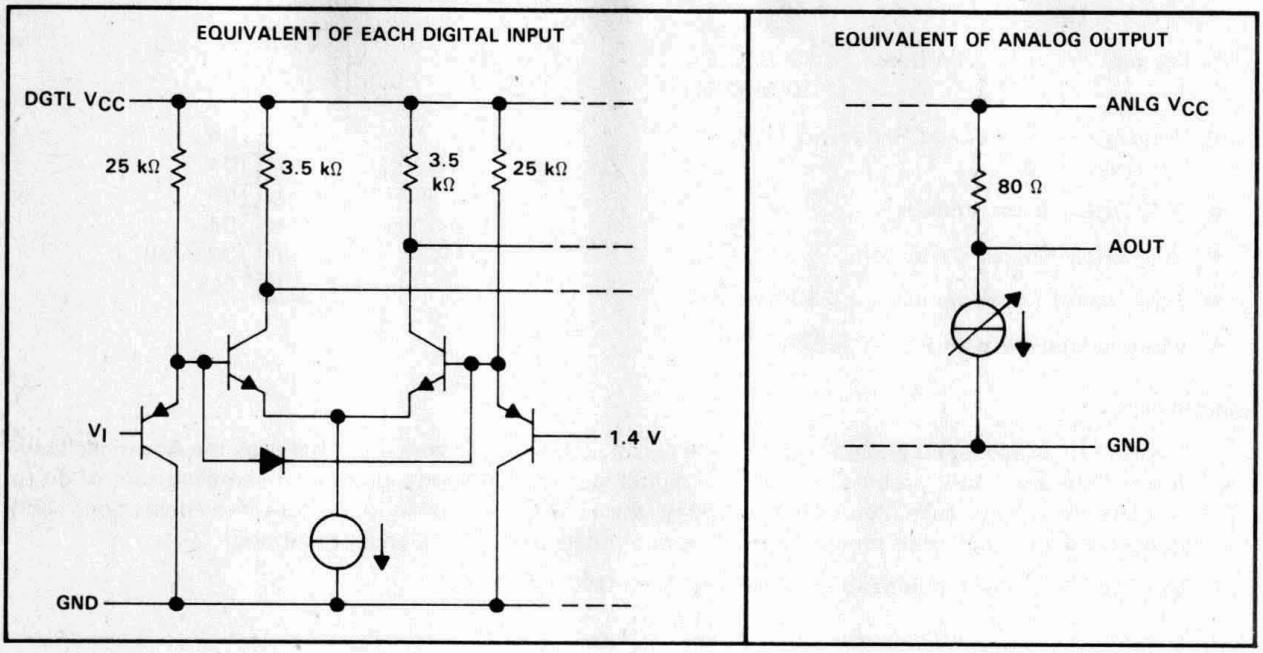
schematics of equivalent input and output circuits



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, ANLG V_{CC}, DGTL V_{CC} . . . . . −0.5 V to 7 V
Digital input voltage range, V_I . . . . . −0.5 V to 7 V
Analog reference voltage range, V_{ref} . . . . . 3.8 V to V_{CC} +0.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{ref}	Analog reference voltage (see Note 1)	3.8	4	4.2	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
t_w	Pulse duration, CLK high or low	25			ns
t_{su}	Setup time, data before CLK↑	12.5			ns
t_h	Hold time, data after CLK↑	12.5			ns
C_{comp}	Phase compensation capacitance (see Note 2)	1			μF
T_A	Operating free-air temperature	0		70	°C

NOTES: 1. $V_{CC} - V_{ref} \leq 1.2$ V
2. This capacitor should be connected between COMP and GND.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_I	Input current at maximum input voltage	V_{CC} = 5.25 V, V_I = 7 V		0	100	μA
I_{IH}	High-level input current	V_{CC} = 5.25 V, V_I = 2.7 V		0	20	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V, V_I = 0.4 V		−40	−400	μA
I_{ref}	Input reference current	V_{ref} = 4 V			10	μA
V_{FS}	Full-scale analog output voltage	V_{CC} = 5 V, V_{ref} = 3.976 V,	V_{CC}−15	V_{CC}	V_{CC}+15	mV
V_{ZS}	Zero-scale analog output voltage	I_O = 0 (no load)	3.919	3.980	4.042	V
r_o	Output resistance	T_A = 25°C	70	80	90	Ω
I_{CC}	Supply current	V_{ref} = 4.05 V		50	75	mA

†All typical values are at V_{CC} = 5 V, V_{ref} = 4 V, T_A = 25°C

operating characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
E_L	Linearity error				±0.2	%FSR
f_{max}	Maximum conversion rate		20	30		MHz

PARAMETER MEASUREMENT INFORMATION

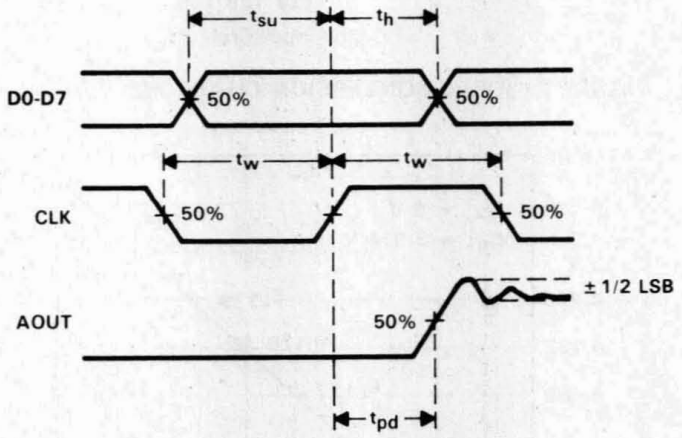


FIGURE 1. VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS

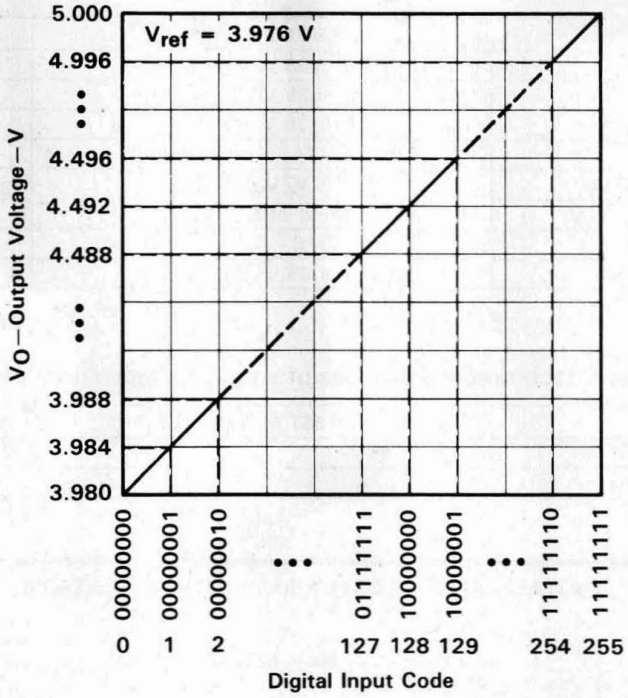


FIGURE 2. IDEAL CONVERSION CHARACTERISTICS

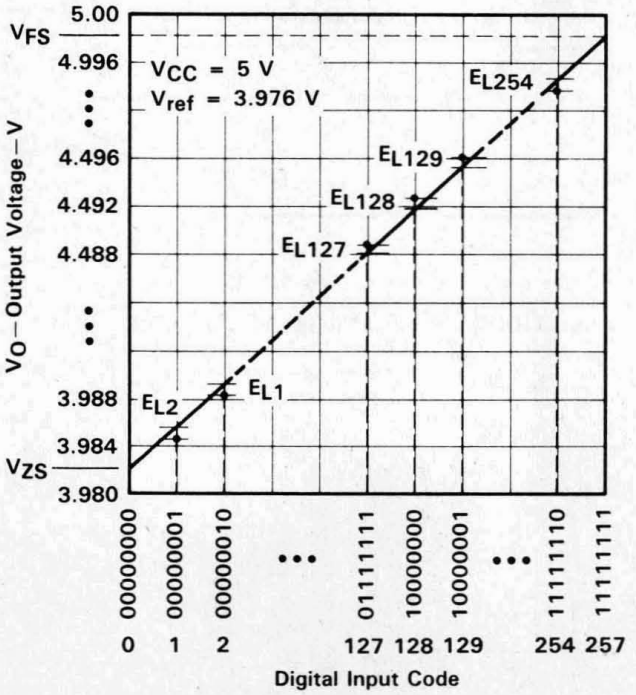
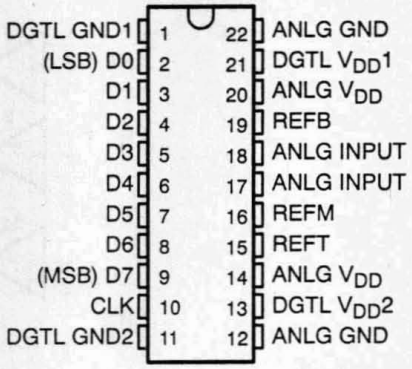


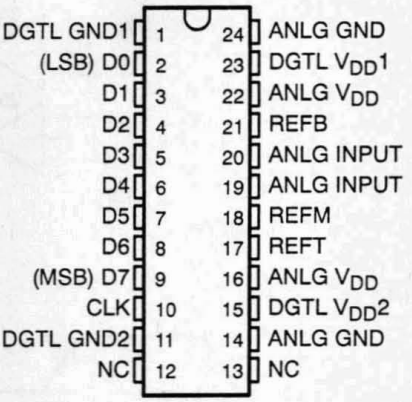
FIGURE 3. END-POINT LINEARITY ERROR

- **LinEPIC™ 1-μm CMOS Process**
- **8-Bit Resolution**
- **Differential Linearity Error . . . ±0.2% Max**
- **Maximum Conversion Rate . . . 20 MHz Typ**
  . . . 10 MHz Min
- **Analog Input Voltage Range . . . 0 V to V_{DD}**
- **TTL Digital I/O Level**
- **Low Power Consumption . . . 150 mW Typ**
- **5-V Single-Supply Operation**

N PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



NC–No internal connection

description

The TLC5502-5 is a low-power ultra-high-speed 8-bit analog-to-digital converter that uses the LinEPIC™ CMOS process. It utilizes the full parallel comparison (flash method) for high-speed conversion. Because of such high-speed capability, the TLC5502-5 is suitable for hard disk drive, motor control, multimedia, and high-speed signal processing.

Separate analog and digital supply pins are provided to reduce coupling between the high-speed digital switching sections and the lower-frequency analog signal comparators. This pin partitioning minimizes crosstalk and unwanted spurious signals.

The TLC5502-5 is characterized for operation from 0°C to 70°C.

During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

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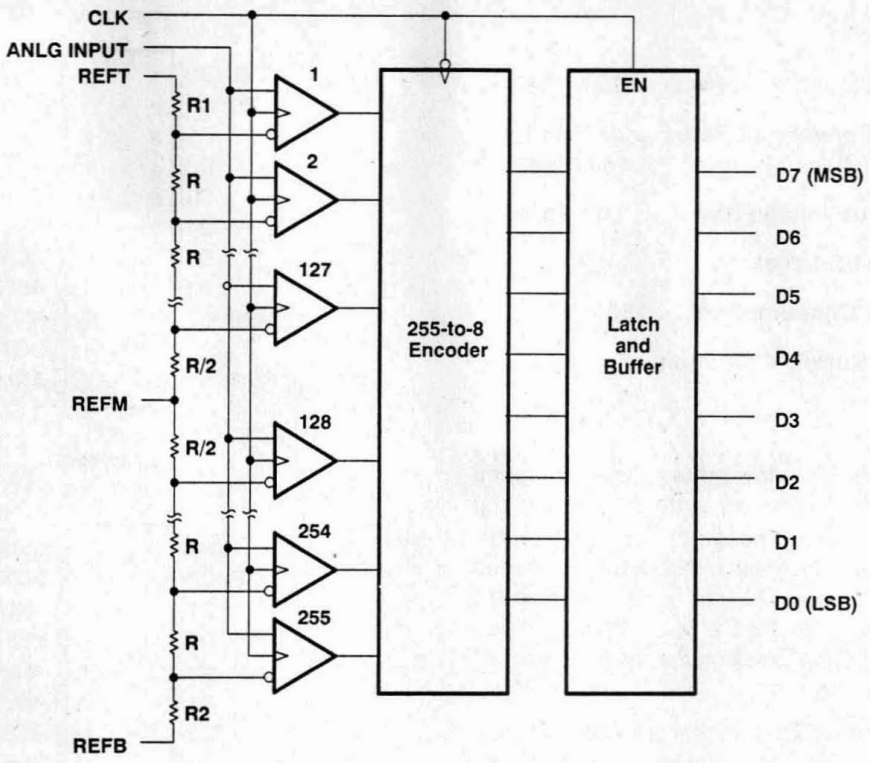
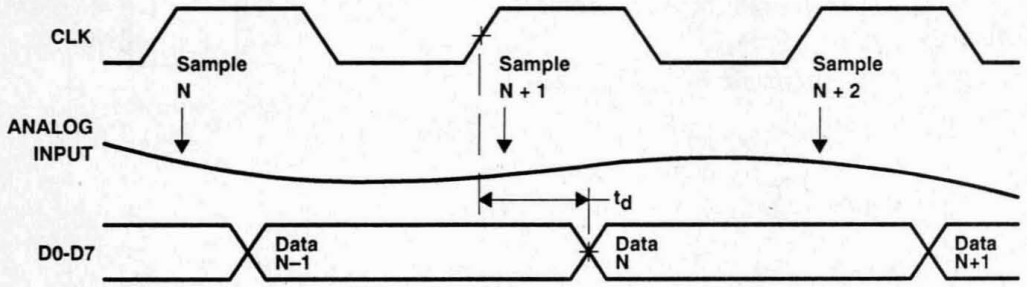
functional block diagram

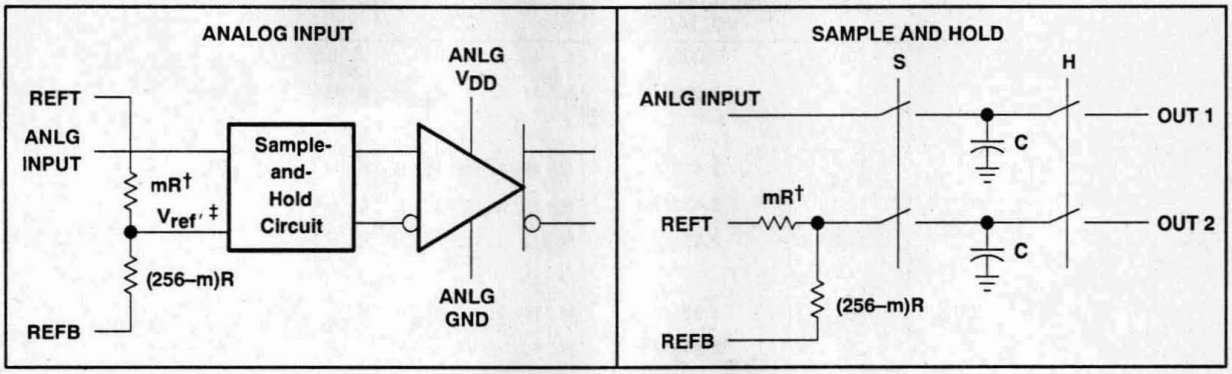


operating sequence



Following the operating sequence above, the rising edge of the clock samples the analog input (sample N) at time t_N and latches sample N−1 at the output. Sample N is encoded to eight digital lines on the next falling edge of the clock and then the following high clock level latches these eight bits to the outputs (with a delay t_d) and acquires sample N + 1. Conversion is completed in one clock cycle and continues the sequence for the next cycle.

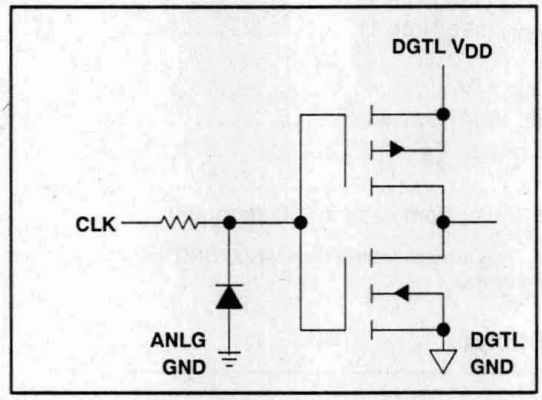
equivalents of analog input circuit



† m = comparator position along the resistor string.

‡ $V_{ref}' = [V_{refT} - V_{refB}] \left[1 - \frac{M}{256}\right] + V_{refB}$

equivalent of digital input circuit



FUNCTION TABLE

STEP	ANALOG INPUT VOLTAGE†	DIGITAL OUTPUT CODE
0	0.000 V	L L L L L L L L
1	0.019 V	L L L L L L L H
. . .	. . .	. . .
127	2.413 V	L H H H H H H H
128	2.432 V	H L L L L L L L
129	2.451 V	H L L L L L L H
. . .	. . .	. . .
254	4.826 V	H H H H H H H L
255	4.845 V	H H H H H H H H

† These values are based on the assumption that V_{refB} and V_{refT} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 0 V and the transition to full scale (V_{FT}) is 4.8545 V. 1 LSB = 19 mV.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, ANLG V_{DD} (see Note 1) . . . . . −0.5 V to 7 V
Supply voltage range, DGTL V_{DD} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage range at CLK, V_I . . . . . −0.3 V to DGTL V_{DD} + 0.3 V
Input voltage range at analog input, V_I . . . . . −0.5 V to ANLG V_{DD} + 0.5 V
Analog reference voltage range, V_{ref} . . . . . −0.5 V to ANLG V_{DD} + 0.5 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: Voltages at analog inputs and ANLG V_{DD} are with respect to the ANLG GND terminals. Voltages at the digital outputs and DGTL V_{DD} are with respect to the DGTL GND terminals.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, ANLG V_{DD}	4.75	5	5.25	V
Supply voltage, DGTL V_{DD}	4.75	5	5.25	V
High-level input voltage, V_{IH}, CLK	2			V
Low-level input voltage V_{IL}, CLK			0.8	V
Input voltage at analog input, V_I	0		5	V
Analog reference voltage (top side), V_{refT}		ANLG V_{DD}		V
Analog reference voltage (midpoint), V_{refM}		$\frac{V_{refT} - V_{refB}}{2}$		V
Analog reference voltage (bottom side), V_{refB}		0		V
Differential reference voltage, $V_{refT} - V_{refB}$		5		V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			4	mA
Clock pulse duration, high or low, t_{wH} or t_{wL}	50			ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over operating supply voltage range, T_A = 25°C

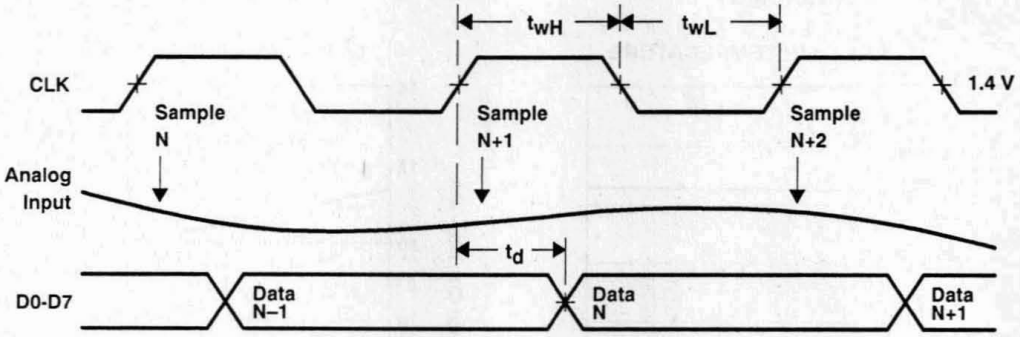
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −400 µA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA			0.4	V
I_I	Analog input current	V_I = 0 to 5 V, f_{clock} = 10 MHz		±0.5		mA
I_{IH}	Digitial high-level input current	V_I = 5 V			1	µA
I_{IL}	Digital low-level input current	V_I = 0			−1	µA
I_{refB}	Reference current	V_{refB} = 0		−10	−20	mA
I_{refT}	Reference current	V_{refT} = 5 V		10	20	mA
C_i	Analog input capacitance			50		pF
I_{DD}	Supply current	f_{clock} = 10 MHz		30	60	mA

operating characteristics over operating supply voltage range, T_A = 25°C

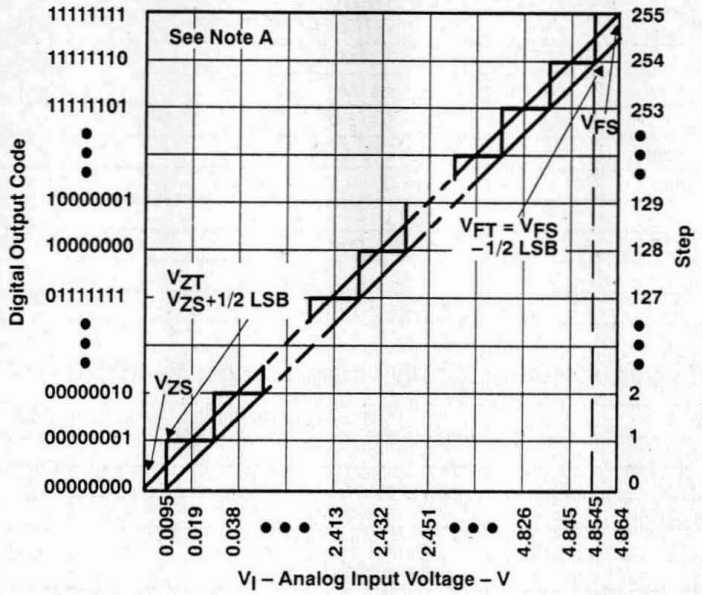
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{c(max)}$	Maximum conversion rate		10	20		MHz
E_D	Linearity error, differential	V_I = 0 to 5 V		±0.1	±0.2	%FSR
E_L	Linearity error, best straight line	V_I = 0 to 5 V			±0.4	%FSR
SNR†	Signal to noise ratio	f_{clock} = 9.9 MHz, f_{IN} = 97 kHz, BW = 5 MHz		−50		dB
THD	Total harmonic distortion			51		dB
BW	Analog input bandwidth (3 dB)	f_{clock} = 10 MHz		5		MHz
t_d	Digital output delay time	C_L = 15 pF		10	30	ns

† SNR is total noise without THD.

timing diagram



TYPICAL CHARACTERISTICS



NOTE A: This curve is based on the assumption that V_{refB} and V_{refT} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 0 and the transition to full scale (V_{FT}) is 4.8545 V. 1 LSB = 19 mV.

Figure 1. Ideal Conversion Characteristics

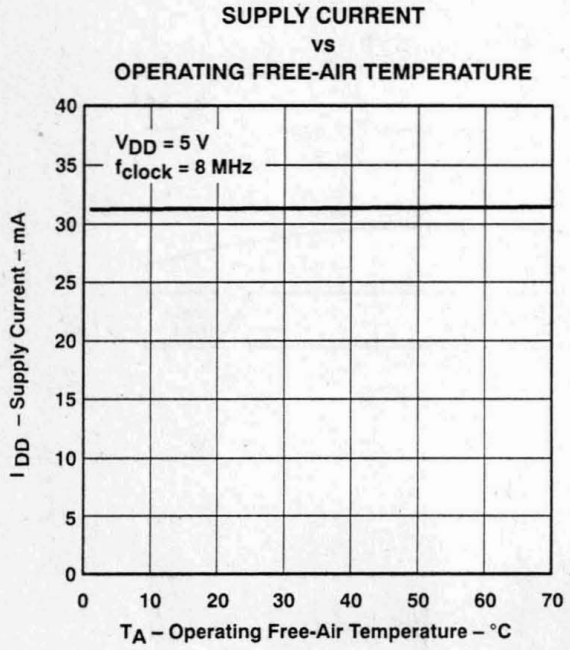


Figure 2

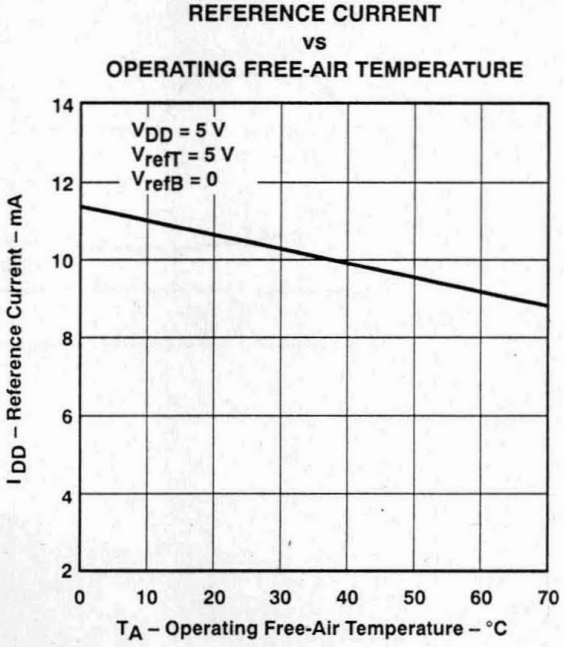


Figure 3

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION
vs
OPERATING FREE-AIR TEMPERATURE

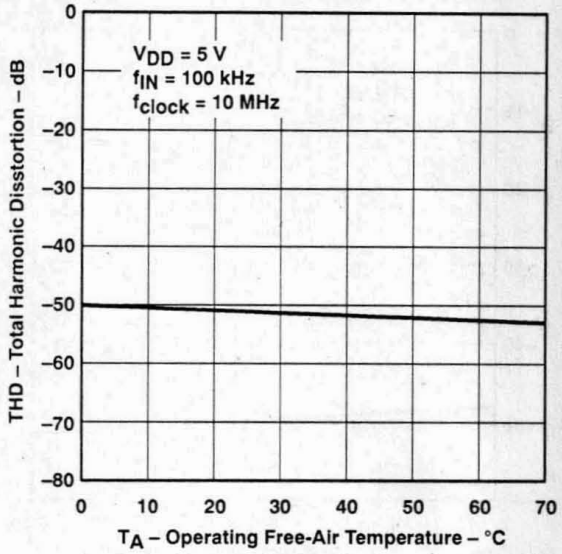


Figure 4

TOTAL HARMONIC DISTORTION
vs
OPERATING FREE-AIR TEMPERATURE

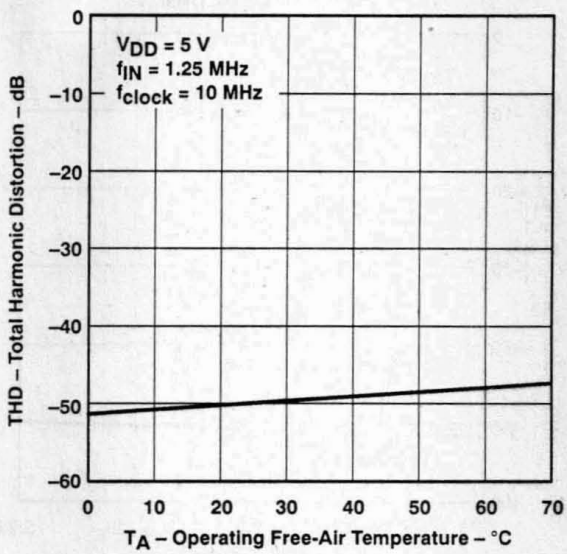


Figure 5

DIFFERENTIAL LINEARITY ERROR
vs
SUPPLY VOLTAGE

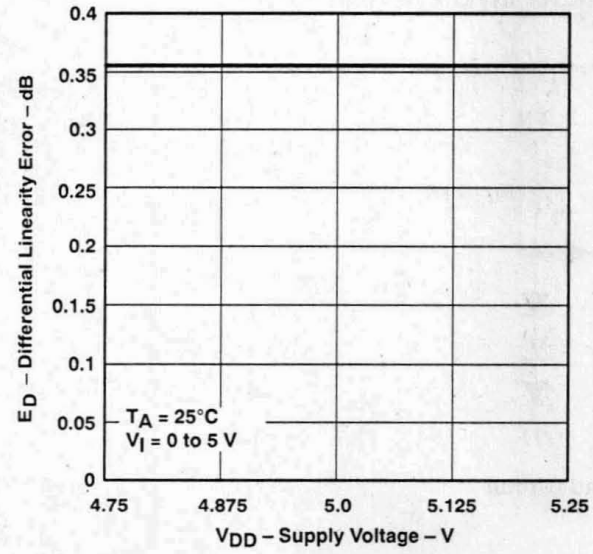


Figure 6

DIFFERENTIAL LINEARITY ERROR
vs
OPERATING FREE-AIR TEMPERATURE

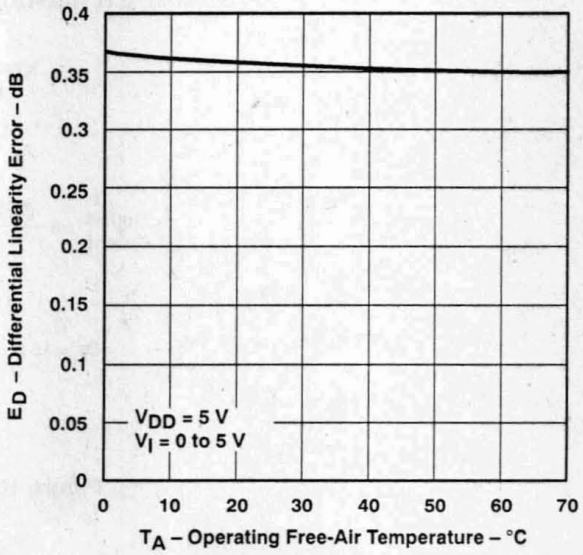


Figure 7

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION
vs
SUPPLY VOLTAGE

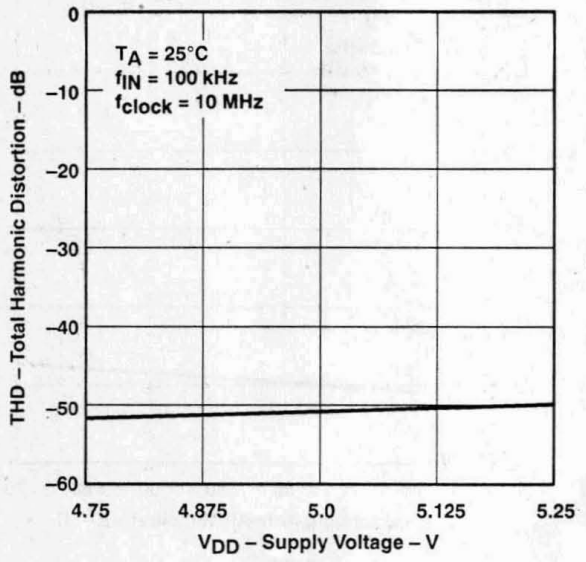


Figure 8

TOTAL HARMONIC DISTORTION
vs
SUPPLY VOLTAGE

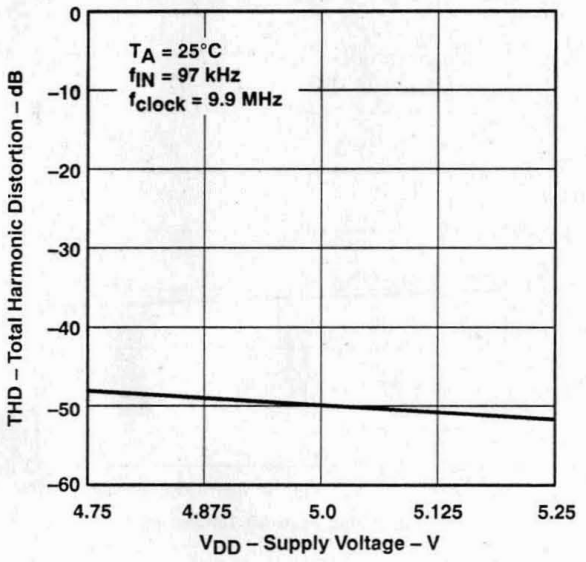


Figure 9

PARAMETER MEASUREMENT INFORMATION

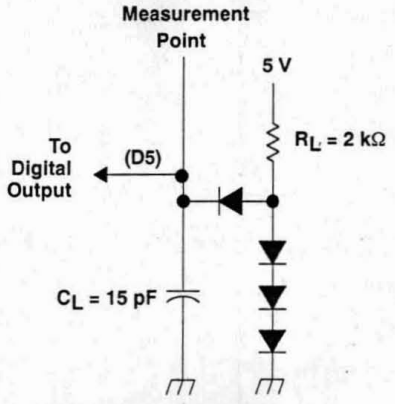


Figure 10. Load Circuit

APPLICATIONS INFORMATION

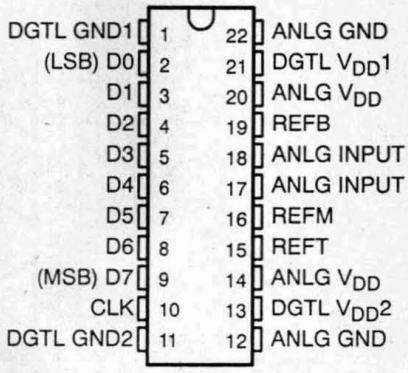
The following design recommendations will benefit the TLC5502-5 user:

1. External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
2. RF breadboarding or PCB techniques should be used throughout the evaluation and production process. Breadboards should be copper clad for bench evaluation.
3. Since the ANLG GND, DGTL GND1, and DGTL GND2 are not connected internally, these pins need to be connected externally. With breadboards, these ground lines should be connected through separate leads with proper supply bypassing. A good method to use is a separate twisted-pair cables for the supply lines to minimize noise pickup. An analog and digital ground plane should be used on PCB layouts.
4. Since the ANLG V_{DD}, DGTL $V_{DD}1$, and DGTL $V_{DD}2$ are not connected internally, these pins also need to be connected externally. To connect ANLG V_{DD}, DGTL $V_{DD}1$, and DGTL $V_{DD}2$, a 50-Ω resistor should be placed in series with the DGTL $V_{DD}1$ pin and then a 0.1-μF capacitor to ground before being connected to the ANLG V_{DD} and DGTL V_{DD2}.
5. ANLG V_{DD} to ANLG GND, DGTL $V_{DD}1$ to DGTL GND1, and DGTL $V_{DD}2$ to DGTL GND2 should be decoupled with 1-μF and 0.01-μF capacitors, respectively, as close as possible to the appropriate device pins. A ceramic chip capacitor is recommended for the 0.01-μF capacitor. Care should be exercised to assure a solid noise free ground connection for the analog and digital grounds.
6. The no connection (NC) pins on the small-outline package should be connected to ground.
7. ANLG V_{DD}, ANLG GND, and the ANLG INPUT pins should be shielded from the higher-frequency pins, CLK and D0-D7. If possible, ANLG GND traces should be placed on both sides of the ANLG INPUT traces on the PCB.
8. In testing or application of the device, the resistance of the driving source connected to the analog input should be 10 Ω or less within the analog frequency range of interest.

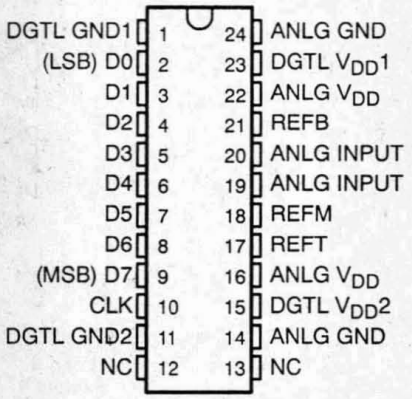
D3739, FEBRUARY 1991–REVISED NOVEMBER 1991

- **LinEPIC™ 1-μm CMOS Process**
- **8-Bit Resolution**
- **Differential Linearity Error . . . ±0.4% Max**
- **Maximum Conversion Rate . . . 25 MHz Typ**
  . . . 20 MHz Min
- **Analog Input Voltage Range . . . 3 V to V_{DD}**
- **TTL Digital I/O Level**
- **Low Power Consumption . . . 190 mW Typ**
- **5-V Single-Supply Operation**

N PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



NC–No internal connection

description

The TLC5503-2 is a low-power ultra-high-speed video-band 8-bit analog-to-digital converter manufactured using the LinEPIC™ CMOS process. It uses full-parallel comparison (flash method) for high-speed conversion of a wide-band analog signal (such as a video signal) to a digital signal at a sampling rate of dc to 25 MHz. Its high-speed capability makes the TLC5503-2 suitable for digital video applications such as digital TV, video processing with a computer, or radar signal processing.

Separate analog and digital supply pins are provided to reduce coupling between the high-speed digital switching sections and the lower-frequency analog signal comparators. This pin partitioning minimizes crosstalk and spurious signals. The two analog inputs (pins 17 and 18 on the N package; pins 19 and 20 on the DW package) should be connected together externally. The REFM input (pin 16 on the N package; pin 18 on the DW package) can be used to adjust for small tolerances in the resistor voltage divider by applying an external midpoint voltage.

The TLC5503-2 is characterized for operation from 0°C to 70°C.

During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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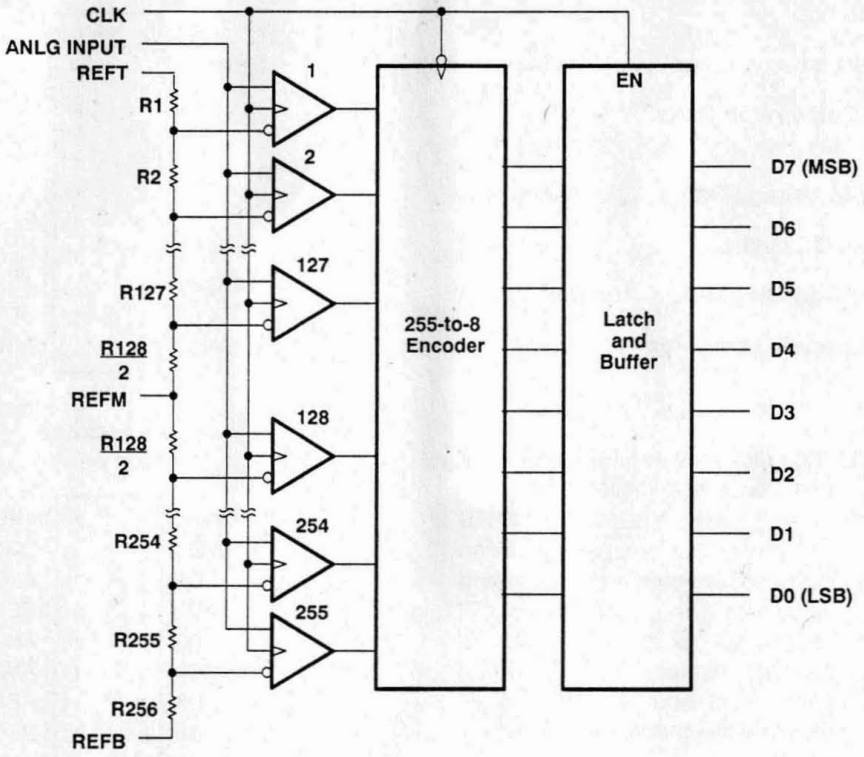
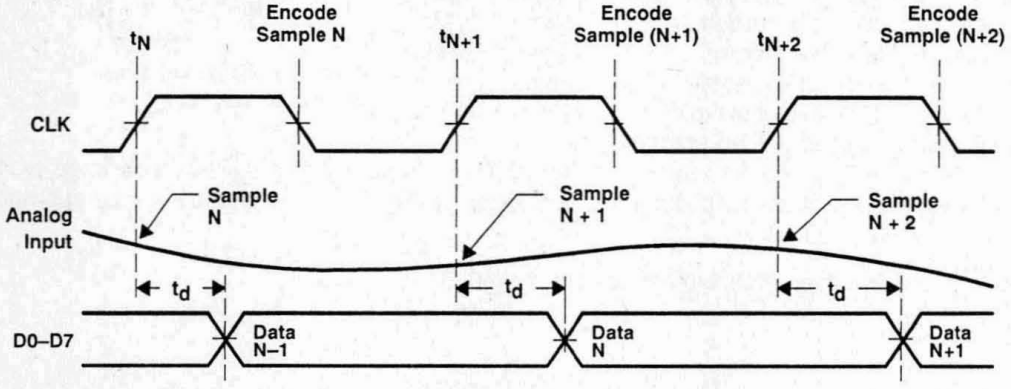
functional block diagram

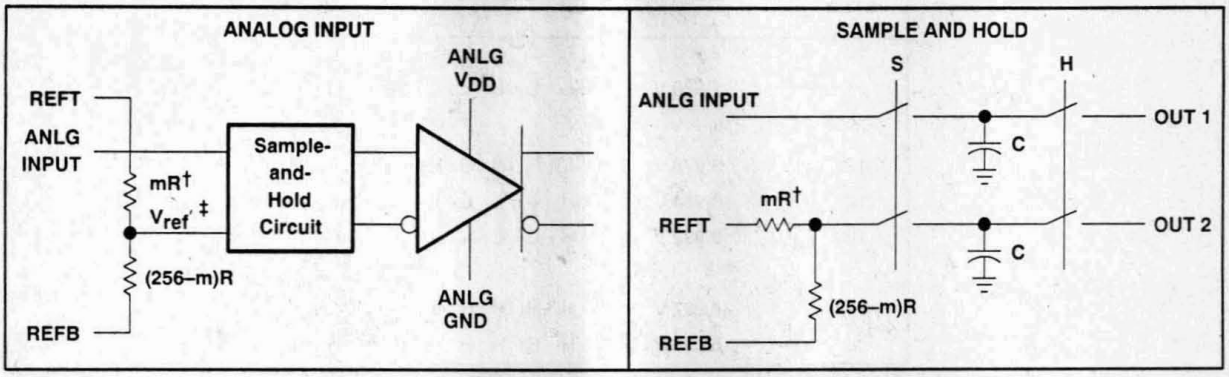


operating sequence



Following the operating sequence above, the rising edge of the clock samples the analog input (sample N) at time t_N and latches sample N−1 at the output (with a delay t_d). Sample N is encoded to eight digital lines on the next falling edge of the clock and then the following high clock level latches these eight bits to the outputs (with a delay t_d) and acquires sample N + 1. Conversion is completed in one clock cycle and continues the sequence for the next cycle.

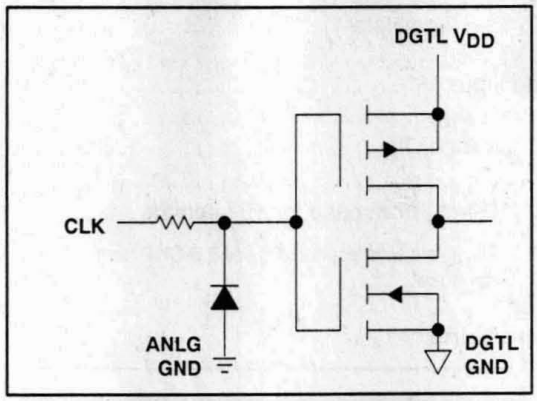
equivalents of analog input circuit



† m = comparator position along the resistor string.

‡ $V_{ref}' = [V_{refT} - V_{refB}] \left[1 - \frac{M}{256}\right] + V_{refB}$

equivalent of digital input circuit



FUNCTION TABLE

STEP	analog input VOLTAGE†	DIGITAL OUTPUT CODE
0	2.960 V	L L L L L L L L
1	2.968 V	L L L L L L L H
. . .	. . .	. . .
127	3.976 V	L H H H H H H H
128	3.984 V	H L L L L L L L
129	3.992 V	H L L L L L L H
. . .	. . .	. . .
254	4.992 V	H H H H H H H L
255	5.000 V	H H H H H H H H

† These values are based on the assumption that V_{refB} and V_{refT} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 2.964 V and the transition to full scale (V_{FT}) is 4.996 V . 1 LSB = 8 mV.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, ANLG V_{DD} (see Note 1) . . . . . −0.5 V to 7 V
Supply voltage range, DGTL V_{DD} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage range at CLK, V_I . . . . . −0.3 V to DGTL V_{DD} + 0.3 V
Input voltage range at analog input, V_I . . . . . −0.5 V to ANLG V_{DD} + 0.5 V
Analog reference voltage range, V_{ref} . . . . . −0.5 V to ANLG V_{DD} + 0.5 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: Voltages at analog inputs and ANLG V_{DD} are with respect to the ANLG GND terminals. Voltages at the digital outputs and DGTL V_{DD} are with respect to the DGTL GND terminals.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, ANLG V_{DD}	4.75	5	5.25	V
Supply voltage, DGTL V_{DD}	4.75	5	5.25	V
High-level input voltage, V_{IH}, CLK	2			V
Low-level input voltage, V_{IL}, CLK			0.8	V
Input voltage at analog input, V_I	3		5	V
Analog reference voltage (top side), V_{refT}		ANLG V_{DD}		V
Analog reference voltage (midpoint), V_{refM}		$\frac{V_{refT} - V_{refB}}{2}$		V
Analog reference voltage (bottom side), V_{refB}	2.5	3		V
Differential reference voltage, $V_{refT} - V_{refB}$		2		V
High-level output current, I_{OH}			−400	µA
Low-level output current, I_{OL}			4	mA
Clock pulse duration, high-level or low-level, t_{wH} or t_{wL}	25			ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over operating supply voltage range, T_A = 25°C

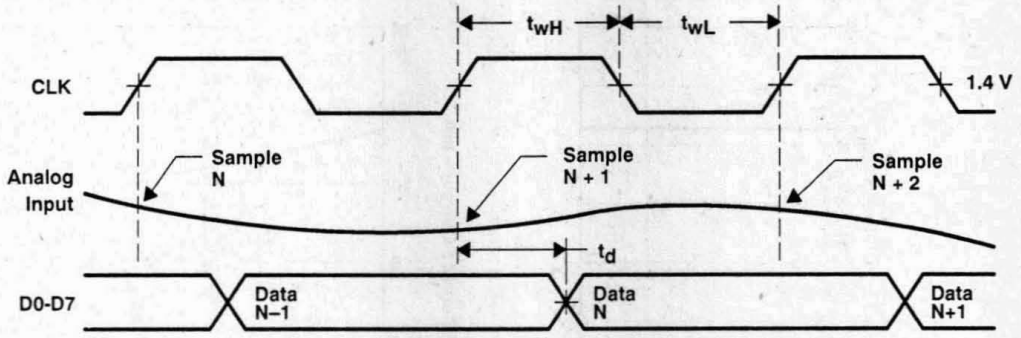
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −400 µA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA			0.4	V
I_I	Analog input current	V_I = 3 to 5 V, f_{clock} = 15 MHz		±0.3		mA
I_{IH}	Digitial high-level input current	V_I = 5 V			1	µA
I_{IL}	Digital low-level input current	V_I = 0			−1	µA
I_{refB}	Reference current	V_{refB} = 3 V		−12	−20	mA
I_{refT}	Reference current	V_{refT} = 5 V		12	20	mA
C_i	Analog input capacitance			50		pF
I_{DD}	Supply current	f_{clock} = 15 MHz		37	60	mA

operating characteristics over operating supply voltage range, T_A = 25°C

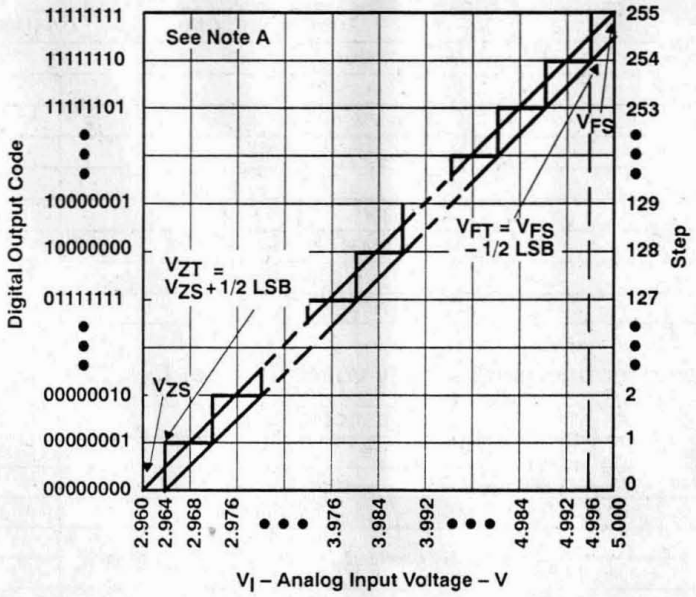
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum conversion rate		20	25		MHz‡
E_D	Linearity error, differential	V_I = 3 V to 5 V, f_{clock} = 15 MHz			±0.4	%FSR
E_L	Linearity error, best straight line	V_I = 3 V to 5 V, f_{clock} = 15 MHz			±0.4	%FSR
G_{diff}	Differential gain	NTSC 40-IRE modulated ramp, f_{clock} = 14.4 MHz		0.9%		
ϕ_{diff}	Differential phase			0.6°		
SNR†	Signal to noise ratio	f_{clock} = 16.4 MHz, f_{IN} = 1.248 MHz (90% P-P), BW = 8.2 MHz		48		dB
THD	Total harmonic distortion			−50		dB
t_d	Digital output dalay time	C_L = 15 pF		10	30	ns

† SNR does not include THD.
‡ No missing codes.

timing diagram



TYPICAL CHARACTERISTICS



NOTE A: This curve is based on the assumption that V_{refB} and V_{refT} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 2.964 V and the transition to full scale (V_{FT}) is 4.996 V. 1 LSB = 8 mV.

Figure 1. Ideal Conversion Characteristics

SUPPLY CURRENT vs OPERATING FREE-AIR TEMPERATURE

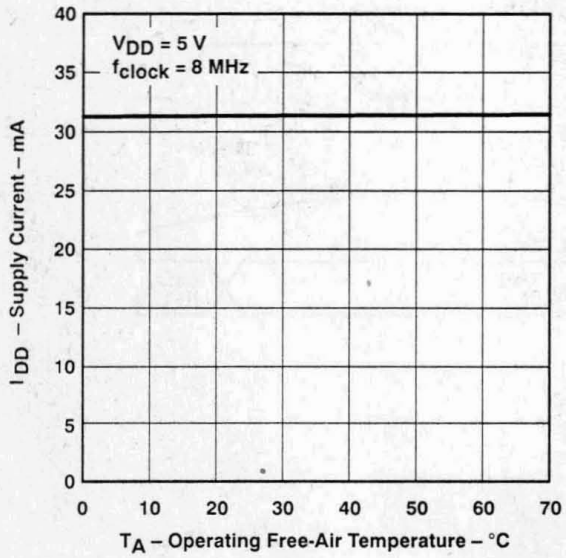


Figure 2

REFERENCE CURRENT vs OPERATING FREE-AIR TEMPERATURE

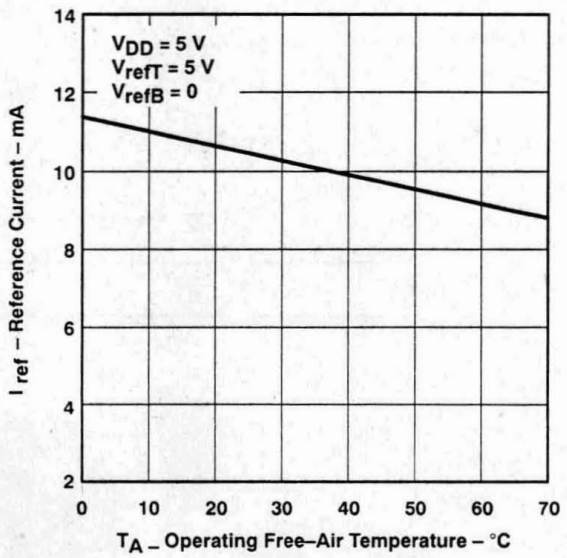


Figure 3

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION
vs
OPERATING FREE-AIR TEMPERATURE

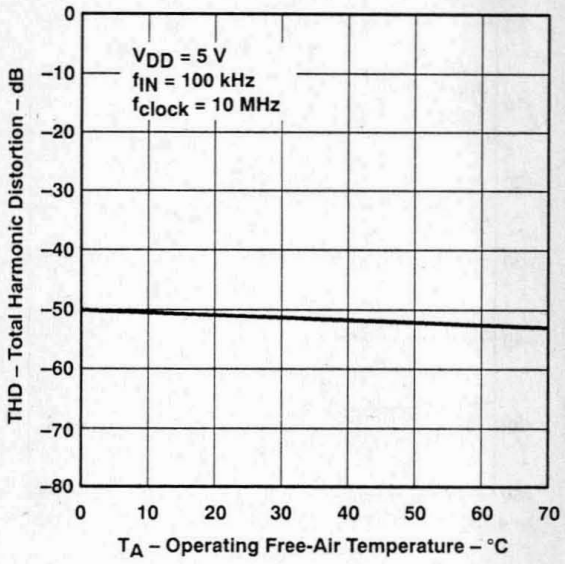


Figure 4

TOTAL HARMONIC DISTORTION
vs
OPERATING FREE-AIR TEMPERATURE

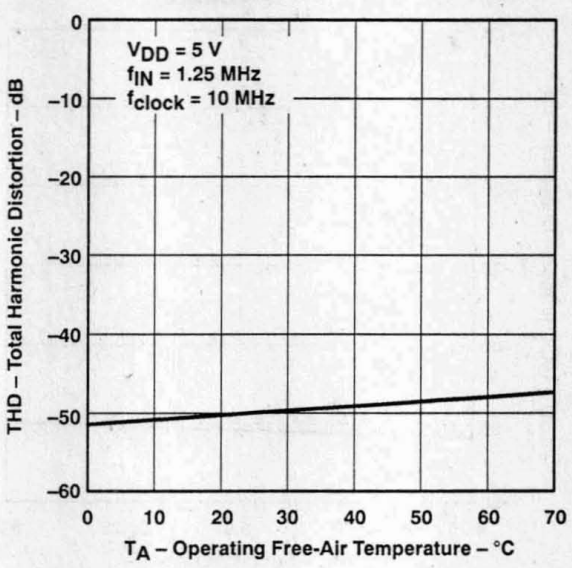


Figure 5

DIFFERENTIAL LINEARITY ERROR
vs
SUPPLY VOLTAGE

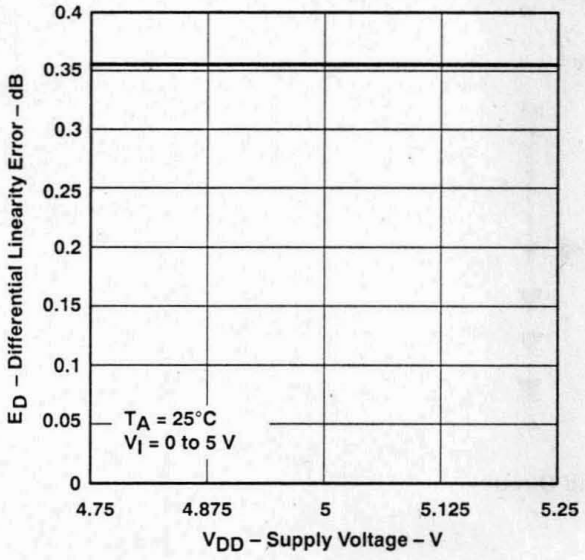


Figure 6

DIFFERENTIAL LINEARITY ERROR
vs
OPERATING FREE-AIR TEMPERATURE

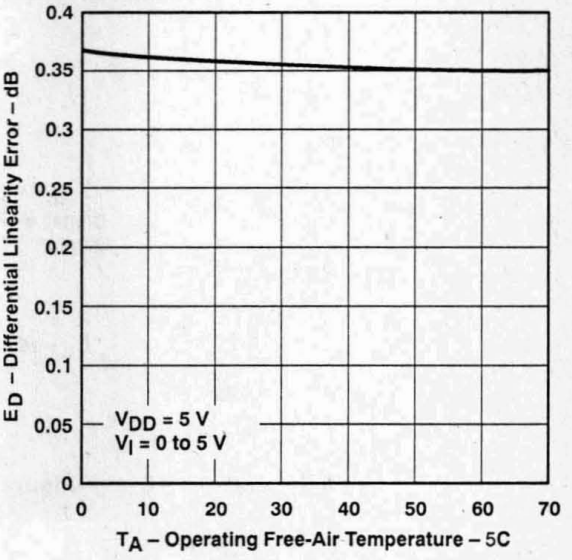


Figure 7

TYPICAL CHARACTERISTICS

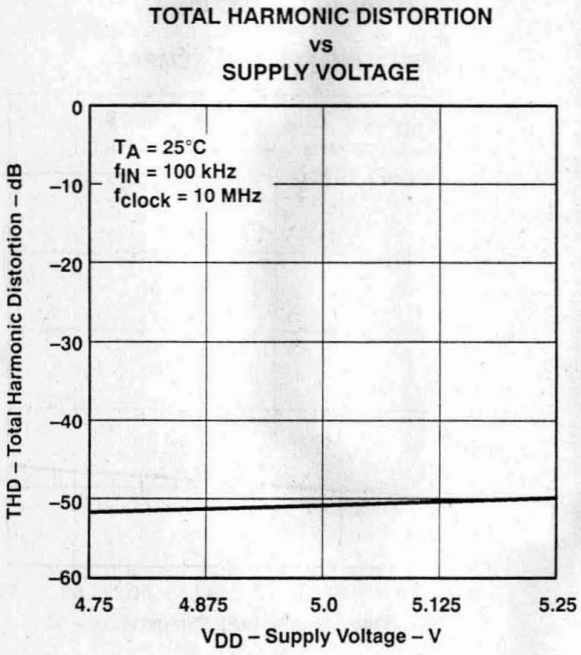


Figure 8

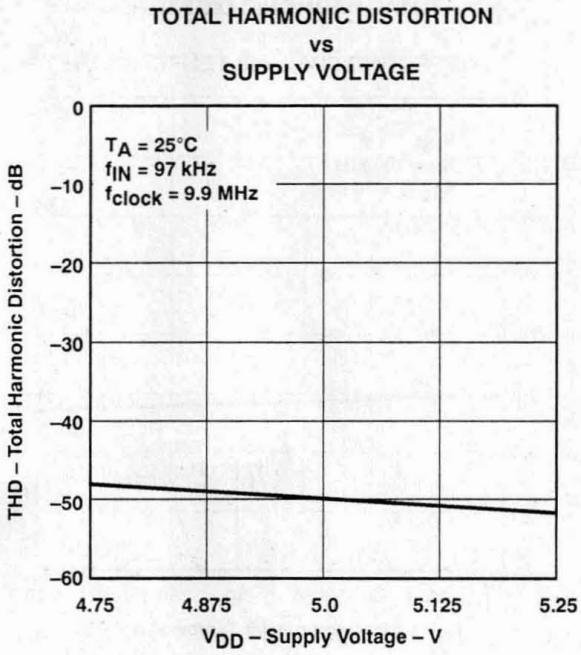


Figure 9

PARAMETER MEASUREMENT INFORMATION

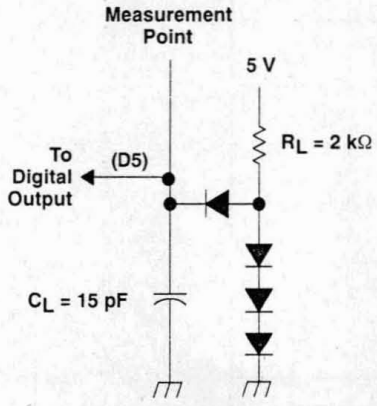


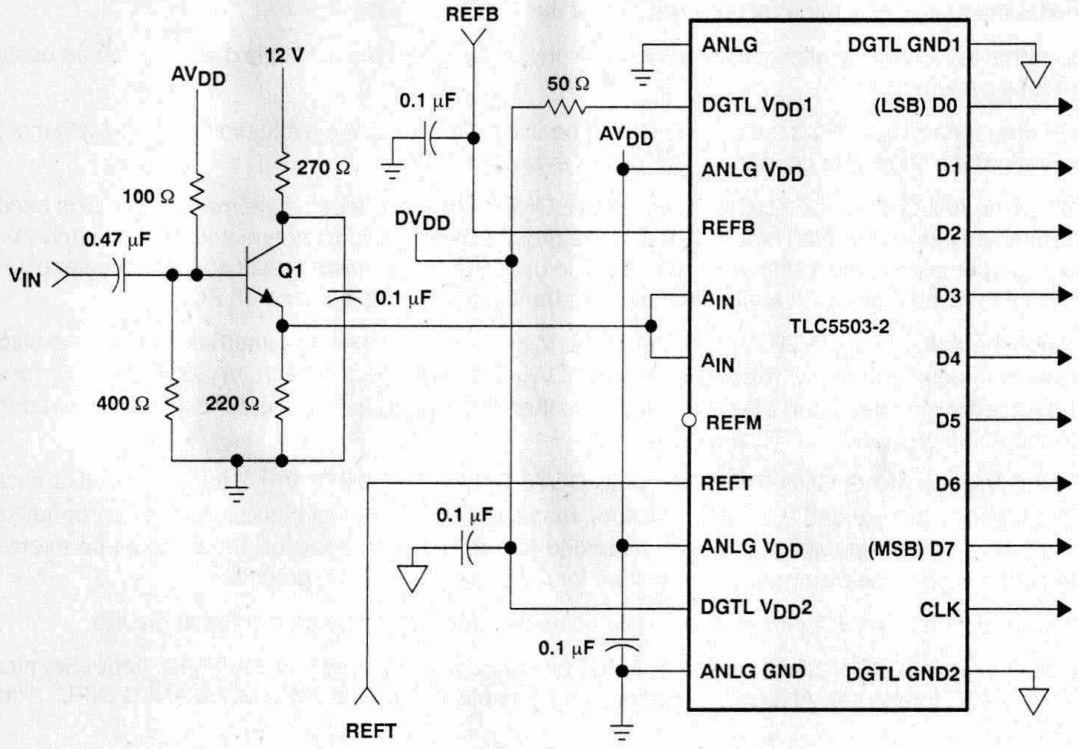
Figure 10. Load Circuit

APPLICATION INFORMATION

The following design recommendations will benefit the TLC5503-2 user:

1. External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
2. RF breadboarding or PCB techniques should be used throughout the evaluation and production process. Breadboards should be copper clad for bench evaluation.
3. Since the ANLG GND, DGTL GND1, and DGTL GND2 are not connected internally, these pins need to be connected externally. With breadboards, these ground lines should be connected through separate leads with proper supply bypassing. A good method to use is separate twisted-pair cables for the supply lines to minimize noise pickup. An analog and digital ground plane should be used on PCB layouts.
4. Since the ANLG V_{DD}, DGTL $V_{DD}1$, and DGTL $V_{DD}2$, are not connected internally, these pins also need to be connected externally. To connection ANLG V_{DD} to DGTL $V_{DD}1$ or DGTL $V_{DD}2$, a 50-Ω resistor should be placed in series with the DGTL $V_{DD}1$ pin and then a 0.1-μF capacitor to ground before being connected to the ANLG V_{DD}, and DGTL $DV_{DD}2$ supply.
5. ANLG V_{DD} to ANLG GND, DGTL $V_{DD}1$ to DGTL GND1, and DGTL $V_{DD}2$ to DGTL GND2 should be decoupled with 1-μF and 0.01-μF capacitors, respectively, as close as possible to the appropriate device pins. A ceramic chip capacitor is recommended for the 0.01-μF capacitor. Care should be exercised to assure a solid noise-free ground connection for the analog and digital grounds.
6. The no connection (NC) pins on the small-outline package should be connected to ground.
7. ANLG V_{DD}, ANLG GND, and the ANLG INPUT pins should be shielded from the higher-frequency pins, CLK and D0-D7. If possible, ANLG GND traces should be placed on both sides of the ANLG INPUT traces on the PCB.
8. In testing or application of the device, the resistance of the driving source connected to the analog input should be 10 Ω or less within the analog frequency range of interest.

APPLICATION INFORMATION

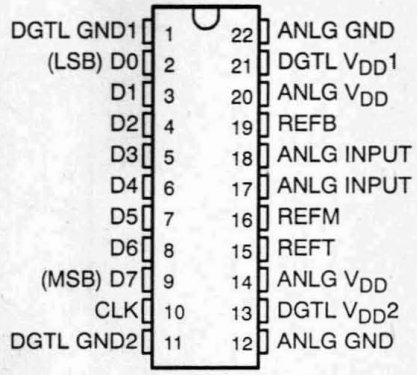


NOTES: A. All resistors are 1/4 W carbon.
B. Q1 is 2N3414 or equivalent.
C. All capacitors are ceramic with as short leads as possible.

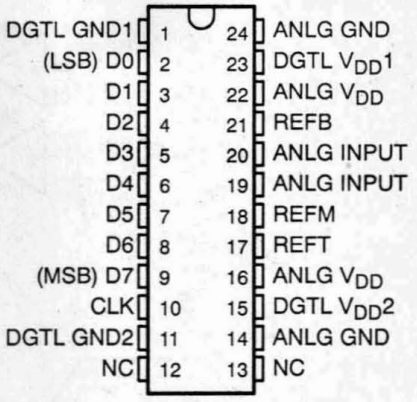
D3637, OCTOBER 1990–REVISED OCTOBER 1991

- **LinEPIC™ 1-μm CMOS Process**
- **8-Bit Resolution**
- **Differential Linearity Error . . . ±0.4% Max**
- **Maximum Conversion Rate . . . 20 MHz Typ**
  . . . 10 MHz Min
- **Analog Input Voltage Range . . . 0 V to V_{DD}**
- **TTL Digital I/O Level**
- **Low Power Consumption . . . 150 mW Typ**
- **5-V Single-Supply Operation**

N PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



NC–No internal connection

description

The TLC5503-5 is a low-power ultra-high-speed 8-bit analog-to-digital converter that uses the LinEPIC™ CMOS process. It utilizes the full parallel comparison (flash method) for high-speed conversion. Because of such high-speed capability, the TLC5503-5 is suitable for hard disk drive, motor control, multimedia, and high-speed signal processing.

Separate analog and digital supply pins are provided to reduce coupling between the high-speed digital switching sections and the lower-frequency analog signal comparators. This pin partitioning minimizes crosstalk and unwanted spurious signals.

The TLC5503-5 is characterized for operation from 0°C to 70°C.

During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

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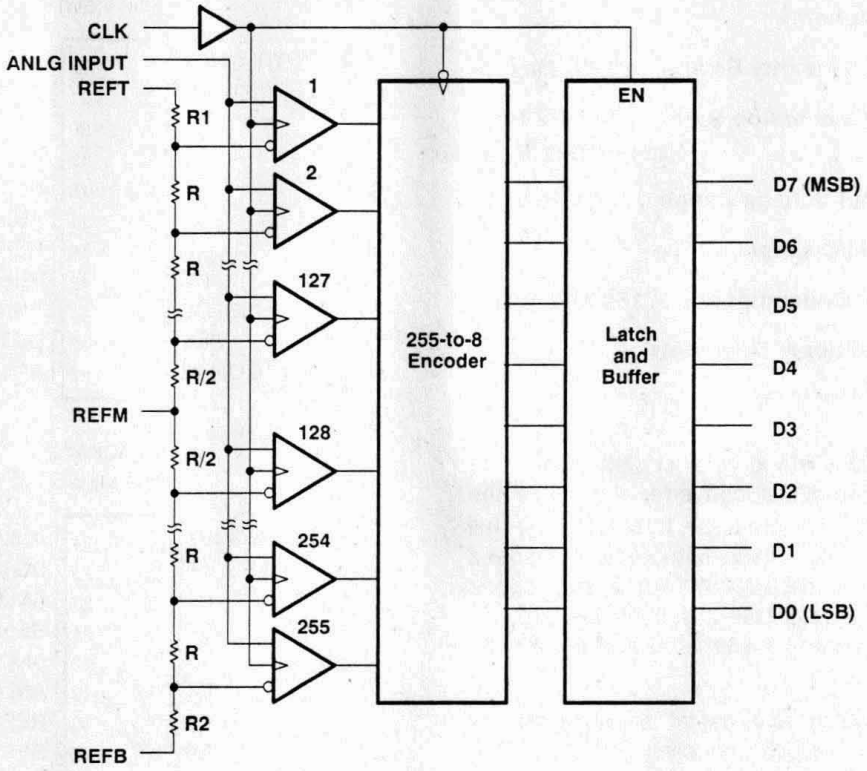
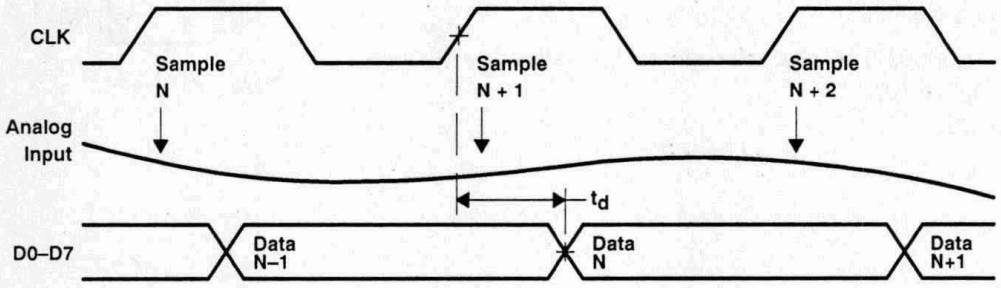
functional block diagram

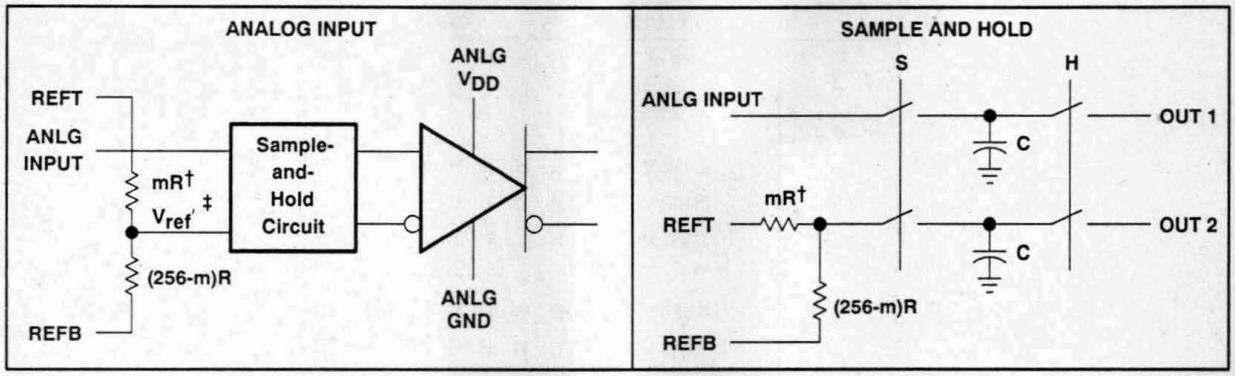


operating sequence



Following the operating sequence above, the rising edge of the clock samples the analog input (sample N) at time t_N and latches sample N−1 at the output. Sample N is encoded to eight digital lines on the next falling edge of the clock and then the following high clock level latches these eight bits to the outputs (with a delay t_d) and acquires sample N + 1. Conversion is completed in one clock cycle and continues the sequence for the next cycle.

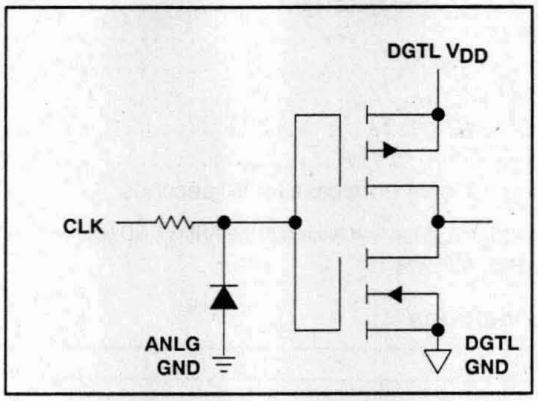
equivalents of analog input circuit



† m = comparator position along the resistor string.

‡ $V_{ref'} = [V_{refT} - V_{refB}] \left[1 - \frac{M}{256}\right] + V_{refB}$

equivalent of digital input circuit



FUNCTION TABLE

STEP	ANALOG INPUT VOLTAGE†	DIGITAL OUTPUT CODE
0	0.000 V	L L L L L L L L
1	0.019 V	L L L L L L L H
⋮	⋮	⋮
127	2.413 V	L H H H H H H H
128	2.432 V	H L L L L L L L
129	2.451 V	H L L L L L L H
⋮	⋮	⋮
254	4.826 V	H H H H H H H L
255	4.845 V	H H H H H H H H

† These values are based on the assumption that V_{refB} and V_{refT} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 0 V and the transition to full scale (V_{FT}) is 4.8545 V. 1 LSB = 19 mV.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, ANLG V_{DD} (see Note 1) ..... −0.5 V to 7 V
Supply voltage range, DGTL V_{DD} (see Note 1) ..... −0.5 V to 7 V
Input voltage range at CLK, V_I ..... −0.3 V to DGTL V_{DD} + 0.3 V
Input voltage range at analog input, V_I ..... −0.5 V to ANLG V_{DD} + 0.5 V
Analog reference voltage range, V_{ref} ..... −0.5 V to ANLG V_{DD} + 0.5 V
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: Voltages at analog inputs and ANLG V_{DD} are with respect to the ANLG GND terminals. Voltages at the digital outputs and DGTL V_{DD} are with respect to the DGTL GND terminals.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, ANLG V_{DD}	4.75	5	5.25	V
Supply voltage, DGTL V_{DD}	4.75	5	5.25	V
High-level input voltage, V_{IH}, CLK	2			V
Low-level input voltage, V_{IL}, CLK			0.8	V
Input voltage at analog input, V_I	0		5	V
Analog reference voltage (top side), V_{refT}		ANLG V_{DD}		V
Analog reference voltage (midpoint), V_{refM}		$\frac{V_{refT} - V_{refB}}{2}$		V
Analog reference voltage (bottom side), V_{refB}		0		V
Differential reference voltage, $V_{refT} - V_{refB}$		5		V
High-level output current, I_{OH}			−400	µA
Low-level output current, I_{OL}			4	mA
Clock pulse duration, high or low, t_{wH} or t_{wL}	50			ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over operating supply voltage range, T_A = 25°C

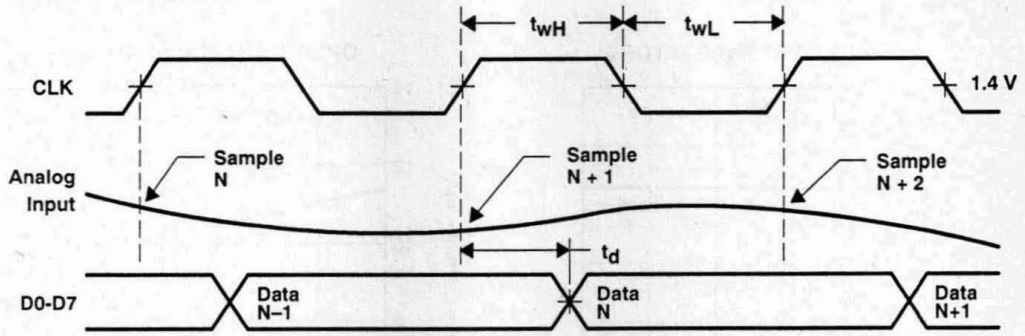
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA			0.4	V
I_I	Analog input current	V_I = 0 to 5 V, f_{clock} = 10 MHz		±0.5		mA
I_{IH}	Digital high-level input current	V_I = 5 V			1	μA
I_{IL}	Digital low-level input current	V_I = 0			−1	μA
I_{refB}	Reference current	V_{refB} = 0		−10	−20	mA
I_{refT}	Reference current	V_{refT} = 5 V		10	20	mA
C_i	Analog input capacitance			50		pF
I_{DD}	Supply current	f_{clock} = 10 MHz		30	60	mA

operating characteristics over operating supply voltage range, T_A = 25°C

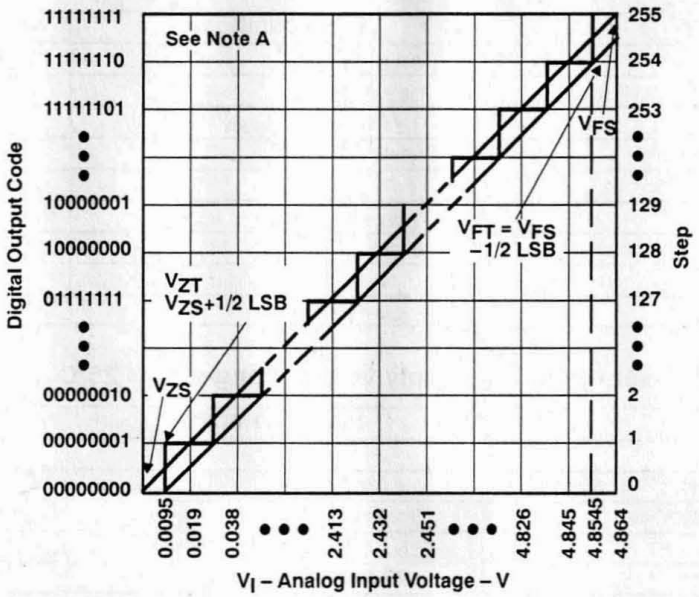
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{c(max)}$	Maximum conversion rate		10	20		MHz
E_D	Linearity error, differential	V_I = 0 to 5 V		±0.1	±0.4	%FSR
E_L	Linearity error, best straight line	V_I = 0 to 5 V			±0.4	%FSR
SNR†	Signal to noise ratio	f_{clock} = 9.9 MHz, f_{IN} = 97 kHz,		−50		dB
THD	Total harmonic distortion	BW = 5 MHz		51		dB
BW	Analog input bandwidth (3 dB)	f_{clock} = 10 MHz		5		MHz
t_d	Digital output delay time	C_L = 15 pF		10	30	ns

† SNR is total noise without THD.

timing diagram



TYPICAL CHARACTERISTICS



NOTE A: This curve is based on the assumption that V_{refB} and V_{refT} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 0 and the transition to full scale (V_{FT}) is 4.8545 V. 1 LSB = 19 mV.

Figure 1. Ideal Conversion Characteristics

SUPPLY CURRENT vs OPERATING FREE-AIR TEMPERATURE

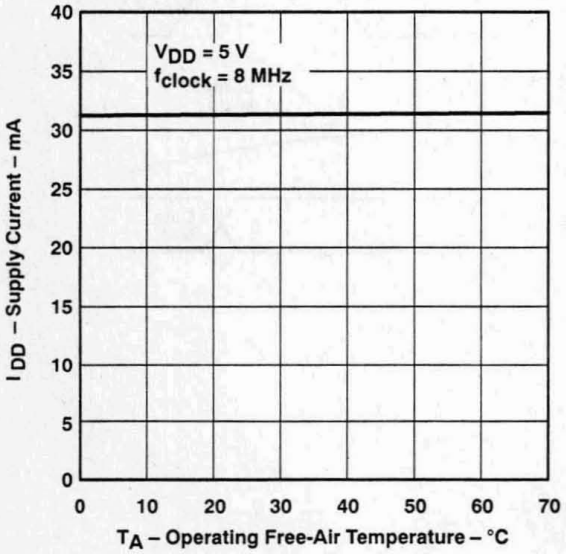


Figure 2

REFERENCE CURRENT vs OPERATING FREE-AIR TEMPERATURE

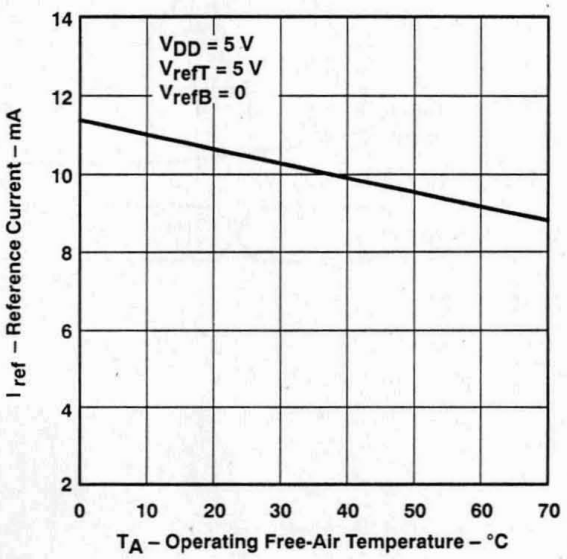


Figure 3

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION
vs
OPERATING FREE-AIR TEMPERATURE

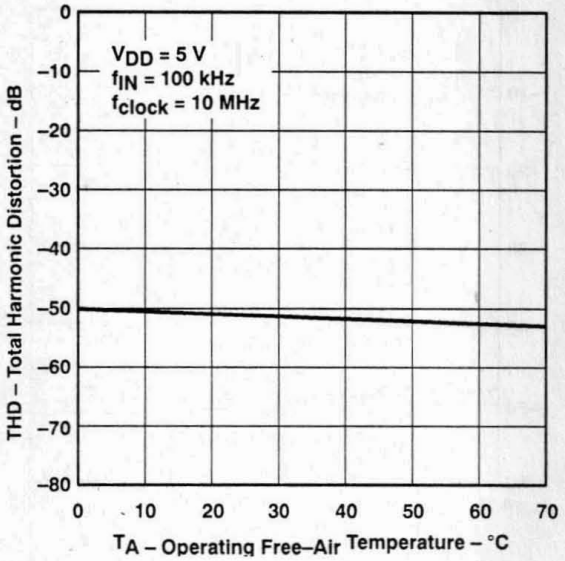


Figure 4

TOTAL HARMONIC DISTORTION
vs
OPERATING FREE-AIR TEMPERATURE

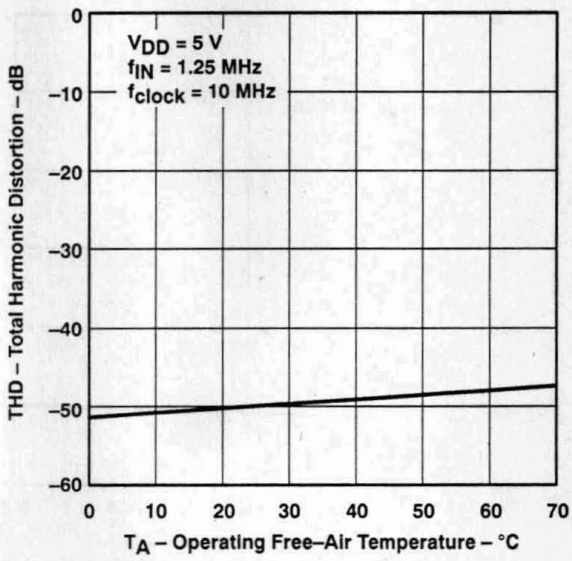


Figure 5

DIFFERENTIAL LINEARITY ERROR
vs
SUPPLY VOLTAGE

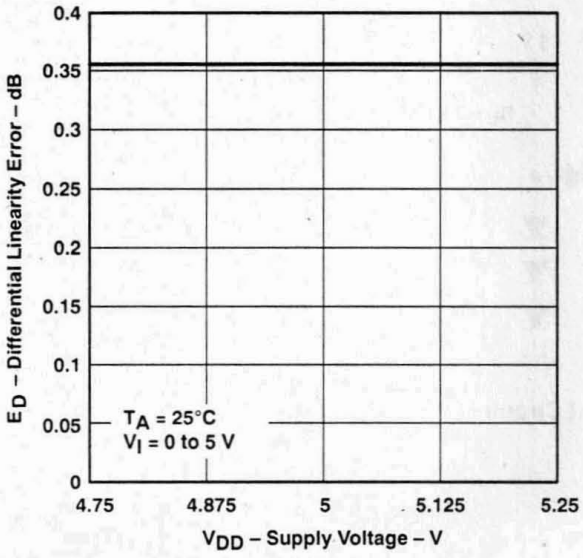


Figure 6

DIFFERENTIAL LINEARITY ERROR
vs
OPERATING FREE-AIR TEMPERATURE

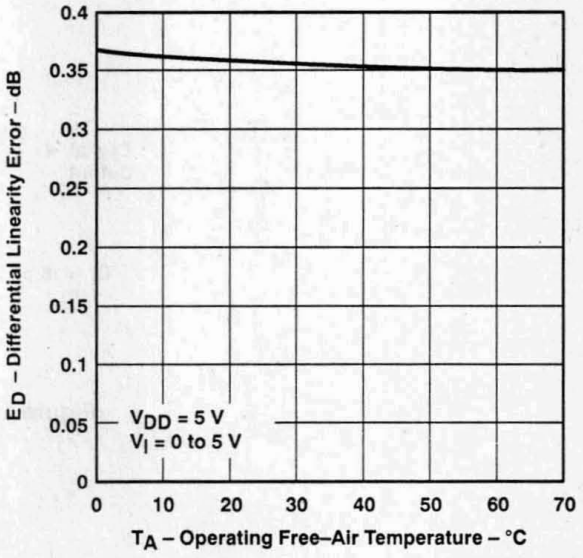


Figure 7

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION
vs
SUPPLY VOLTAGE

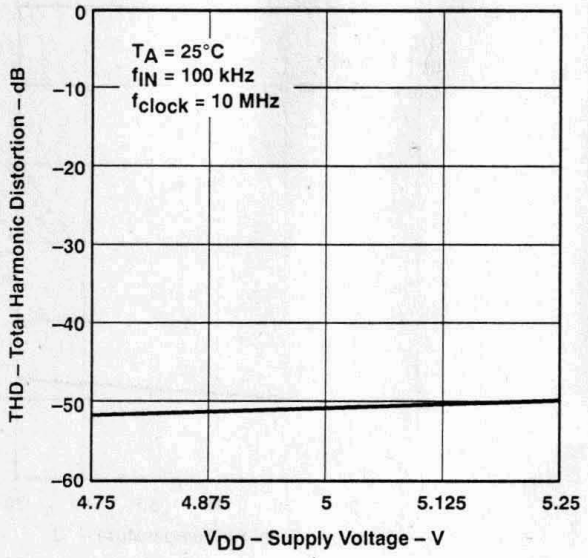


Figure 8

TOTAL HARMONIC DISTORTION
vs
SUPPLY VOLTAGE

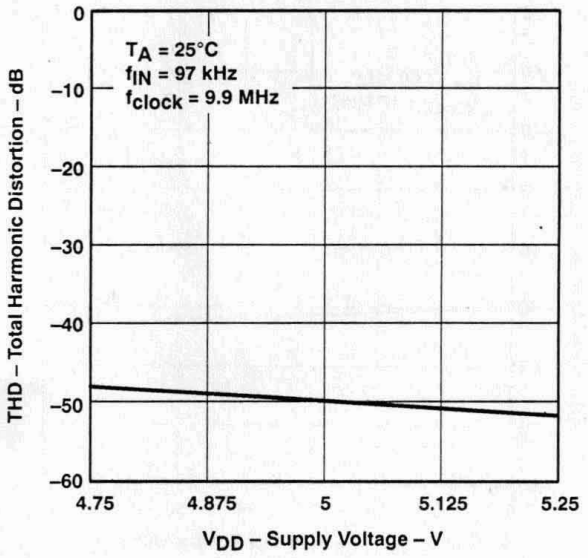


Figure 9

PARAMETER MEASUREMENT INFORMATION

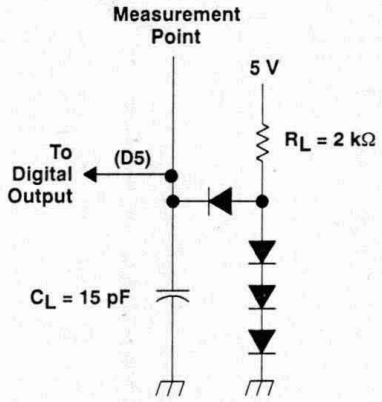


Figure 10. Load Circuit

APPLICATIONS INFORMATION

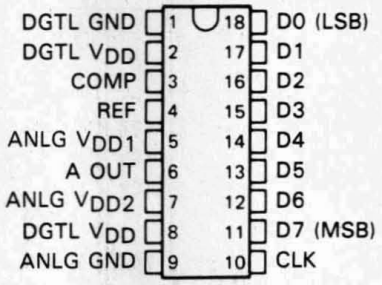
The following design recommendations will benefit the TLC5503-5 user:

1. External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
2. RF breadboarding or PCB techniques should be used throughout the evaluation and production process. Breadboards should be copper clad for bench evaluation.
3. Since the ANLG GND, DGTL GND1, and DGTL GND2 are not connected internally, these pins need to be connected externally. With breadboards, these ground lines should be connected through separate leads with proper supply bypassing. A good method to use is separate twisted-pair cables for the supply lines to minimize noise pickup. An analog and digital ground plane should be used on PCB layouts.
4. Since the ANLG V_{DD}, DGTL $V_{DD}1$, and DGTL $V_{DD}2$ are not connected internally, these pins also need to be connected externally. To connect ANLG V_{DD}, DGTL $V_{DD}1$, and DGTL $V_{DD}2$, a 50-Ω resistor should be placed in series with the DGTL $V_{DD}1$ pin and then a 0.1-μF capacitor to ground before being connected to the ANLG V_{DD} and DGTL $V_{DD}2$ supply.
5. ANLG V_{DD} to ANLG GND, DGTL $V_{DD}1$ to DGTL GND1, and DGTL $V_{DD}2$ to DGTL GND2 should be decoupled with 1-μF and 0.01-μF capacitors, respectively, as close as possible to the appropriate device pins. A ceramic chip capacitor is recommended for the 0.01-μF capacitor. Care should be exercised to assure a solid noise free ground connection for the analog and digital grounds.
6. The no connection (NC) pins on the small-outline package should be connected to ground.
7. ANLG V_{DD}, ANLG GND, and the ANLG INPUT pins should be shielded from the higher-frequency pins, CLK and D0-D7. If possible, ANLG GND traces should be placed on both sides of the ANLG INPUT traces on the PCB.
8. In testing or application of the device, the resistance of the driving source connected to the analog input should be 10 Ω or less within the analog frequency range of interest.

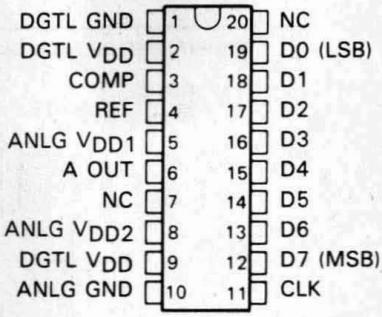
D3224, FEBRUARY 1989—REVISED JANUARY 1990

- 8-Bit Resolution
- ±0.2% Linearity
- Maximum Conversion Rate
  - 30 MHz Typ
  - 20 MHz Min
- Analog Output Voltage Range of V_{DD} to V_{DD} – 1 V
- TTL Digital Input Voltage
- 5-V Single Power Supply Operation
- Low Power Consumption
  - 80 mW Typical
- Interchangeable with Fujitsu MB40778

N PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



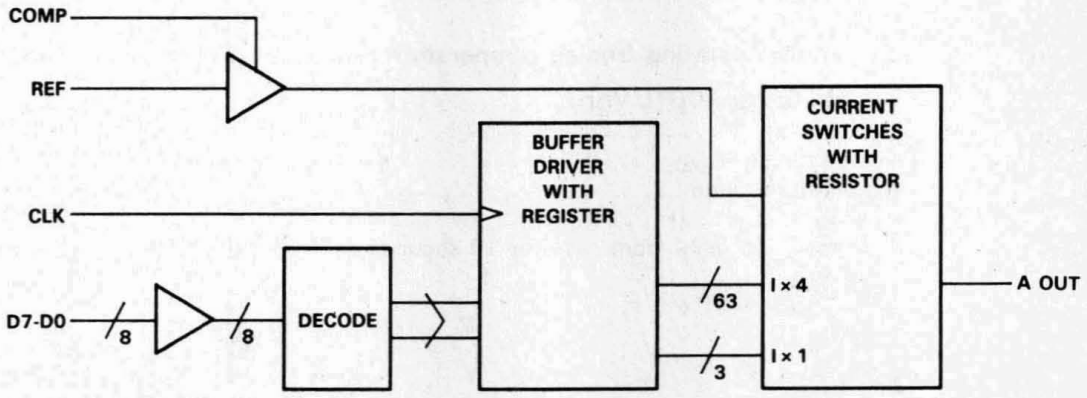
NC—No internal connection

description

The TLC5602 and TLC5602A are low-power ultra-high speed video digital-to-analog converters that use the LinEPIC™ 1-μm CMOS process. The TLC5602 and TLC5602A convert digital signals to analog signals at a sampling rate of dc to 20 MHz. Because of high-speed operation, the TLC5602 and TLC5602A are suitable for digital video applications such as digital television, video processing with a computer, and radar-signal processing.

The TLC5602 and TLC5602A are characterized for operation from 0°C to 70°C.

functional block diagram



During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

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PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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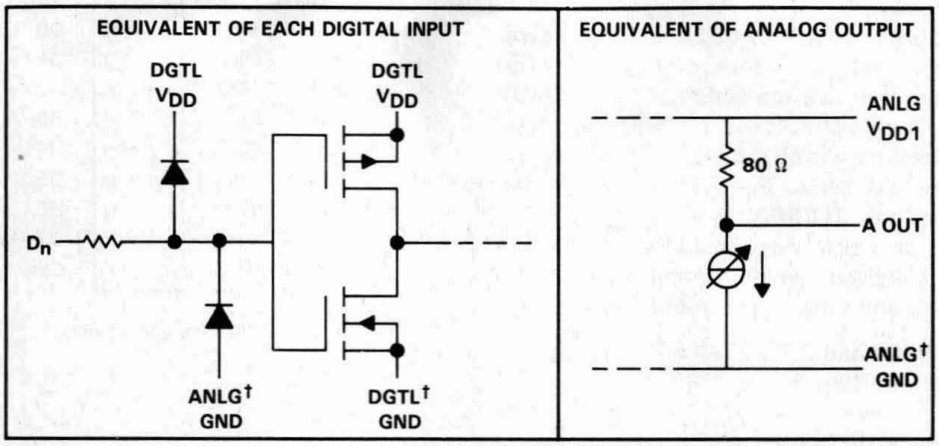
FUNCTION TABLE

STEP	DIGITAL INPUTS								OUTPUT VOLTAGE†
	D7	D6	D5	D4	D3	D2	D1	D0	
0	L	L	L	L	L	L	L	L	3.980 V
1	L	L	L	L	L	L	L	H	3.984 V
⋮					⋮				⋮
127	L	H	H	H	H	H	H	H	4.488 V
128	H	L	L	L	L	L	L	L	4.492 V
129	H	L	L	L	L	L	L	H	4.496 V
⋮					⋮				⋮
254	H	H	H	H	H	H	H	L	4.996 V
255	H	H	H	H	H	H	H	H	5.000 V

†For V_{DD} = 5 V, V_{ref} = 4.050 V.

schematic of digital input and analog output



†ANLG GND and DGTL GND are not connected internally and should be tied together as close to the device pins as possible.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, ANLG V_{DD}, DGTL V_{DD} . . . . . −0.5 V to 7 V
Digital input voltage range, V_I . . . . . −0.5 V to 7 V
Analog reference voltage range, V_{ref} . . . . . V_{DD} − 1.7 V to V_{DD} + 0.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.75	5	5.25	V
Analog reference voltage, V_{ref}		3.8	4	4.2	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Pulse duration, CLK high or low, t_w		25			ns
Setup time, data before CLK↑, t_{su}		16.5			ns
Hold time, data after CLK↑, t_h	TLC5602	12.5			ns
	TLC5602A	4.5			
Phase compensation capacitance, C_{comp} (see Note 1)		1			μF
Operating free-air temperature, T_A		0		70	°C

NOTE 1: The phase compensation capacitor should be connected between COMP and ANLG GND.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{IH}	High-level input current	Digital inputs	V_I = 5 V			±1	μA
I_{IL}	Low-level input current		V_I = 0 V			±1	μA
I_{ref}	Input reference current		V_{ref} = 4 V			10	μA
V_{FS}	Full-scale analog output voltage		V_{DD} = 5 V, V_{ref} = 4.05 V	$V_{DD}-15$	V_{DD}	$V_{DD}+15$	mV
V_{ZS}	Zero-scale analog output voltage			3.919	3.98	4.042	V
r_o	Output resistance		T_A = 25°C	60	80	100	Ω
C_i	Input capacitance		f_{clock} = 1 MHz, T_A = 25°C		15		pF
I_{DD}	Supply current		f_{clock} = 20 MHz, V_{ref} = V_{DD} − 0.95 V		16	25	mA

operating characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
E_L	Linearity error, best straight line				±0.2%	
E_L	Linearity error, end point			±0.15%		
E_D	Linearity error, differential				±0.2%	
G_{diff}	Differential gain	NTSC 40 IRE modulated ramp, f_{clock} = 14.3 MHz		0.7%		
ϕ_{diff}	Differential phase			0.4°		
t_{pd}	Propagation delay, CLK to analog output	C_L = 10 pF		25		ns
t_s	Settling time to within ½LSB	C_L = 10 pF		30		ns

†All typical values are at V_{DD} = 5 V and T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

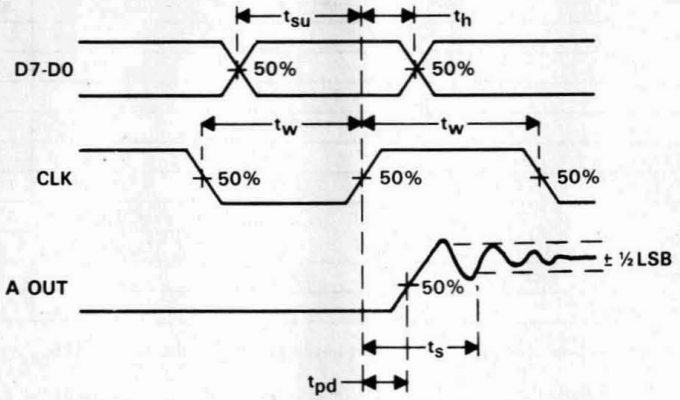


FIGURE 1. VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS

IDEAL CONVERSION CHARACTERISTICS

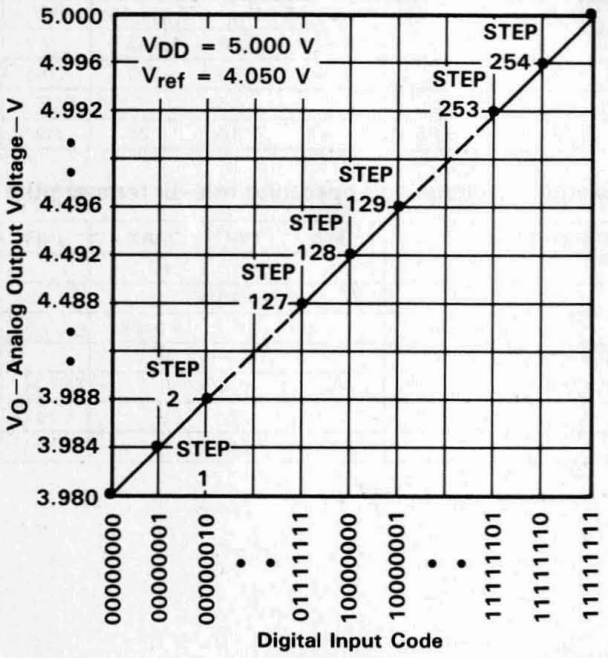


FIGURE 2

BEST-STRAIGHT-LINE LINEARITY ERROR

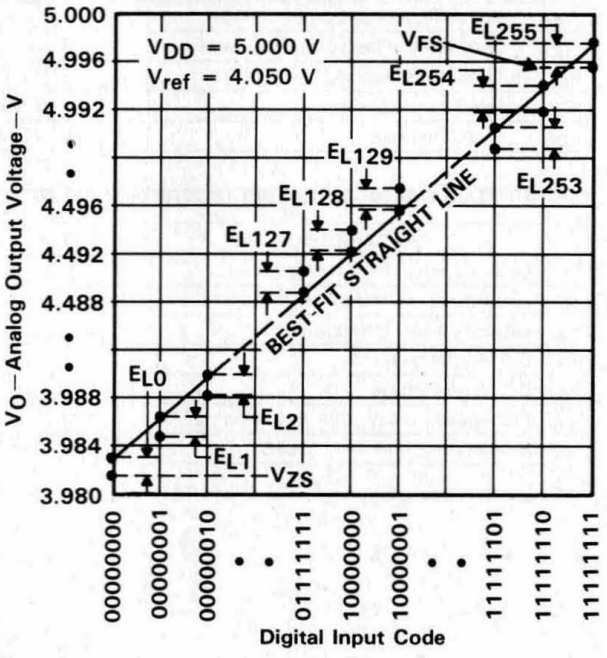


FIGURE 3

TYPICAL CHARACTERISTICS

ZERO-SCALE OUTPUT VOLTAGE
vs
TEMPERATURE

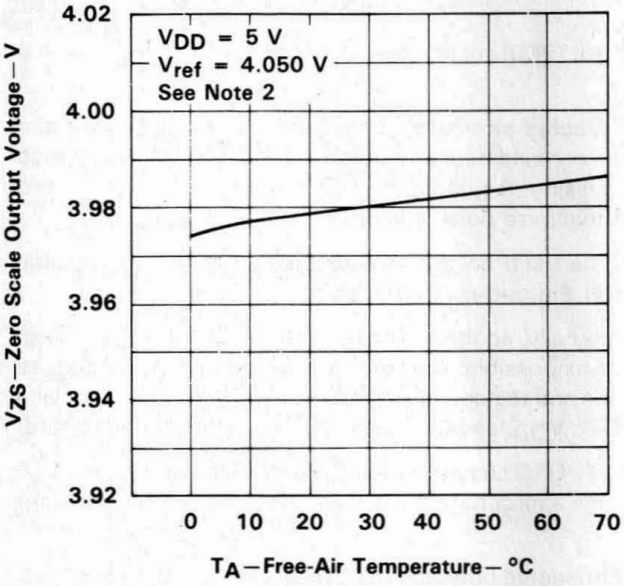


FIGURE 4

OUTPUT RESISTANCE
vs
TEMPERATURE

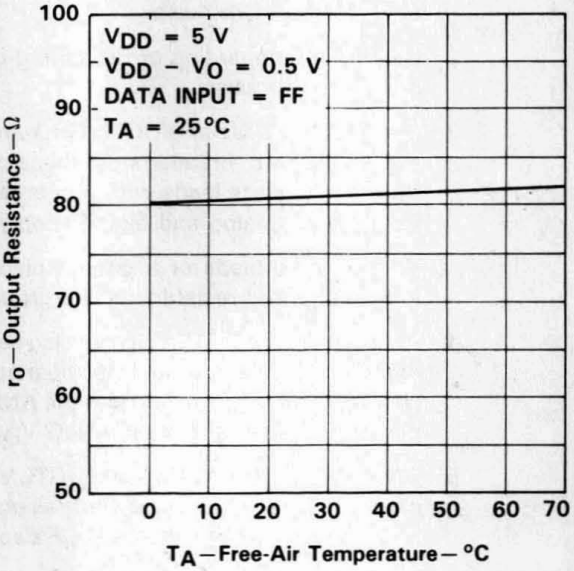


FIGURE 5

SUPPLY CURRENT
vs
TEMPERATURE

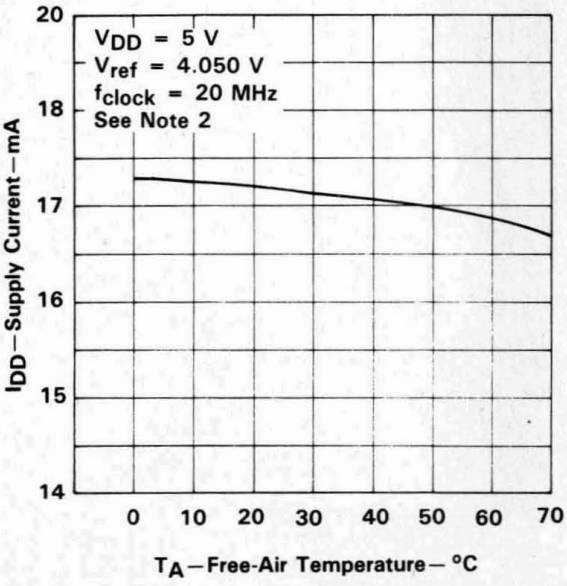


FIGURE 6

ZERO-SCALE OUTPUT VOLTAGE
vs
REFERENCE VOLTAGE

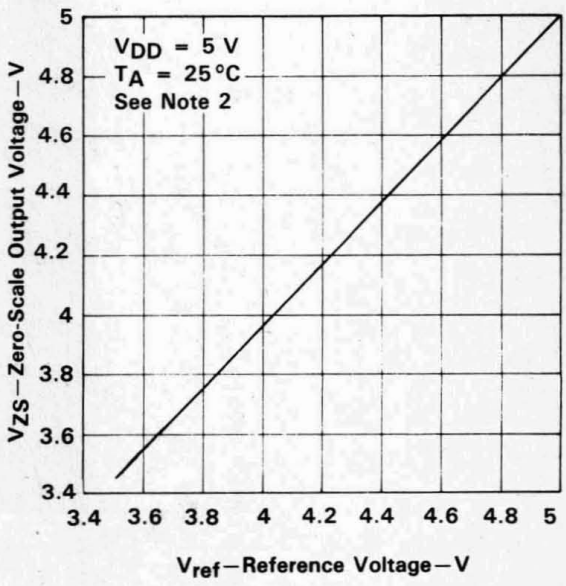


FIGURE 7

NOTE 2. V_{ref} is relative to ANLG GND. V_{DD} is the voltage between ANLG V_{DD} and DGTL V_{DD} tied together and ANLG GND and DGTL GND tied together.

APPLICATION INFORMATION

The following design recommendations will benefit the TLC5602 and TLC5602A user:

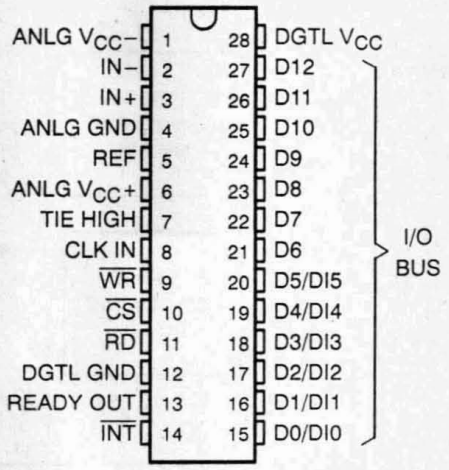
1. External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
2. Use RF breadboarding or RF printed-circuit board (PCB) techniques throughout the evaluation and production process.
3. Since ANLG GND and DGTL GND are not connected internally, these pins need to be connected externally. With breadboards, these ground lines should be connected to the power supply ground through separate leads with proper supply bypassing. A good method is to use a separate twisted pair for the analog and digital supply lines to minimize noise pickup.

   Wide ground leads or a ground plane should be used on the PCB layouts to minimize parasitic inductance and resistance. The ground plane is the better choice for noise reduction.
4. ANLG V_{DD} and DGTL V_{DD} are also separate internally, so they must be connected externally. These external PCB leads should also be made as wide as possible. A ferrite bead or equivalent inductance should be placed in series with the ANLG V_{DD} pin and the decoupling capacitor as close to the device pins as possible before the ANLG V_{DD} and DGTL V_{DD} leads are connected together on the board.
5. ANLG V_{DD} to ANLG GND and DGTL V_{DD} to DGTL GND should be decoupled with a 1-μF and 0.01-μF capacitor, respectively, as close as possible to the appropriate device pins. A ceramic chip capacitor is recommended for the 0.01-μF capacitor.
6. The phase compensation capacitor should be connected between the COMP pin and the ANLG GND pin with as short a lead-in as possible.
7. The no-connection (NC) pins on the small-outline package should be connected to the ANLG GND pin.
8. ANLG V_{DD}, ANLG GND, and the A OUT pins should be shielded from the high-frequency pins, CLK and D0-D7. ANLG GND ground traces should be placed on both sides of the A OUT trace on the PCB.

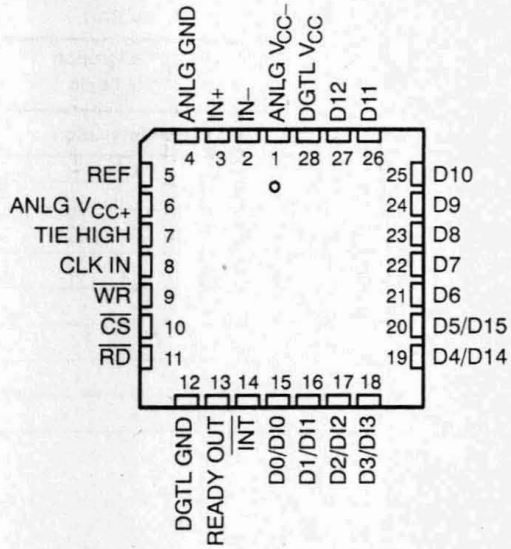
General Information 1
General Purpose ADCs 2
General Purpose DACs 3
Video and High-Speed ADCs and DACs 4
DSP Analog Interface and Conversion 5
Video Interface Palettes 6
Analog Switches 7
Filters 8
Data Manuals 9
Application Reports 10
Mechanical Data 11

- **Advanced LinCMOS™ Technology**
- **Self-Calibration Eliminates Expensive Trimming at Factory and Offset Adjustment in the Field**
- **12-Bit Plus Sign Resolution**
- **11-Bit Linearity**
- **12-μs Conversion Period (clock = 2 MHz)†**
- **Compatible with All Microprocessors**
- **Single 5-V and ±5-V Supply Operation**
- **True Differential Analog Voltage Inputs with $-V_{ref}$ to V_{ref} Differential Input Range**
- **For Single 5-V Supply, Input Common-Mode Voltage Range is 0 V to 5 V**
- **For ±5-V Supplies, Input Common-Mode Voltage Range is –5 V to 5 V**
- **Unipolar or Bipolar Operation**
- **2s Complement Output**
- **Low Power . . . 85 mW Maximum**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The TLC1125 converter is manufactured with Texas Instruments highly efficient Advanced LinCMOS™ technology. The TLC1125 CMOS analog-to-digital converter can be operated with a single 5-V supply or with ±5-V supplies. The differential input range is $-V_{ref}$ to V_{ref} in both supply configurations. The common-mode input range is ANLG V_{CC-} to ANLG V_{CC+}. For single 5-V supply operation, grounding IN– corresponds to standard unipolar conversion. For ±5-V supply operation, grounding IN– corresponds to standard bipolar conversion. Conversion is performed via the successive-approximation method. The TLC1125 outputs the converted data in a parallel word and interfaces directly to a 16-bit data bus. Negative numbers are given in the two's complement data format. All digital signals are fully TTL and CMOS compatible.

This converter uses a self-calibration technique by which seven of the internal capacitors in the capacitive array of the A/D conversion circuitry can be automatically calibrated. The internal capacitors are calibrated during a nonconversion capacitor-calibrate cycle in which all seven of the internal capacitors are calibrated at the same time. A conversion requires only 24 clock cycles. Self-calibration requires 300 clock cycles. The calibration or conversion cycle may be initiated at any time by issuing the proper command word to the data bus. The self-calibrating technique eliminates the need for expensive trimming of thin-film resistors at the factory and provides excellent performance at low cost.

The TLC1125I is characterized for operation from –40°C to 85°C.

† The conversion period is the reciprocal of the conversion rate and includes the access, sample, setup, and A/D conversion times.
Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

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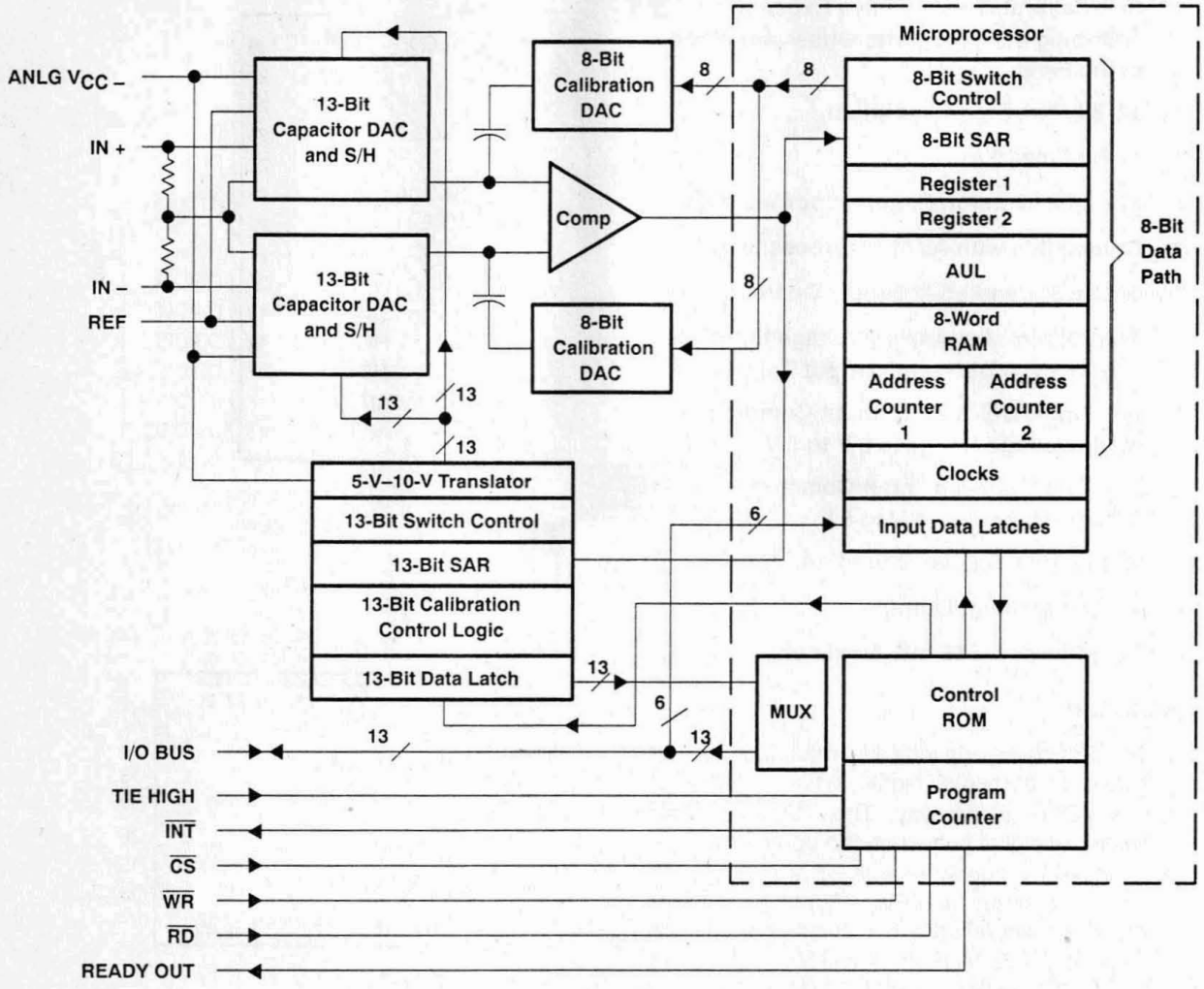
functional block diagram



operation description

calibration of comparator offset

The following actions are performed to calibrate the comparator offset:

1) The IN+ and IN– inputs are internally shorted together so that the converter input is zero. A course comparator offset calibration is performed by storing the offset voltages of the interconnecting comparator stages on the coupling capacitors that connect these stages. Refer to Figure 1. The storage of offset voltages is accomplished by closing all switches and then opening switches A and A', then switches B and B', and then C and C'. This process continues until all interconnecting stages of the comparator are calibrated. After this action, some of the comparator offset still remains uncalibrated.

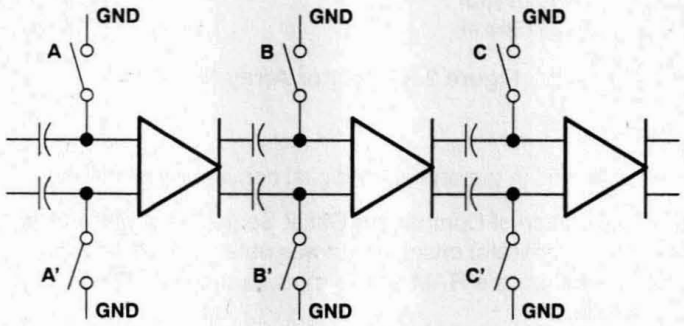


Figure 1. Comparator Offset Null

2) An A/D conversion is done on the remaining offset with the 8-bit calibration DACs and 8-bit SAR and the result is stored in the RAM.

calibration of the ADC's capacitive capacitor array

The following actions are performed to calibrate capacitors in the 13-bit DACs that comprise the ADC's capacitive array:

1) The IN+ and IN– inputs are internally disconnected from the 13-bit DACs.
2) The most significant bit (MSB) capacitor is tied to REF, while the rest of the array capacitors are tied to GND. The A/D conversion result for the remaining comparator offset, obtained in Step 2 above, is retrieved from the RAM and is input to the 8-bit DACs.
3) Step 1 of the Calibration of Comparator Offset sequence is performed. The 8-bit DAC input is returned to zero and the remaining comparator offset is then subtracted. Thus, the comparator offset is completely corrected.
4) Now the MSB capacitor is tied to GND, while the rest of the array capacitors, C_x, are tied to REF. An MSB capacitor voltage error (see Figure 2) on the comparator output will occur if the MSB capacitor does not equal the sum of the other capacitors in the capacitive array. This error voltage is converted to an 8-bit word from which a capacitor error is computed and stored in the RAM.
5) The capacitor voltage error for the next most significant capacitor is calibrated by keeping the MSB capacitor grounded and then performing the above Steps 1-4 while using the next most significant capacitor in lieu of the MSB capacitor. The seven most significant capacitors are calibrated in this manner.

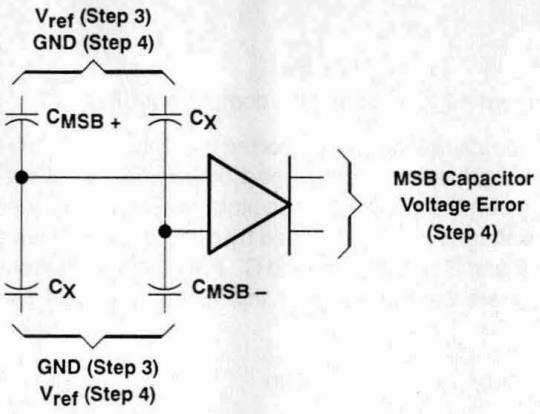


Figure 2. Capacitor Array Null

analog-to-digital conversion

The following steps are performed in the analog-to-digital conversion process:

1) Step 1 of the Calibration of Comparator Offset Sequence is performed. The A/D conversion result for the remaining comparator offset, which was obtained in Step 2 of the Calibration of Comparator Offset, is retrieved from the RAM and is input to the 8-bit DACs. Thus the comparator offset is completely corrected.
2) IN+ and IN– are sampled into the 13-bit capacitive arrays.
3) The 13-bit analog-to-digital conversion is performed. As the successive-approximation conversion proceeds successively through the seven most significant capacitors, the error for each of these capacitors is recovered from the RAM and accumulated in a register. This register controls the 8-bit DACs so the total accumulated error for these capacitors is subtracted out during the conversion process.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (ANLG V_{CC+} AND DGTL V_{CC}) (see Note 1) ..... 7.5 V
Supply voltage, ANLG V_{CC-} ..... –7.5 V
Control and Clock input voltage range ..... –0.3 V to DGTL V_{CC} +0.3 V
Analog input (IN+, IN–) voltage range, V_{I+} and V_{I-} ..... ANLG V_{CC-} –0.3 V to ANLG V_{CC+} +0.3 V
Reference voltage range, V_{ref} ..... –0.3 V to ANLG V_{CC+} +0.3 V
Pin 7 voltage range ..... –0.3 V to ANLG V_{CC+} +0.3 V
Output voltage range ..... –0.3 V to DGTL V_{CC} +0.3 V
Input current (per pin) ..... ±5 mA
Input current (per package) ..... ±20 mA
Operating free-air temperature range, T_A ..... –40°C to 85°C
Storage temperature range ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds ..... 260°C

NOTE 1: All analog voltages are referred to ANLG GND and all digital voltages are referred to DGTL GND.

recommended operating conditions

			MIN	MAX	UNIT
Supply voltage		ANLG V_{CC+}	4.5	6	V
		ANLG V_{CC-}	−5.5	ANLG GND	
		DGTL V_{CC}	4.5	6	
High-level input voltage, V_{IH} (V_{CC} = 4.75 V to 5.25 V)	All digital inputs except CLK IN		2		V
	CLK IN		3.5		
Low-level input voltage, V_{IL} (V_{CC} = 4.75 V to 5.25 V)	All digital inputs except CLK IN			0.8	V
	CLK IN			1.4	
Analog input voltage, V_{I+}, V_{I-}			ANLG V_{CC-} − 0.05	ANLG V_{CC+} 0.05	V
Pin 7 (TIE HIGH)			2		V
Clock input frequency, f_{clock}			0.3	2	MHz
Clock duty cycle			40%	60%	
Pulse duration, $\overline{CS}$ and $\overline{WR}$ low, t_w			15		ns
Setup time before $\overline{WR}\uparrow$ or $\overline{CS}\uparrow$, t_{su}			60		ns
Hold time after $\overline{WR}\uparrow$ or $\overline{CS}\uparrow$, t_h			50		ns
Operating free-air temperature, T_A			−40	85	°C

electrical characteristics over recommended operating free-air temperature range, ANLG V_{CC+} = DGTL V_{CC} = V_{ref} = 5 V, ANLG V_{CC-} = −5 V or ANLG GND (unless otherwise noted) (see Note 2)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	DGTL V_{CC} = 4.75 V	I_O = −1.8 mA	2.4		V
			I_O = −50 μA	4.5		
V_{OL}	Low-level output voltage	DGTL V_{CC} = 4.75 V,	I_O = 3.2 mA		0.4	V
r_{ref}	Input resistance, REF terminal			1	10	MΩ
I_{IH}	High-level input current	V_I = 5 V			5	μA
I_{IL}	Low-level input current	V_I = 0			−5	μA
I_{OZ}	High-impedance-state output leakage current	V_O = 0			−3	μA
		V_O = 5 V			3	
I_O	Output current	V_O = 0		−6		mA
		V_O = 5 V		8		
DGTL I_{CC}	Supply current from DGTL V_{CC}	f_{clock} = 2 MHz,	$\overline{CS}$ high		6	mA
ANLG I_{CC+}	Supply current from ANLG V_{CC+}	f_{clock} = 2 MHz,	$\overline{CS}$ high		9	mA
ANLG I_{CC-}	Supply current from ANLG V_{CC-}	f_{clock} = 2 MHz,	$\overline{CS}$ high		−3	mA

NOTE 2: The input voltage range is defined as: V_{I+} = −5.05 V to 5.05 V, V_{I-} = −5.05 V to 5.05 V, and $|V_{I+} - V_{I-}| \leq 5.05$ V when ANLG V_{CC-} = −5 V. The input voltage range is defined as: V_{I+} = −0.05 V to 5.05 V, V_{I-} = −0.05 V to 5.05 V, and $|V_{I+} - V_{I-}| \leq 5.05$ V when ANLG V_{CC-} = ANLG GND.

electrical characteristics over recommended operating free-air temperature range, ANLG V_{CC+} = DGTL V_{CC} = V_{ref} = 5 V, ANLG V_{CC-} = −5 V or ANLG GND, f_{clock} = 2 MHz (unless otherwise noted) (see Note 2)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
E_L	Integral linearity error					±0.024%	FSR‡
E_D	Differential linearity		−5 V < (IN+ − IN−) < 5 V, V_{CC+} = 5 V, V_{CC-} = −5 V	>−1		2	LSB‡§
			0 < (IN+ − IN−) < 5.05 V, V_{CC+} = 5 V, V_{CC-} = 0	>−1		2	
	Zero error					±1.5	LSB‡
	Unadjusted positive and negative full-scale error					±2	LSB‡
	Temperature coefficient of gain				15		ppm/°C
	Temperature coefficient of offset point				1.5		ppm/°C
k_{SVS}	Supply voltage sensitivity	Zero error	ANLG V_{CC+} = 5 V ±5%, ANLG V_{CC-} = −5 V ±5%, DGTL V_{CC} = 5 V ±5%		±0.75		LSB‡§
		Positive and negative full-scale error			±0.75		
		Linearity error			±0.25		
CMRR	Common-mode rejection ratio		IN− = IN+ = −5 V to 5 V		65		dB
	Common-mode rejection (maximum code change from code 0000000000000)		IN− = IN+ = −5 V to 5 V		4		LSB‡
t_{period}	Conversion period ($1/f_{clk}$) (see Note 3)					24	clock cycles
t_a	Access time (delay from falling edge of $\overline{CS} \cdot \overline{RD}$ to data output)		C_L = 100 pF			95	ns
t_{dis}	Disable time, output (delay from rising edge of $\overline{RD}$ to high-impedance state)		R_L = 2 kΩ, C_L = 100 pF			90	ns
$t_{d1(READY)}$	Control signal edge to READY OUT delay time			100			ns
$t_{d2(READY)}$	Control signal edge to READY OUT delay time					100	ns
$t_{d(INT)}$	$\overline{RD}$ or $\overline{WR}$ to reset of $\overline{INT}$ delay time					100	ns

† All typical values are at T_A = 25°C.

‡ FSR is Full-Scale Range: 0.024% FSR linearity error is equivalent to 11-bits of linearity with 1 LSB = 1.22 mV defined for 12 bits.

§ No missing codes.

NOTES: 2. The input voltage range is defined as: V_{I+} = −5.05 V to 5.05 V, V_{I-} = −5.05 V to 5.05 V, and $|V_{I+} - V_{I-}| \leq 5.05$ V when ANLG V_{CC-} = −5 V. The input voltage range is defined as: V_{I+} = −0.05 V to 5.05 V, V_{I-} = −0.05 V to 5.05 V, and $|V_{I+} - V_{I-}| \leq 5.05$ V when ANLG V_{CC-} = ANLG GND.

3. In practical use of the device, if $\overline{INT}$ and $\overline{RD}$ go low within the same f_{clock} period, $\overline{INT}$ will not be reset until $\overline{WR}$ is brought low. If $\overline{INT}$ and $\overline{RD}$ do not go low within the same f_{clock} period, $\overline{INT}$ will be reset.

PARAMETER MEASUREMENT INFORMATION

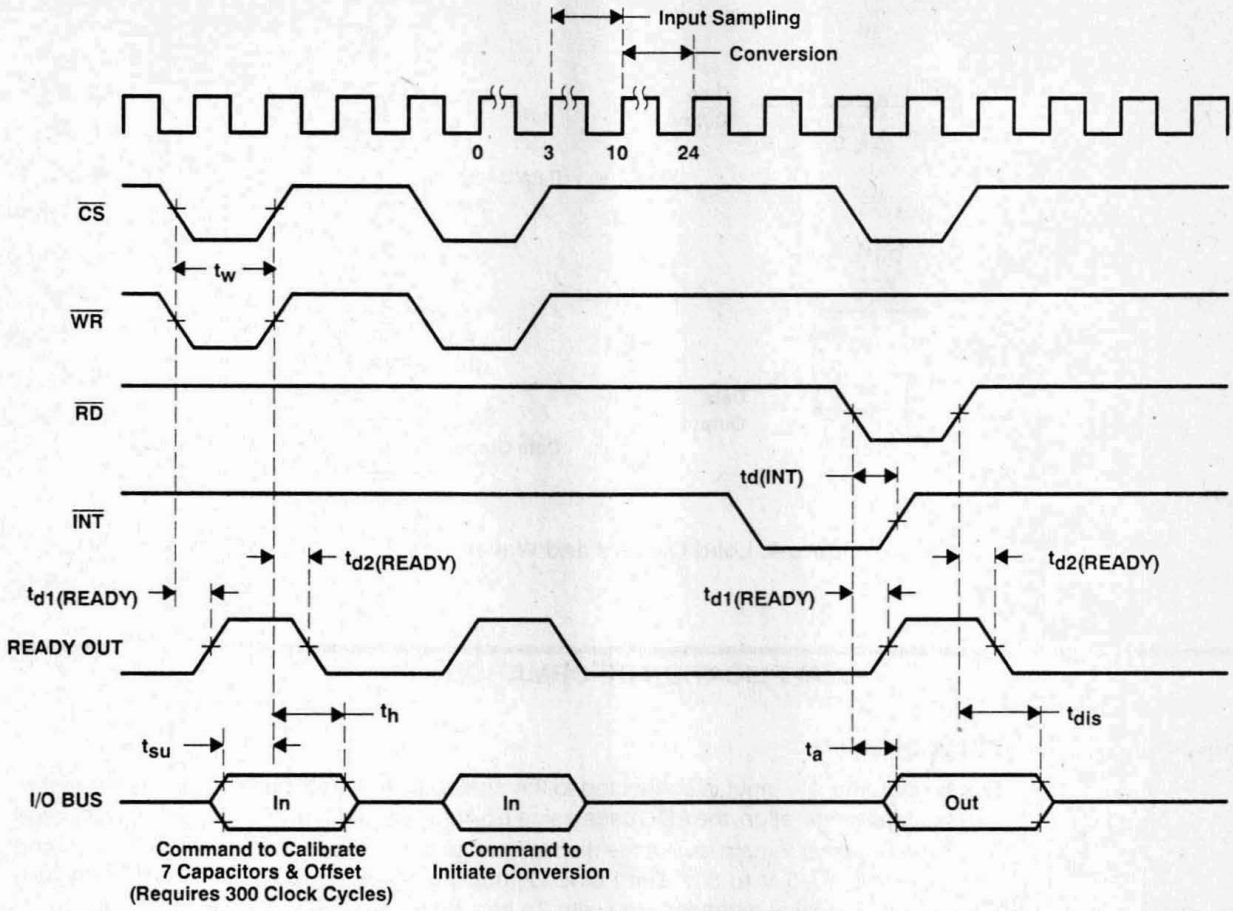


Figure 3. Timing Diagram

PARAMETER MEASUREMENT INFORMATION

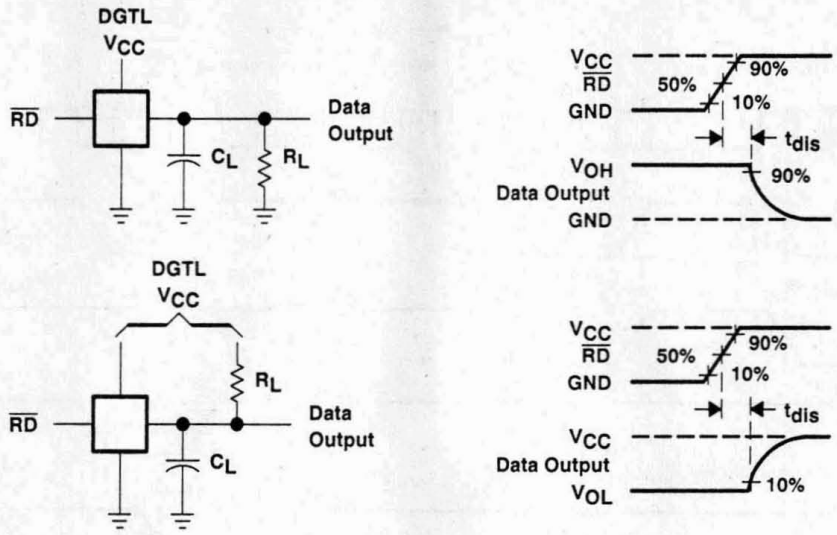


Figure 4. Load Circuits and Waveforms

APPLICATION INFORMATION

unipolar and bipolar operation

For single-ended signal input, the IN+ input is connected to the analog source and the IN– input is connected to ANLG GND. In the unipolar configuration, the ADC uses a single 5-V supply and the analog input voltage range is 0 V to 5 V. Data bit D12 will always remain low. In the bipolar configuration, the ADC uses ±5-V supplies and the analog input voltage range is –5 V to 5 V. Data bit D12 indicates the sign of the input signal. In both configurations, the 13-bit data format is extended sign with 2's complement, right justified data.

power-up sequence

Calibration is not automatic on power-up. Calibration is initiated by writing control words to the six least significant bits of the data bus. V_{ref} must have fully settled before calibration is initiated. If addressed or initiated, conversion can begin after the first clock cycle. However, full A/D conversion accuracy is not established until after internal capacitor calibration.

conversion start sequence

The writing of the conversion command word to the six least significant bits of the data bus, when either $\overline{CS}$ or $\overline{WR}$ goes high, initiates the conversion sequence.

analog sampling sequence

Sampling of the input signal occurs during clock cycles 3 thru 10 of the conversion sequence.

completed A/D conversion

When $\overline{INT}$ goes low, conversion is complete and the A/D result can be read. A new conversion can begin immediately. The A/D conversion is complete at the end of clock cycle 24 of the conversion sequence.

aborting a conversion in process and beginning a new conversion

If a conversion is initiated while a conversion sequence is in process, the ongoing conversion will be aborted and a new conversion sequence will begin.

reading the conversion result

When both $\overline{CS}$ and $\overline{RD}$ go low, all 13 bits of conversion data are output to the I/O bus. The format of the output is extended sign with 2's complement, right justified data. The sign bit D12 is low if $V_{I+} - V_{I-}$ is positive and high if $V_{I+} - V_{I-}$ is negative.

general

reset INT

When reading the conversion data, the falling edge of the first low-going combination of $\overline{CS}$ and $\overline{RD}$ will reset $\overline{INT}$. The falling edge of the low-going combination of $\overline{CS}$ and $\overline{WR}$ will also reset $\overline{INT}$.

ready out

For high-speed microprocessors, READY OUT allows the TLC1125 to insert a wait state in the microprocessor's read or write cycle.

reference voltage (V_{ref})

This voltage defines the range for $|V_{I+} - V_{I-}|$. When $|V_{I+} - V_{I-}|$ equals V_{ref}, the highest conversion data value results. When $|V_{I+} - V_{I-}|$ equals 0, the conversion data value is zero. Thus, for a given input, the conversion data changes ratiometrically with changes in V_{ref}. Calibration should be performed with the same value of V_{ref} as will be used during conversion.

TIE HIGH

This pin is a digital input and should be tied high.

calibration and conversion considerations

Calibration of the internal capacitors and A/D conversion are two separate actions. Each action is independently initiated. A calibration command should be initiated prior to subsequent conversions. It is not necessary to recalibrate before each conversion. Capacitor calibration is expected to last indefinitely as long as the clock signal and power are not interrupted. However, the offset calibration may drift with temperature changes. The temperature coefficient of the offset point is shown in the electrical characteristics table. We recommend periodic calibration at the user's convenience. Calibration and conversion commands require 300 and 24 clock cycles, respectively.

The calibrate and conversion commands are initiated by writing control words on the six least significant bits of the data bus. These control words are written into the IC when either $\overline{CS}$ or $\overline{WR}$ goes high. The initiation of these commands is illustrated in the Timing Diagram. The bit patterns for the commands are shown in Table 1.

Table 1. Conversion Commands

COMMAND	$\overline{CS} + \overline{WR}$	I/O BUS						REQUIRED NUMBER OF CLOCK CYCLES
		DI5	DI4	DI3	DI2	DI1	DI0	
Conversion	↑	H	L	X	X	X	L	24
Calibrate†	↑	L	X	L	L	L	L	300

† Calibration is lost when clock is stopped.

analog inputs

differential inputs provide common-mode rejection

The differential inputs reduce common-mode noise. Common-mode noise is noise common to both IN+ and IN− inputs, such as 60-Hz noise. There is no time interval between the sampling of the IN+ and IN− so these inputs are truly differential. Thus, no conversion errors result from a time interval between the sampling of the IN+ and IN− inputs.

input bypass capacitors

Input bypass capacitors may be used for noise filtering. However, the charge on these bypass capacitors will be depleted during the input sampling sequence when the internal sampling capacitors are charged. Note that the charging of the bypass capacitors through the differential source resistances must keep pace with the charge depletion of the bypass capacitors during the input sampling sequence. Higher source resistances reduce the amount of charging current for the bypass capacitors. Also, note that fast, successive conversion will have the greatest charge depletion effect on the bypass capacitors. Therefore, the above phenomenon becomes more significant as source resistances and the conversion rate (i.e., higher clock frequency and conversion initiation rate) increase.

In addition, if the above phenomenon prevents the bypass capacitors from fully charging between conversions, voltage drops across the source resistances will result due to the ongoing bypass capacitor charging currents. The voltage drops will cause a conversion error. Also, the voltage drops increase with higher $|V_{I+} - V_{I-}|$ values, higher source resistances, and lower charge on the bypass capacitors (i.e., faster conversion rate).

For low-source-resistance applications ($R_{source} < 100\ \Omega$), a 0.001-μF bypass capacitor at the inputs will prevent pickup due to the series lead inductance of a long wire. A 100-Ω resistor can be placed between the capacitor and the output of an operational amplifier to isolate the capacitor from the operational amplifier.

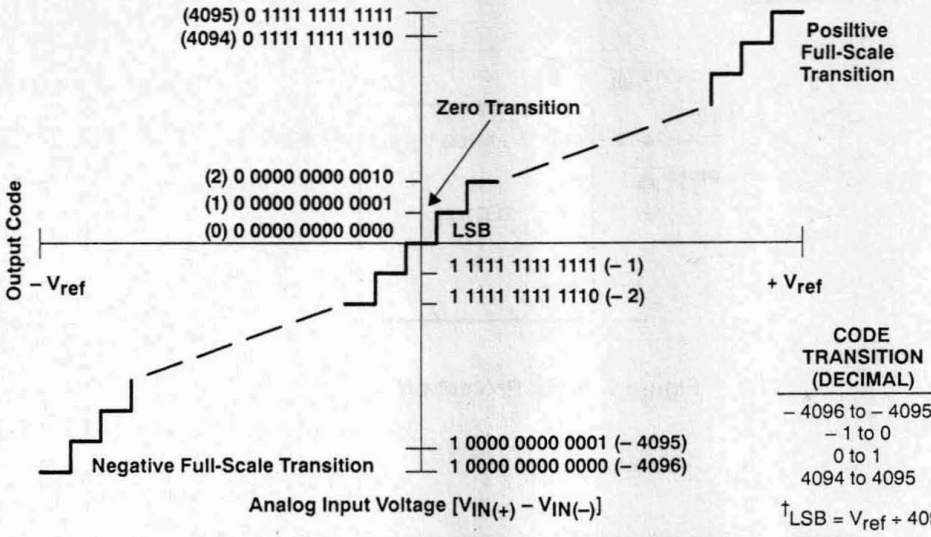
input leads

The input leads should be kept as short as possible, since the coupling of noise and digital clock signals to the the inputs can cause errors.

power supply considerations

Noise spikes on the V_{CC} lines can cause conversion error. Low-inductance tantalum capacitors (> 1 μF) with short leads should be used to bypass ANLG V_{CC} and DGTL V_{CC}. A separate regulator for the TLC1125 and other analog circuitry will greatly reduce digital noise on the supply line.

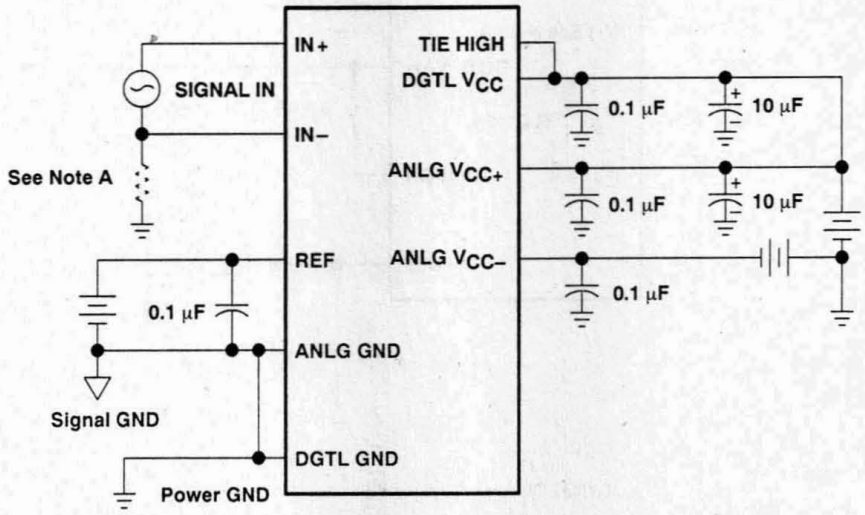
APPLICATION INFORMATION



CODE TRANSITION (DECIMAL)	ANALOG INPUT VOLTAGE (LSB)†
– 4096 to – 4095	– 4095.5
– 1 to 0	– 0.5
0 to 1	0.5
4094 to 4095	4094.5

†LSB = V_{ref} ÷ 4095.5

Figure 5. Transfer Characteristic



NOTES: A. The analog input must have some current return path to ANALOG GND.
B. Bypass capacitor leads must be as short as possible.
C. For high-accuracy applications, use a larger capacitor to reduce reference noise.

Figure 6. Analog Considerations

APPLICATION INFORMATION

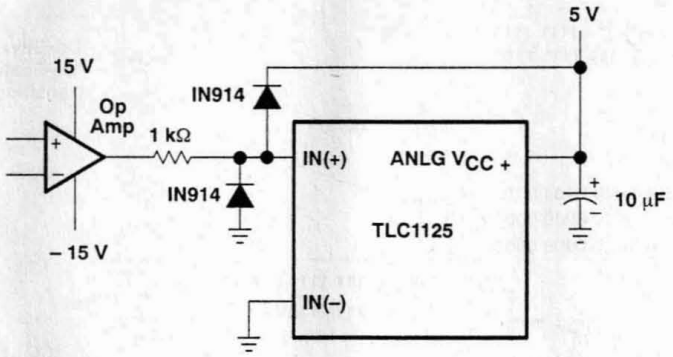
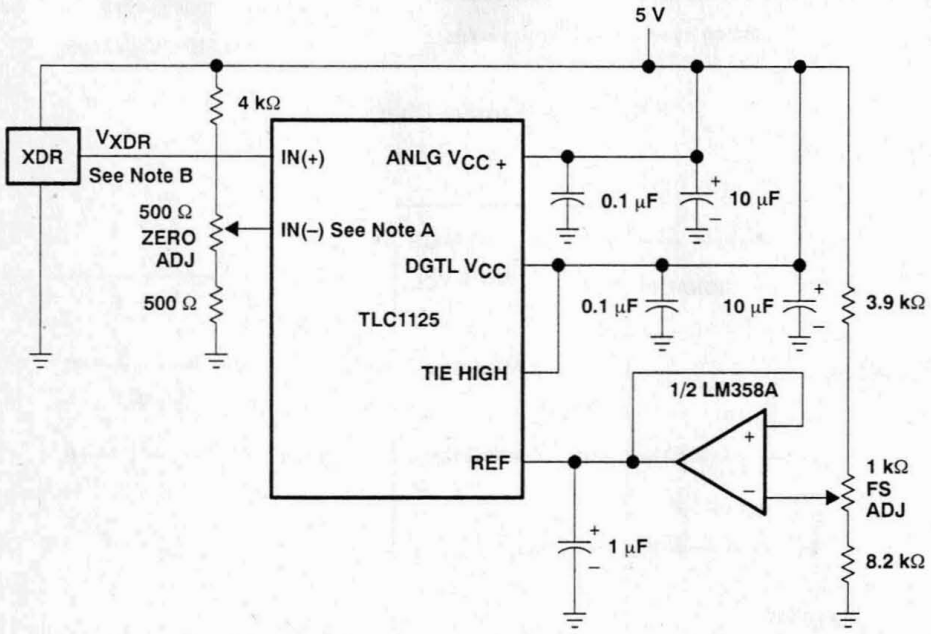


Figure 7. Input Protection

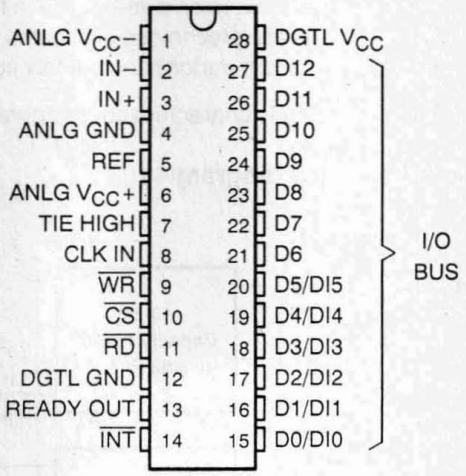


NOTES: A. $V_I = 0.15 \times$ ANLG V_{CC+}.
B. 15% of ANALOG $V_{CC} \le V_{XDR} \le$ 85% of ANALOG V_{CC}.

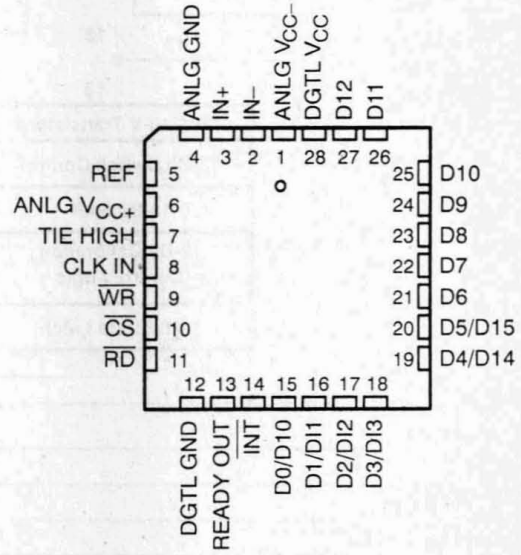
Figure 8. Operating With Ratiometric Transducers

- **Advanced LinCMOS™ Technology**
- **Self-Calibration Eliminates Expensive Trimming at Factory and Offset Adjustment in the Field**
- **12-Bit Plus Sign Resolution**
- **12-Bit Linearity**
- **12-μs Conversion Period at f_{clock} = 2 MHz†**
- **Compatible With All Microprocessors**
- **Single 5-V and ±5-V Supply Operation**
- **True Differential Analog Voltage Inputs With $-V_{ref}$ to V_{ref} Differential Input Range**
- **For Single 5-V Supply, Input Common-Mode Voltage Range is 0 V to 5 V**
- **For ±5-V Supplies, Input Common-Mode Voltage Range is –5 V to 5 V**
- **Unipolar or Bipolar Operation**
- **2s-Complement Output**
- **Low-Power . . . 85 mW Maximum**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The TLC1225 converter is manufactured with Texas Instruments highly efficient Advanced LinCMOS™ technology. The TLC1225 CMOS analog-to-digital converter can be operated with a single 5-V supply or with ±5-V supplies. The differential input range is $-V_{ref}$ to V_{ref} in both supply configurations. The common-mode input range is ANLG V_{CC-} to ANLG V_{CC+}. For single 5-V supply operation, grounding IN– corresponds to standard unipolar conversion. For ±5-V supply operation, grounding IN– corresponds to standard bipolar conversion. Conversion is performed via the successive-approximation method. The TLC1225 outputs the converted data in a parallel word and interfaces directly to a 16-bit data bus. Negative numbers are given in the twos-complement data format. All digital signals are fully TTL and CMOS compatible.

This converter uses a self-calibration technique by which seven of the internal capacitors in the capacitive array of the A/D conversion circuitry can be automatically calibrated. The internal capacitors are calibrated during a nonconversion capacitor-calibrate cycle in which all seven of the internal capacitors are calibrated at the same time. A conversion period requires only 24 clock cycles. Self-calibration requires 300 clock cycles. The

† The conversion period is the reciprocal of the conversion rate and includes the access, sample, setup, and A/D conversion times.
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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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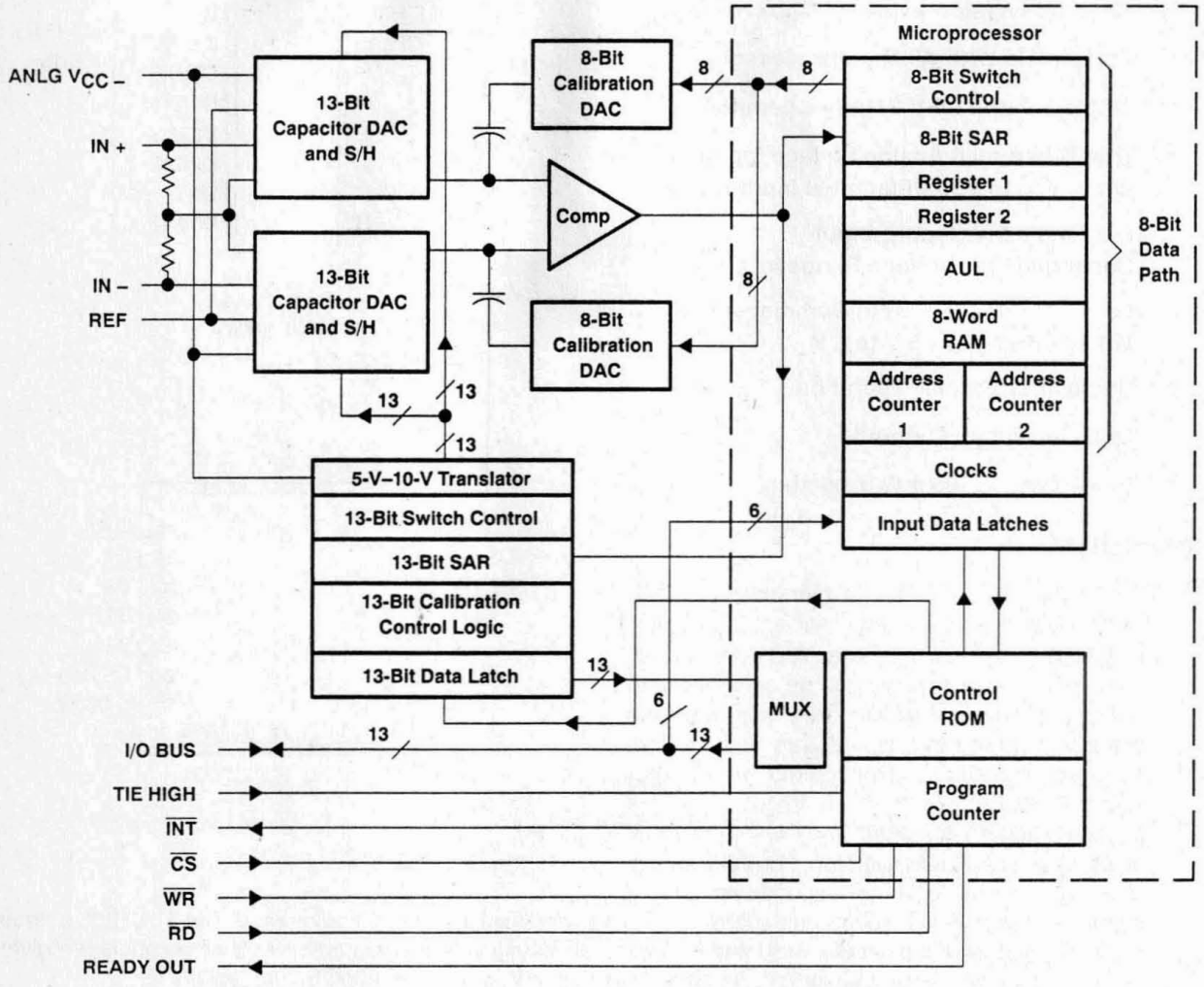
description (continued)

calibration or conversion cycle can be initiated at any time by issuing the proper command word to the data bus. The self-calibrating technique eliminates the need for expensive trimming of thin-film resistors at the factory and provides excellent performance at low cost.

The TLC1225I is characterized for operation from −40°C to 85°C.

functional block diagram



operation description

calibration of comparator offset

The following actions are performed to calibrate the comparator offset:

1) The IN+ and IN– inputs are internally shorted together so that the converter input is zero. A course comparator offset calibration is performed by storing the offset voltages of the interconnecting comparator stages on the coupling capacitors that connect these stages. Refer to Figure 1. The storage of offset voltages is accomplished by closing all switches and then opening switches A and A', then switches B and B', and then C and C'. This process continues until all interconnecting stages of the comparator are calibrated. After this action, some of the comparator offset still remains uncalibrated.

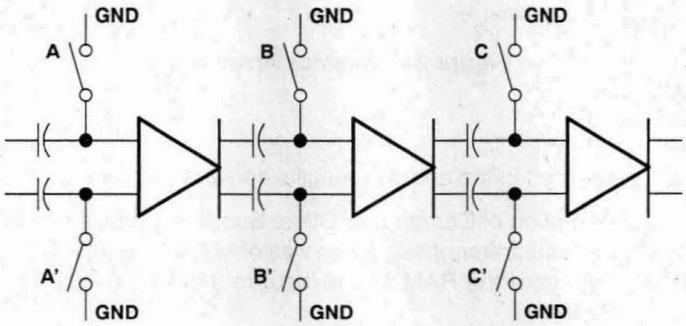


Figure 1. Comparator Offset Null

2) An A/D conversion is done on the remaining offset with the 8-bit calibration DACs and 8-bit SAR, and the result is stored in the RAM.

calibration of the ADC's capacitive capacitor array

The following actions are performed to calibrate capacitors in the 13-bit DACs that comprise the ADC's capacitive array:

1) The IN+ and IN– inputs are internally disconnected from the 13-bit DACs.
2) The most significant bit (MSB) capacitor is tied to REF, while the rest of the array capacitors are tied to GND. The A/D conversion result for the remaining comparator offset, obtained in Step 2 above, is retrieved from the RAM and is input to the 8-bit DACs.
3) Step 1 of the Calibration of Comparator Offset sequence is performed. The 8-bit DAC input is returned to zero and the remaining comparator offset is then subtracted. Thus the comparator offset is completely corrected.
4) Now the MSB capacitor is tied to GND, while the rest of the array capacitors, C_X, are tied to REF. An MSB capacitor voltage error (see Figure 2) on the comparator output will occur if the MSB capacitor does not equal the sum of the other capacitors in the capacitive array. This error voltage is converted to an 8-bit word from which a capacitor error is computed and stored in the RAM.
5) The capacitor voltage error for the next most significant capacitor is calibrated by keeping the MSB capacitor grounded and then performing the above Steps 1-4 while using the next most significant capacitor in lieu of the MSB capacitor. The seven most significant capacitors are calibrated in this manner.

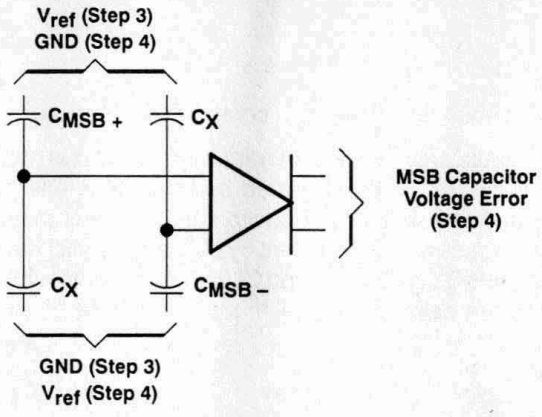


Figure 2. Capacitor Array Null

analog-to-digital conversion

The following steps are performed in the analog-to-digital conversion process:

1) Step 1 of the Calibration of Comparator Offset Sequence is performed. The A/D conversion result for the remaining comparator offset, which was obtained in Step 2 of the Calibration of Comparator Offset, is retrieved from the RAM and is input to the 8-bit DACs. Thus the comparator offset is completely corrected.
2) IN+ and IN– are sampled into the 13-bit capacitive arrays.
3) The 13-bit analog-to-digital conversion is performed. As the successive-approximation conversion proceeds successively through the seven most significant capacitors, the error for each of these capacitors is recovered from the RAM and accumulated in a register. This register controls the 8-bit DACs so the total accumulated error for these capacitors is subtracted out during the conversion process.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (ANLG V_{CC+} and DGTL V_{CC}) (see Note 1) ..... 7.5 V
Supply voltage, ANLG V_{CC-} ..... –7.5 V
Differential supply voltage, ANLG V_{CC+} – ANLG V_{CC-} ..... 15 V
Clock input voltage range ..... –0.3 V to V_{CC} + 0.3 V
Control input voltage range ..... –0.3 V to V_{CC} + 0.3 V
Analog input (IN+, IN–) voltage range,
V_{I+} and V_{I-} ..... ANLG V_{CC-} –0.3 V to ANLG VCC+ +0.3 V
Reference voltage range, V_{ref} ..... –0.3 V to ANLG V_{CC+} +0.3 V
Pin 7 voltage range ..... –0.3 V to ANLG V_{CC+} +0.3 V
Output voltage range ..... –0.3 V to DGTL V_{CC} +0.3 V
Input current (per pin) ..... ±5 mA
Input current (per package) ..... ±20 mA
Operating free-air temperature range, T_A ..... –40°C to 85°C
Storage temperature range ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds ..... 260°C

NOTE 1: All analog voltages are referred to ANLG GND and all digital voltages are referred to DGTL GND.

recommended operating conditions

			MIN	MAX	UNIT
Supply voltage		ANLG V_{CC+}	4.5	5.5	V
		ANLG V_{CC-}	−5.5	ANLG GND	
		DGTL V_{CC}	4.5	5.5	
High-level input voltage, V_{IH} (V_{CC} = 4.75 V to 5.25 V)	All digital inputs except CLK IN		2		V
	CLK IN		3.5		
Low-level input voltage, V_{IL} (V_{CC} = 4.75 V to 5.25 V)	All digital inputs except CLK IN			0.8	V
	CLK IN			1.4	
Analog input voltage, V_{I+}, V_{I-}			ANLG V_{CC-} − 0.05	ANLG V_{CC+} 0.05	V
Pin 7 (TIE HIGH)	V_{CC} = 5 V		2		V
Clock input frequency, f_{clock}	V_{CC} = 5 V		0.3	2	MHz
Clock duty cycle	V_{CC} = 5 V		40%	60%	
Pulse duration, $\overline{CS}$ and $\overline{WR}$ low, t_w	V_{CC} = 5 V		15		ns
Setup time before $\overline{WR}\uparrow$ or $\overline{CS}\uparrow$, t_{su}	V_{CC} = 5 V		60		ns
Hold time after $\overline{WR}\uparrow$ or $\overline{CS}\uparrow$, t_h	V_{CC} = 5 V		50		ns
Operating free-air temperature, T_A			−40	85	°C

electrical characteristics over recommended operating free-air temperature range, ANLG V_{CC+} = DGTL V_{CC} = V_{ref} = 5 V, ANLG V_{CC-} = −5 V or ANLG GND (unless otherwise noted) (see Note 2)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	DGTL V_{CC} = 4.75 V	I_O = −1.8 mA	2.4		V
			I_O = −50 μA	4.5		
V_{OL}	Low-level output voltage	DGTL V_{CC} = 4.75 V,	I_O = 3.2 mA		0.4	V
r_{ref}	Input resistance, REF terminal			1	10	MΩ
I_{IH}	High-level input current	V_I = 5 V			5	μA
I_{IL}	Low-level input current	V_I = 0			−5	μA
I_{OZ}	High-impedance-state output leakage current	V_O = 0			−3	μA
		V_O = 5 V			3	
I_O	Output current	V_O = 0		−6		mA
		V_O = 5 V		8		
DGTL I_{CC}	Supply current from DGTL V_{CC}	f_{clock} = 2 MHz,	$\overline{CS}$ high		6	mA
ANLG I_{CC+}	Supply current from ANLG V_{CC+}	f_{clock} = 2 MHz,	$\overline{CS}$ high		9	mA
ANLG I_{CC-}	Supply current from ANLG V_{CC-}	f_{clock} = 2 MHz,	$\overline{CS}$ high		−3	mA

NOTE 2: The input voltage range is defined as: V_{I+} = −5.05 V to 5.05 V, V_{I-} = −5.05 V to 5.05 V, and $|V_{I+} - V_{I-}| \leq 5.05$ V when ANLG V_{CC-} = −5 V. The input voltage range is defined as: V_{I+} = −0.05 V to 5.05 V, V_{I-} = −0.05 V to 5.05 V, and $|V_{I+} - V_{I-}| \leq 5.05$ V when ANLG V_{CC-} = ANLG GND.

electrical characteristics over recommended operating free-air temperature range, ANLG V_{CC+} = DGTL V_{CC} = V_{ref} = 5 V, ANLG V_{CC-} = −5 V or ANLG GND, f_{clock} = 2 MHz (unless otherwise noted) (see Note 2)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
E_L	Integral linearity error					±0.012%	FSR‡
E_D	Differential linearity		−5 V < (IN+ − IN−) < 5 V, V_{CC+} = 5 V, V_{CC-} = −5 V	>−1		1	LSB§
			0 < (IN+ − IN−) < 5.05 V, V_{CC+} = 5 V, V_{CC-} = 0	>−1		1	
	Zero error					±1.5	LSB
	Unadjusted positive and negative full-scale error					±2	LSB
	Temperature coefficient of gain				15		ppm/°C
	Temperature coefficient of offset point				1.5		ppm/°C
k_{SVS}	Supply voltage sensitivity	Zero error	ANLG V_{CC+} = 5 V ±5%, ANLG V_{CC-} = −5 V ±5%, DGTL V_{CC} = 5 V ±5%		±0.75		LSB
		Positive and negative full-scale error			±0.75		
		Linearity error			±0.25		
CMRR	Common-mode rejection ratio		IN− = IN+ = −5 V to 5 V		65		dB
	Common-mode rejection (maximum code change from code 0000000000000)		IN− = IN+ = −5 V to 5 V		2		LSB
t_{period}	Conversion period ($1/f_{clk}$) (see Notes 3 and 4)					24	clock cycles
t_a	Access time (delay from falling edge of $\overline{CS} \cdot \overline{RD}$ to data output)		C_L = 100 pF			95	ns
t_{dis}	Disable time, output (delay from rising edge of $\overline{RD}$ to high-impedance state)		R_L = 2 kΩ, C_L = 100 pF			90	ns
$t_{d1(READY)}$	Control signal edge to READY OUT delay time			100			ns
$t_{d2(READY)}$	Control signal edge to READY OUT delay time					100	ns
$t_{d(INT)}$	$\overline{RD}$ or $\overline{WR}$ to reset of $\overline{INT}$ delay time					100	ns

† All typical values are at T_A = 25°C.

‡ FSR is Full-Scale Range: 0.012% FSR linearity error is equivalent to 1 LSB = 1.22 mV.

§ No missing codes.

NOTES: 2. The input voltage range is defined as: V_{I+} = −5.05 V to 5.05 V, V_{I-} = −5.05 V to 5.05 V, and $|V_{I+} - V_{I-}| \leq 5.05$ V when ANLG V_{CC-} = −5 V. The input voltage range is defined as: V_{I+} = −0.05 V to 5.05 V, V_{I-} = −0.05 V to 5.05 V, and $|V_{I+} - V_{I-}| \leq 5.05$ V when ANLG V_{CC-} = ANLG GND.

3. If $\overline{INT}$ and $\overline{RD}$ go low within the same f_{clock} period, $\overline{INT}$ will not be reset until $\overline{WR}$ is brought low. If $\overline{INT}$ and $\overline{RD}$ do not go low within the same f_{clock} period, $\overline{INT}$ will be reset.
4. The conversion period is the reciprocal of the conversion rate and includes the access, sample, setup, and A/D conversion times.

PARAMETER MEASUREMENT INFORMATION

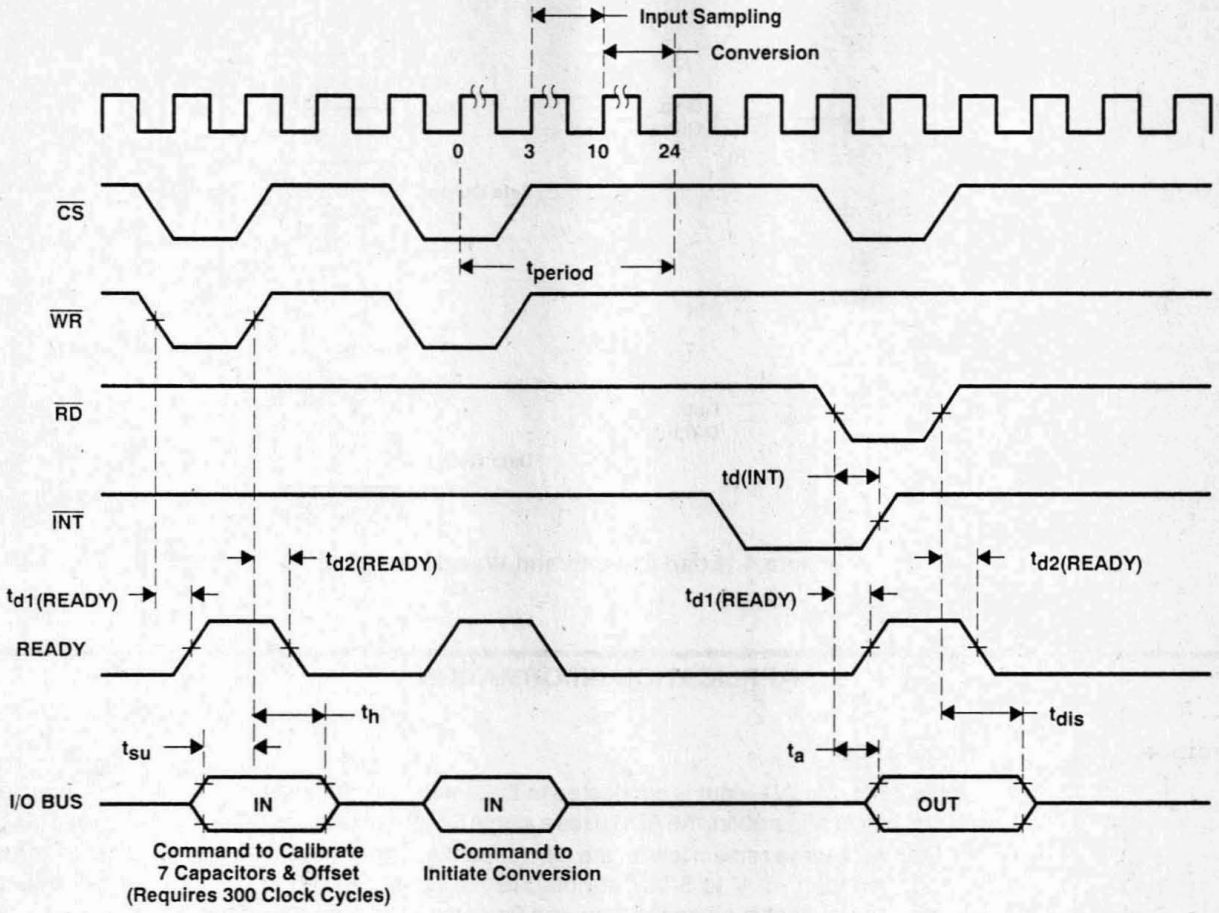


Figure 3. Timing Diagram

PARAMETER MEASUREMENT INFORMATION

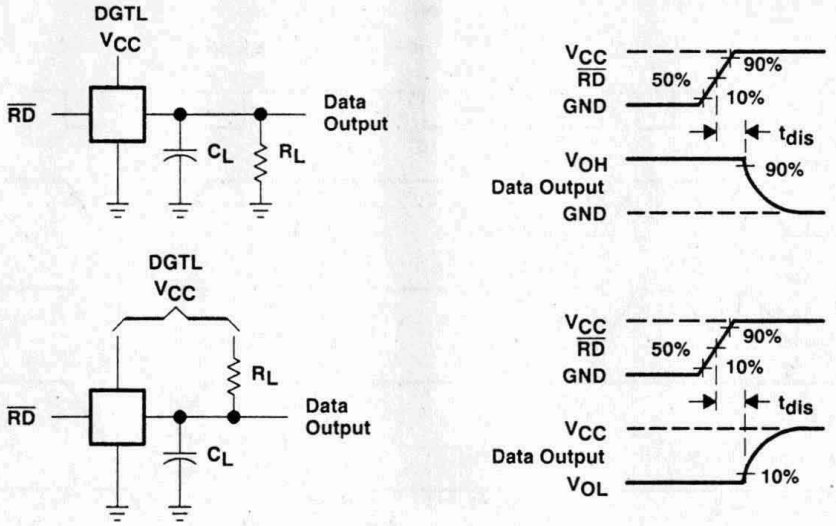


Figure 4. Load Circuits and Waveforms

APPLICATION INFORMATION

unipolar and bipolar operation

For single-ended signal input, the IN+ input is connected to the analog source and the IN– input is connected to ANLG GND. In the unipolar configuration, the ADC uses a single 5-V supply and the analog input voltage range is 0 V to 5 V. Data bit D12 will always remain low. In the bipolar configuration, the ADC uses ±5-V supplies and the analog input voltage range is –5 V to 5 V. Data bit D12 indicates the sign of the input signal. In both configurations, the 13-bit data format is extended sign with 2s-complement, right-justified data.

power-up sequence

Calibration is not automatic on power-up. Calibration is initiated by writing control words to the six least significant bits of the data bus. V_{ref} must have fully settled before calibration is initiated. If addressed or initiated, conversion can begin after the first clock cycle. However, full A/D conversion accuracy is not established until after internal capacitor calibration.

conversion period start sequence

The writing of the conversion command word to the six least significant bits of the data bus, when either $\overline{CS}$ or $\overline{WR}$ goes high, initiates the conversion sequence.

analog sampling sequence

Sampling of the input signal occurs during clock cycles 3 through 10 of the conversion sequence.

completed A/D conversion

When $\overline{INT}$ goes low, conversion is complete and the A/D result can be read. A new conversion period can begin immediately. The A/D conversion is complete at the end of clock cycle 24 of the conversion period.

aborting a conversion period in process and beginning a new conversion

If a conversion period is initiated while a conversion sequence is in process, the ongoing conversion will be aborted and a new conversion period will begin.

reading the conversion result

When both $\overline{CS}$ and $\overline{RD}$ go low, all 13 bits of conversion data are output to the I/O bus. The format of the output is extended sign with 2s-complement, right-justified data. The sign bit D12 is low if $V_{I+} - V_{I-}$ is positive and high if $V_{I+} - V_{I-}$ is negative.

general

reset $\overline{INT}$

When reading the conversion data, the falling edge of the first low-going combination of $\overline{CS}$ and $\overline{RD}$ will reset $\overline{INT}$. The falling edge of the low-going combination of $\overline{CS}$ and $\overline{WR}$ will also reset $\overline{INT}$.

ready out

For high-speed microprocessors, READY OUT allows the TLC1225 to insert a wait state in the microprocessor's read or write cycle.

reference voltage (V_{ref})

This voltage defines the range for $|V_{I+} - V_{I-}|$. When $|V_{I+} - V_{I-}|$ equals V_{ref}, the highest conversion data value results. When $|V_{I+} - V_{I-}|$ equals 0, the conversion data value is zero. Thus, for a given input, the conversion data changes ratiometrically with changes in V_{ref}. Calibration should be performed with the same value of V_{ref} as will be used during conversion.

tie high

This pin is a digital input and should be tied high.

calibration and conversion period considerations

Calibration of the internal capacitors and A/D conversion are two separate actions. Each action is independently initiated. A calibration command should be initiated prior to subsequent conversions. It is not necessary to recalibrate before each conversion. Capacitor calibration is expected to last indefinitely as long as the clock signal and power are not interrupted. However, the offset calibration may drift with temperature changes. The temperature coefficient of the offset point is shown in the electrical characteristics table. Periodic calibration is recommended. Calibration and conversion commands require 300 and 24 clock cycles, respectively.

The calibrate and conversion commands are initiated by writing control words on the six least significant bits of the data bus. These control words are written into the IC when either $\overline{CS}$ or $\overline{WR}$ goes high. The initiation of these commands is illustrated in the Timing Diagram. The bit patterns for the commands are shown in Table 1.

Table 1. Conversion Commands

COMMAND	$\overline{CS} + \overline{WR}$	I/O BUS						REQUIRED NUMBER OF CLOCK CYCLES
		D15	D14	D13	D12	D11	D10	
Conversion	↑	H	L	X	X	X	L	24
Calibrate†	↑	L	X	L	L	L	L	300

† Calibration is lost when clock is stopped.

analog inputs

differential inputs provide common-mode rejection

The differential inputs reduce common-mode noise. Common-mode noise is noise common to both IN+ and IN− inputs, such as 60-Hz noise. There is no time interval between the sampling of the IN+ and IN− so these inputs are truly differential. Thus no conversion errors result from a time interval between the sampling of the IN+ and IN− inputs.

input bypass capacitors

Input bypass capacitors can be used for noise filtering. However, the charge on these bypass capacitors will be depleted during the input sampling sequence when the internal sampling capacitors are charged. Note that the charging of the bypass capacitors through the differential source resistances must keep pace with the charge depletion of the bypass capacitors during the input sampling sequence. Higher source resistances reduce the amount of charging current for the bypass capacitors. Also, note that fast, successive conversion has the greatest charge depletion effect on the bypass capacitors. Therefore, the above phenomenon becomes more significant as source resistances and the conversion rate (i.e., higher clock frequency and conversion initiation rate) increase.

In addition, if the above phenomenon prevents the bypass capacitors from fully charging between conversions, voltage drops across the source resistances will result due to the ongoing bypass capacitor charging currents. The voltage drops cause a conversion error. Also, the voltage drops increase with higher $|V_{I+} - V_{I-}|$ values, higher source resistances, and lower charge on the bypass capacitors (i.e., faster conversion rate).

For low-source-resistance applications ($R_{source} < 100\ \Omega$), a 0.001-μF bypass capacitor at the inputs prevents pickup due to the series lead inductance of a long wire. A 100-Ω resistor can be placed between the capacitor and the output of an operational amplifier to isolate the capacitor from the operational amplifier.

input leads

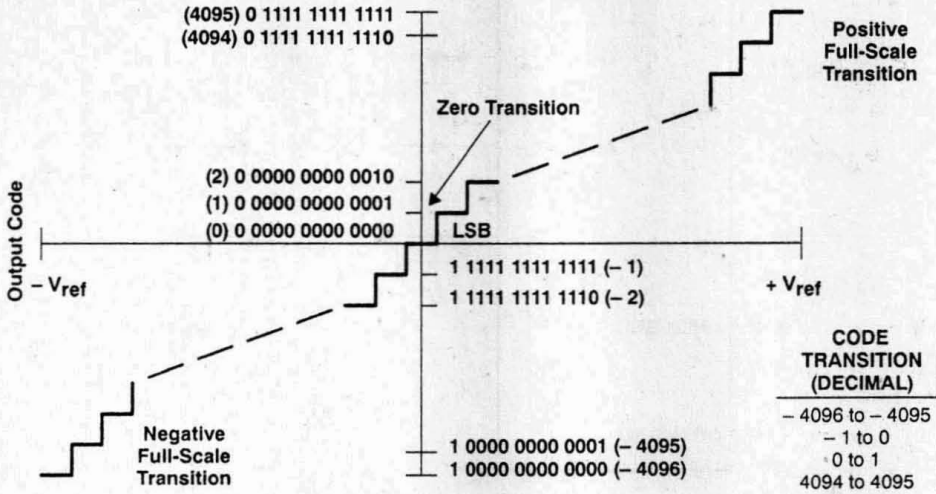
The input leads should be kept as short as possible since the coupling of noise and digital clock signals to the the inputs can cause errors.

power supply considerations

Noise spikes on the V_{CC} lines can cause conversion error. Low-inductance tantalum capacitors (> 1 μF) with short leads should be used to bypass ANLG V_{CC} and DGTL V_{CC}. A separate regulator for the TLC1225 and other analog circuitry greatly reduces digital noise on the supply line.

A ferrite bead or equivalent inductance can be used between the analog and digital ground planes if the digital ground noise is excessive.

APPLICATION INFORMATION

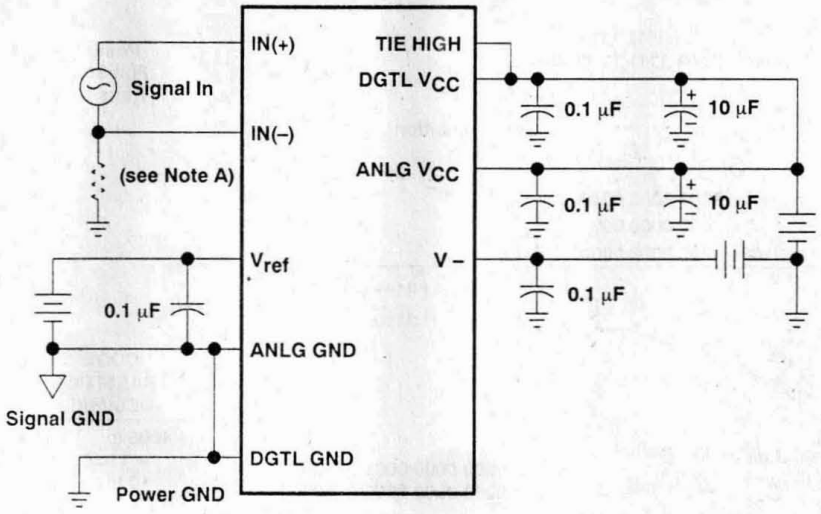


CODE TRANSITION (DECIMAL)	ANALOG INPUT VOLTAGE (LSB)†
– 4096 to – 4095	– 4095.5
– 1 to 0	– 0.5
0 to 1	0.5
4094 to 4095	4094.5

†LSB = V_{ref} + 4096

Figure 5. Transfer Characteristic

APPLICATION INFORMATION



NOTES: A. The analog input must have some current return path to ANALOG GND.
B. Bypass capacitor leads must be as short as possible.
C. For high-accuracy applications, use a larger capacitor to reduce reference noise.

Figure 6. Analog Considerations

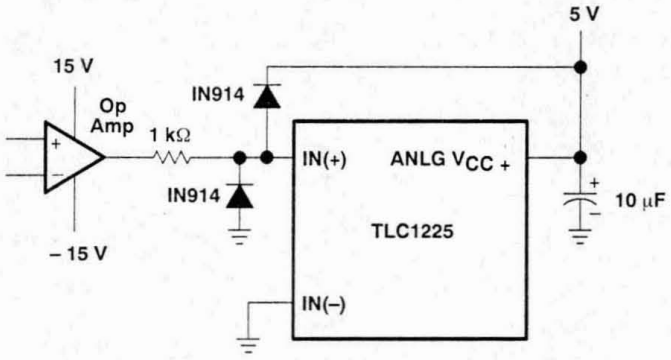
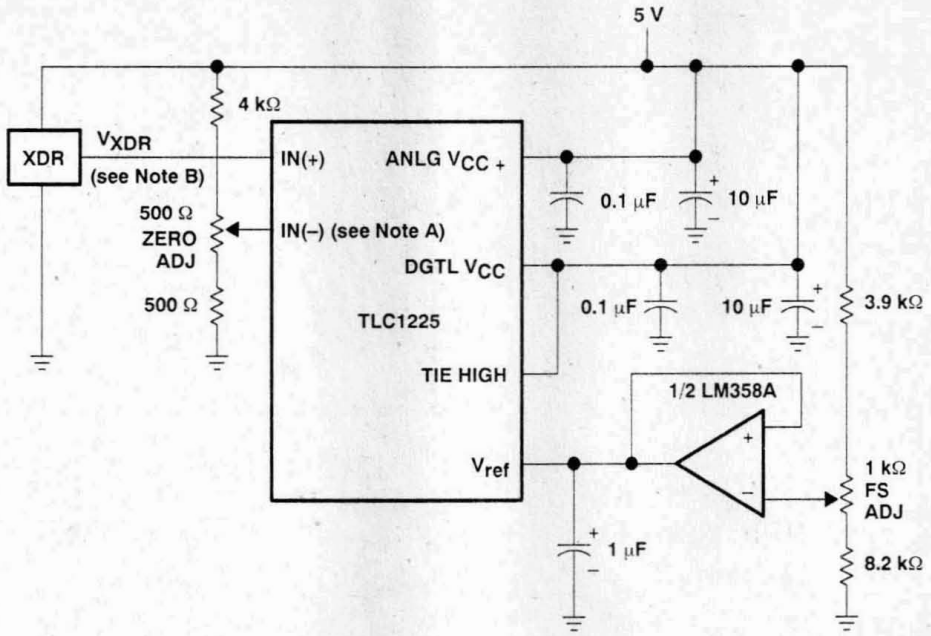


Figure 7. Input Protection

APPLICATION INFORMATION

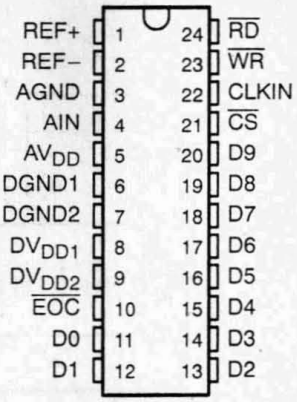


NOTES: A. $V_I = 0.15 \times$ ANLG V_{CC+}.
B. 15% of ANALOG $V_{CC} \le V_{XDR} \le$ 85% of ANALOG V_{CC}.

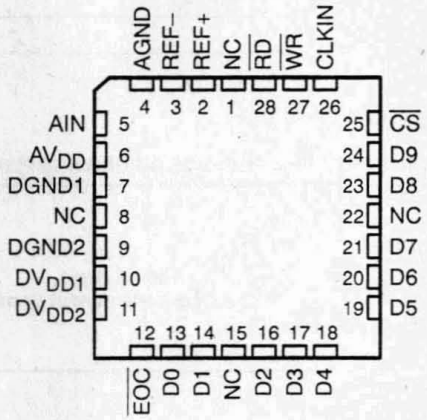
Figure 8. Operating with Ratiometric Transducers

- **Single-Poly Advanced LinEPIC™ Silicon-Gate 1-μm CMOS Technology**
- **Power Dissipation (Max) . . . 40 mW**
- **Advanced LinEPIC™ Single-Poly Process Provides Close Capacitor Matching for Better Accuracy**
- **Fast Parallel Processing for DSP and μP Interface**
- **Either External or Internal Clock Can Be Used**
- **Conversion Time . . . 6 μs**
- **Total Unadjusted Error . . . ±1 LSB Max**

NW PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TLC1550 and TLC1551 are data acquisition converters using a 10-bit, switched-capacitor, successive-approximation network. A high-speed, 3-state parallel port directly interfaces to a digital signal processor (DSP) or microprocessor (μP) system data bus. D0 through D9 are the digital output pins with D0 being the least-significant bit (LSB). Separate power pins for the analog and digital portions minimize noise pickup in the supply leads. Additionally, the digital power is divided into two parts to separate the lower current logic from the higher current bus drivers. An external clock can be applied to the CLKIN pin to override the internal system clock if desired.

The TLC1550I and TLC1551I are characterized for operation from −40°C to 85°C.

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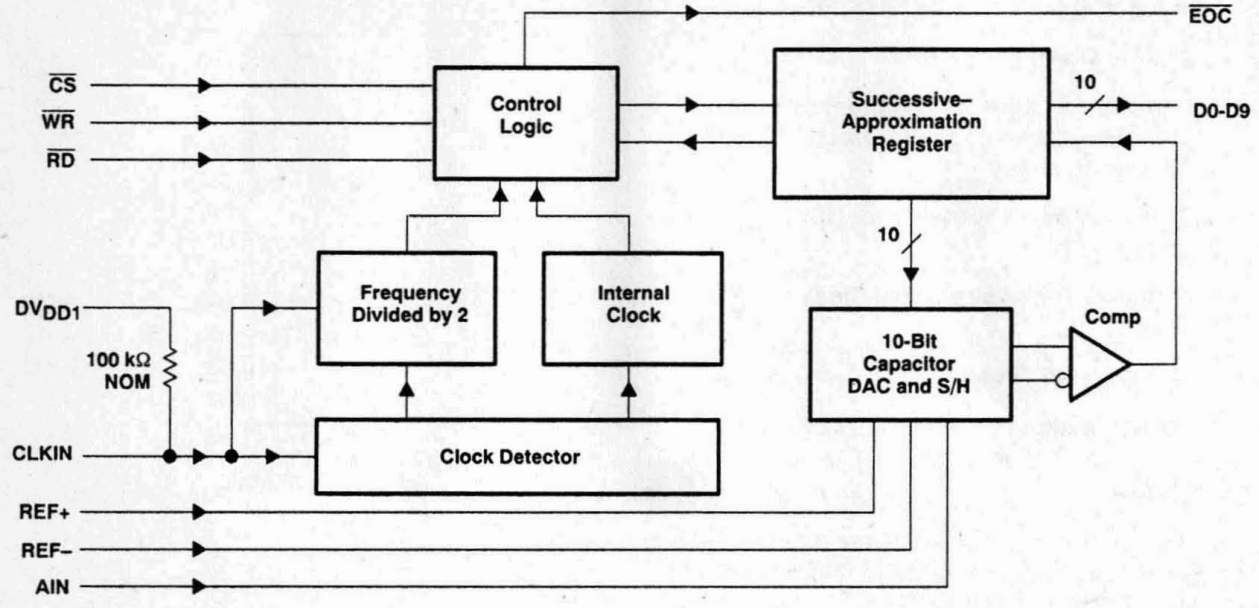
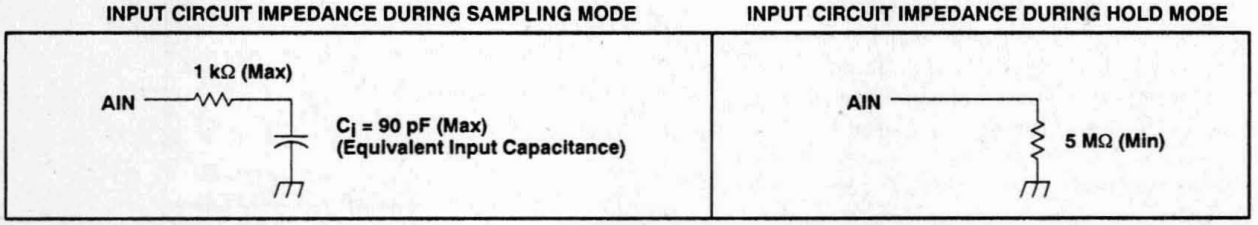
functional block diagram



typical equivalent inputs



Terminal Functions

PIN NAME	PIN NO.†	DESCRIPTION
AGND	3 [4]	This pin is the analog ground and is the reference point for the voltage applied on pins AV_{DD}, AIN, REF+, and REF–.
AIN	4 [5]	Analog voltage input pin. The voltage applied to this pin is converted to the equivalent digital output.
AV_{DD}	5 [6]	The analog positive power supply voltage is applied to this pin. The voltage applied to this pin is designated V_{DD3}.
CLKIN	22 [26]	This pin can be used for external clocking instead of using the internal system clock. It usually takes a few microseconds before the internal clock is disabled. To use the internal clock, this pin should be tied high or left unconnected.
$\overline{CS}$	21 [25]	The chip-select input must be low for $\overline{RD}$ or $\overline{WR}$ to be recognized by the A/D converter.
D0	11 [13]	Data bus output. D0 is bit 1 (LSB).
D1	12 [14]	Data bus output. D1 is bit 2.
D2	13 [16]	Data bus output. D2 is bit 3.
D3	14 [17]	Data bus output. D3 is bit 4.
D4	15 [18]	Data bus output. D4 is bit 5.
D5	16 [19]	Data bus output. D5 is bit 6.
D6	17 [20]	Data bus output. D6 is bit 7.
D7	18 [21]	Data bus output. D7 is bit 8.
D8	19 [23]	Data bus output. D8 is bit 9.
D9	20 [24]	Data bus output. D9 is bit 10 (MSB).
DGND1	6 [7]	Digital ground 1 is the ground for power supply DV_{DD1} and is the substrate connection.
DGND2	7 [9]	Digital ground 2 is the ground for power supply DV_{DD2}.
DV_{DD1}	8 [10]	This is the digital positive power-supply voltage pin that supplies the logic. The voltage applied to this pin is designated V_{DD1}.
DV_{DD2}	9 [11]	This is the digital positive power-supply voltage pin that supplies only the higher-current output buffers. The voltage applied to this pin is designated V_{DD2}.
$\overline{EOC}$	10 [12]	End of Conversion output signal. This signal going low indicates that conversion is complete and the results have been transferred to the output latch. This pin can be connected to the μP or DSP interrupt pin or can be continuously polled.
$\overline{RD}$	24 [28]	When $\overline{CS}$ is low and $\overline{RD}$ is taken low, the data is placed on the data bus from the output latch. The output latch stores the conversion results at the most recent negative edge of $\overline{EOC}$. The falling edge of $\overline{RD}$ resets $\overline{EOC}$ to a high within the $t_{d(EOC)}$ specifications.
REF+	1 [2]	Positive voltage-reference input. Any analog input that is greater than or equal to the voltage on this pin will convert to 1111111111. Analog input voltages between REF+ and REF– will convert to the appropriate result in a ratiometric manner.
REF–	2 [3]	Negative voltage reference input. Any analog input that is less than or equal to the voltage on this pin will convert to 0000000000.
$\overline{WR}$	23 [27]	When $\overline{CS}$ is low, conversion is started on the rising edge of $\overline{WR}$. On this rising edge, the ADC holds the analog input until conversion is completed. Before and after the conversion period, which is given by t_{conv}, the ADC remains in the sampling mode.

† Brackets indicate pin number for FN package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD1}, V_{DD2}, and V_{DD3} (see Note 1) . . . . . 6.5 V
Input voltage range (any input) . . . . . −0.3 V to V_{DD} + 0.3 V
Output voltage range . . . . . −0.3 V to V_{DD} + 0.3 V
Peak input current (any digital input) . . . . . ±10 mA
Peak total input current (all inputs) . . . . . ±30 mA
Operating free-air temperature range . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: NW package . . . . . 260°C

NOTE 1: V_{DD1} is the voltage measured at the DV_{DD1} pin with respect to the DGND1 pin. V_{DD2} is the voltage measured at the DV_{DD2} pin with respect to the DGND2 pin. V_{DD3} is the voltage measured at the AV_{DD} pin with respect to the AGND pin. For these specifications, all ground pins are tied together (and represent 0 V). When V_{DD1}, V_{DD2}, and V_{DD3} are equal, they are referred to simply as V_{DD}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD1}, V_{DD2}, V_{DD3}	4.75	5	5.5	V
Positive reference voltage, V_{REF+} (see Note 2)		V_{DD3}		V
Negative reference voltage, V_{REF-} (see Note 2)		0		V
Differential reference voltage, $V_{REF+} - V_{REF-}$, (see Note 2)		V_{DD3}	V_{DD3}	V
Analog input voltage range	0		V_{DD3}	V
High-level control input voltage, V_{IH}	2			V
Low-level control input voltage, V_{IL}			0.8	V
Input clock frequency, $f_{(CLKIN)}$	0.5		7.8	MHz
Setup time, $\overline{CS}$ low before $\overline{WR}$ or $\overline{RD}$ goes low, $t_{su(CS)}$	0			ns
Hold time, $\overline{CS}$ low after $\overline{WR}$ or $\overline{RD}$ goes high, $t_{h(CS)}$	0			ns
$\overline{WR}$ or $\overline{RD}$ pulse duration, $t_{w(WR)}$	50			ns
Input clock low pulse duration, $t_{wL(CLKIN)}$	40% of period		80% of period	
Operating free-air temperature, T_A	−40		85	°C

NOTE 2: Analog input voltages greater than that applied to REF+ convert to all '1's (1111111111), while input voltages less than that applied to REF− convert to all '0's (0000000000). The total unadjusted error may increase as this differential voltage falls below 4.75 V.

electrical characteristics over recommended operating free-air temperature range, $V_{DD} = V_{REF+} = 4.75$ to 5.5 V and $V_{REF-} = 0$ (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 4.75 V,	I_{OH} = −360 μA	2.4			V
V_{OL}	Low-level output voltage		V_{DD} = 4.75 V,	I_{OL} = 2.4 mA			0.4	V
I_{OZ}	Off-state (high-impedance state) output current		$V_O = V_{DD}$,	$\overline{CS}$ and $\overline{RD}$ at V_{DD}			10	μA
			V_O = 0,	$\overline{CS}$ and $\overline{RD}$ at V_{DD}			−10	
I_{IH}	High-level input current		$V_I = V_{DD}$			0.005	2.5	μA
I_{IL}	Low-level input current (except CLKIN)		V_I = 0		−2.5	−0.005		μA
I_{IL}	Low-level input current (CLKIN)				−150	−50		μA
I_{OS}	Short-circuit output current		V_O = 5 V,	T_A = 25°C	7	14		mA
			V_O = 0,	T_A = 25°C		−12	−6	
I_{DD}	Operating supply current		$\overline{CS}$ low and $\overline{RD}$ high			2	8	mA
C_i	Input capacitance	Analog inputs	See typical equivalent inputs			60	90	pF
		Digital inputs				5	15	

operating characteristics over recommended operating free-air temperature range with internal clock and minimum sampling time of 4 μs, $V_{DD} = V_{REF+} = 5$ V and $V_{REF-} = 0$ (unless otherwise noted)

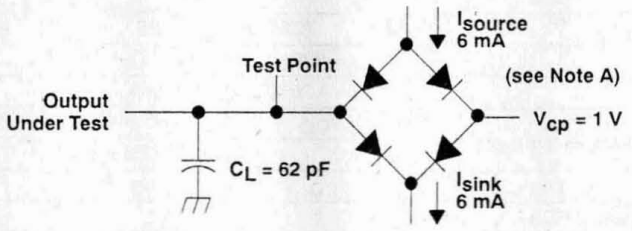
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
E_L	Linearity error	TLC1550	See Note 3			±0.5	LSB
		TLC1551				±1	
E_{ZS}	Zero-scale error	See Notes 2 and 4				±1	LSB
E_{FS}	Full-scale error	TLC1550	See Notes 2 and 4			±0.5	LSB
		TLC1551				±1	
	Total unadjusted error	See Note 5				±1	LSB
t_{conv}	Conversion time	f_{CLK} (external) = 4.2 MHz or internal clock				6	μs
$t_{a(D)}$	Data access time after $\overline{RD}$ goes low	See Figure 1				35	ns
$t_{v(D)}$	Data valid time after $\overline{RD}$ goes high			5			ns
$t_{dis(D)}$	Disable time, delay time from $\overline{RD}$ high to Hi-Z					30	ns
$t_{d(EOC)}$	Delay time, $\overline{RD}$ low to $\overline{EOC}$ high			0	15		ns

† All typical values are at V_{DD} = 5 V, T_A = 25°C.

NOTES: 2. Analog input voltages greater than that applied to REF+ convert to all '1's (1111111111), while input voltages less than that applied to REF− convert to all '0's (0000000000). The total unadjusted error may increase as this differential voltage falls below 4.75 V.

3. Linearity error is the difference between the actual analog value at the transition between any two adjacent steps and its ideal value after zero-scale error and full-scale error have been removed.
4. Zero-scale error is the difference between the actual mid-step value and the nominal mid-step value at specified zero scale. Full-scale error is the difference between the actual mid-step value and the nominal mid-step value at specified full scale.
5. Total unadjusted error is the difference between the actual analog value at the transition between any two adjacent steps and its ideal value. It includes contributions from zero-scale error, full-scale error, and linearity error.

PARAMETER MEASUREMENT INFORMATION



NOTE A. Equivalent load circuit of the Teradyne A500 tester for timing parameter measurement.

Figure 1. Test Load Circuit

PRINCIPLES OF OPERATION

The operating sequence for complete data acquisition is shown in Figure 2. Processors can address the TLC1550 and TLC1551 as an external memory device by simply connecting the address lines to a decoder and the decoder output to the $\overline{CS}$ pin. Like other peripheral devices, the write ($\overline{WR}$) and read ($\overline{RD}$) input signals are valid only when $\overline{CS}$ is low. Once $\overline{CS}$ is low, the on-board system clock permits the conversion to begin with a simple write command and the converted data to be presented to the data bus with a simple read command. The device remains in a sampling (track) mode until conversion begins with the rising edge of $\overline{WR}$, which initiates the hold mode. After the hold mode begins, the clock controls the conversion automatically. When the conversion is complete, the end-of-conversion ($\overline{EOC}$) signal goes low indicating that the digital data has been transferred to the output latch. Lowering $\overline{CS}$ and $\overline{RD}$ then resets $\overline{EOC}$ and transfers the data to the data bus for the processor read cycle.

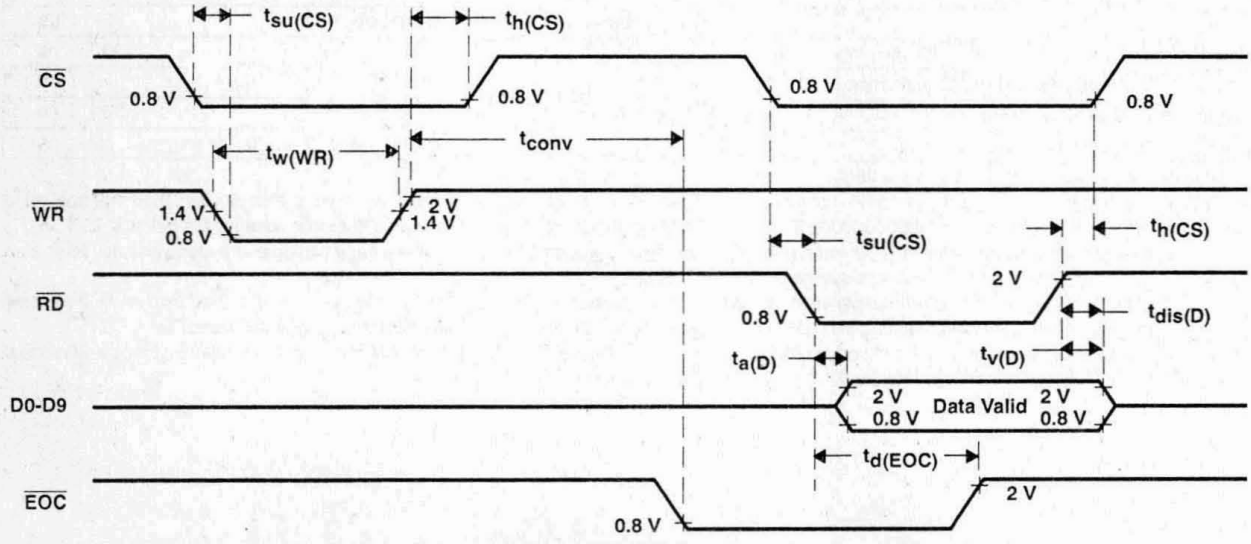


Figure 2. TLC1550 or TLC1551 Operating Sequence

APPLICATIONS INFORMATION

Using the equivalent circuit in Figure 3, the time required to charge the analog input capacitance from 0 to V_S within 1 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S \left(1-e^{-t_c/R_tC_i}\right) \quad (1)$$

where

$$R_t = R_s + r_i$$

The final voltage to 1 LSB is given by

$$V_C\ (\text{LSB}) = V_S - (V_S/1024) \quad (2)$$

Equating equation 1 to equation 2 and solving for time t_c gives

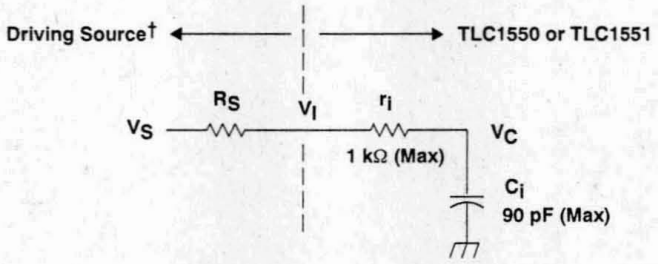
$$V_S - (V_S/1024) = V_S\left(1-e^{-t_c/R_tC_i}\right) \quad (3)$$

and

$$t_c\ (\text{LSB}) = R_t \times C_i \times \ln 1024 \quad (4)$$

Therefore, with the values given

$$t_c\ (\text{LSB}) = (R_s + 1\ \text{k}\Omega) \times 60\ \text{pF} \times \ln 1024 \quad (5)$$



V_I = Input Voltage at AIN
V_S = External Driving Source Voltage
R_s = Source Resistance
r_i = Input Resistance
C_i = Equivalent Input Capacitance

Figure 3. Equivalent Input Circuit Including the Driving Source

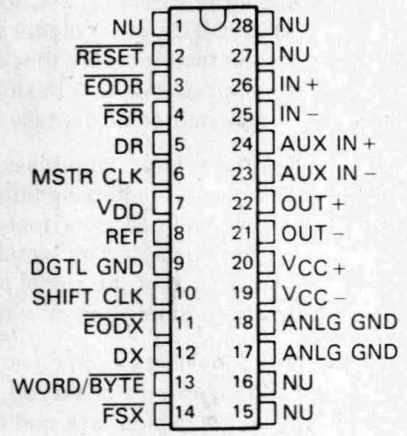
† Driving source requirements for 10-bit measurements

1. $R_S \le 100\ \Omega$
2. Noise and distortion ≤ 80 dB
3. R_S must be real at the input frequency.

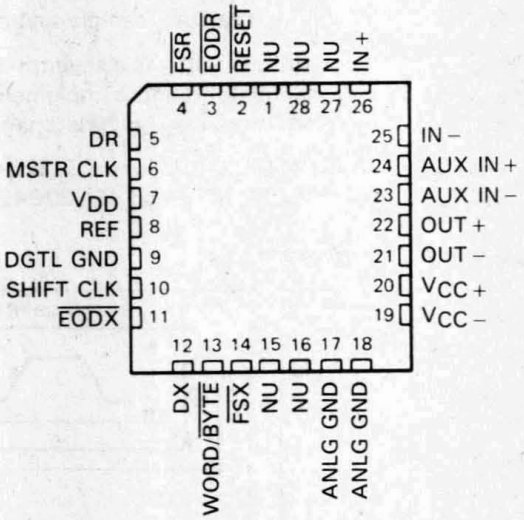
- **Advanced LinCMOS™ Silicon-Gate Process Technology**
- **14-Bit Dynamic Range ADC and DAC**
- **Variable ADC and DAC Sampling Rate Up to 19,200 Samples per Second**
- **Switched-Capacitor Antialiasing Input Filter and Output-Reconstruction Filter**
- **Serial Port for Direct Interface to TMS32011, TMS320C17, TMS32020, and TMS320C25 Digital Processors**
- **Synchronous or Asynchronous ADC and DAC Conversion Rates with Programmable Incremental ADC and DAC Conversion Timing Adjustments**
- **Serial Port Interface to SN74299 Serial-to-Parallel Shift Register for Parallel Interface to TMS32010, TMS320C15, or Other Digital Processors**
- **600-mil Wide N Package (C_L to C_L)**

PART NUMBER	DESCRIPTION
TLC32040	Analog Interface Circuit with internal reference. Also a plug-in replacement for TLC32041.
TLC32041	Analog Interface Circuit without internal reference.
TLC32042	Identical to TLC32040, but has a slightly wider bandpass filter bandwidth

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NU—Nonusable; no external connection should be made to these pins.

description

The TLC32040, TLC32041, and TLC32042 are complete analog-to-digital and digital-to-analog input/output systems, each on a single monolithic CMOS chip. This device integrates a bandpass switched-capacitor antialiasing input filter, a 14-bit-resolution A/D converter, four microprocessor-compatible serial port modes, a 14-bit-resolution D/A converter, and a low-pass switched-capacitor output-reconstruction filter. The device offers numerous combinations of Master Clock input frequencies and conversion/sampling rates, which can be changed via digital processor control.

Typical applications for this IC include modems (7.2-, 8-, 9.6-, 14.4-, and 19.2-kHz sampling rate), analog interface for digital signal processors (DSPs), speech recognition/storage systems, industrial process control, biomedical instrumentation, acoustical signal processing, spectral analysis, data acquisition, and instrumentation recorders. Four serial modes, which allow direct interface to the TMS32011, TMS320C17, TMS32020, and TMS320C25 digital signal processors, are provided. Also, when the transmit and receive sections of the Analog Interface Circuit (AIC) are operating synchronously, it will interface to two SN74299

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description (continued)

serial-to-parallel shift registers. These serial-to-parallel shift registers can then interface in parallel to the TMS32010, TMS320C15, other digital signal processors, or external FIFO circuitry. Output data pulses are emitted to inform the processor that data transmission is complete or to allow the DSP to differentiate between two transmitted bytes. A flexible control scheme is provided so that the functions of the IC can be selected and adjusted coincidentally with signal processing via software control.

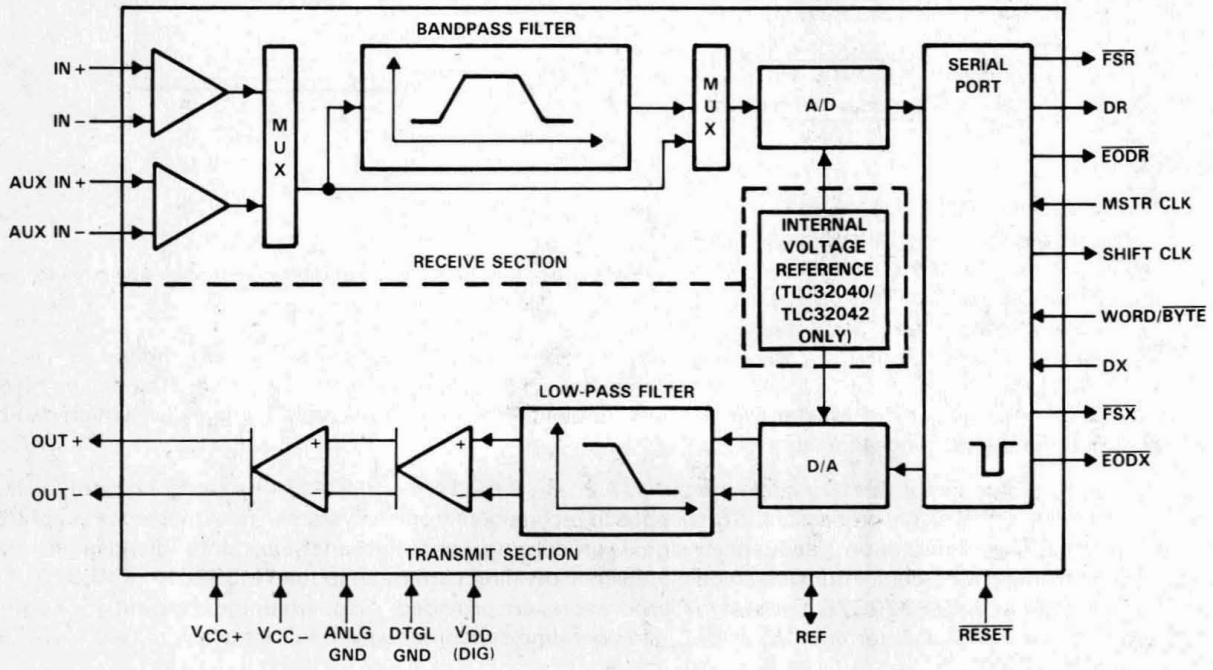
The antialiasing input filter comprises seventh-order and fourth-order CC-type (Chebyshev/elliptic transitional) low-pass and high-pass filters, respectively, and a fourth-order equalizer. The input filter is implemented in switched-capacitor technology and is preceded by a continuous time filter to eliminate any possibility of aliasing caused by sampled data filtering. When no filtering is desired, the entire composite filter can be switched out of the signal path. A selectable, auxiliary, differential analog input is provided for applications where more than one analog input is required.

The A/D and D/A converters each have 14 bits of resolution. The A/D and D/A architectures ensure no missing codes and monotonic operation. An internal voltage reference is provided on the TLC32040 and TLC32042 to ease the design task and to provide complete control over the performance of the IC. The internal voltage reference is brought out to a pin and is available to the designer. Separate analog and digital voltage supplies and grounds are provided to minimize noise and ensure a wide dynamic range. Also, the analog circuit path contains only differential circuitry to keep noise to an absolute minimum. The only exception is the DAC sample-and-hold, which utilizes pseudo-differential circuitry.

The output-reconstruction filter is a seventh-order CC-type (Chebyshev/elliptic transitional low-pass filter with a fourth-order equalizer) and is implemented in switched-capacitor technology. This filter is followed by a continuous-time filter to eliminate images of the digitally encoded signal.

The TLC32040C, TLC32041C, and TLC32042C are characterized for operation from 0°C to 70°C and the TLC32040I, TLC32041I, and TLC32042I are characterized for operation from −40°C to 85°C.

functional block diagram



PRINCIPLES OF OPERATION

analog input

Two sets of analog inputs are provided. Normally, the IN+ and IN− input set is used; however, the auxiliary input set, AUX IN+ and AUX IN−, can be used if a second input is required. Each input set can be operated in either differential or single-ended modes, since sufficient common-mode range and rejection are provided. The gain for the IN+, IN−, AUX IN+, and AUX IN− inputs can be programmed to be either 1, 2, or 4 (see Table 2). Either input circuit can be selected via software control. It is important to note that a wide dynamic range is assured by the differential internal analog architecture and by the separate analog and digital voltage supplies and grounds.

A/D bandpass filter, A/D bandpass filter clocking, and A/D conversion timing

The A/D bandpass filter can be selected or bypassed via software control. The frequency response of this filter is presented in the following pages. This response results when the switched-capacitor filter clock frequency is 288 kHz. Several possible options can be used to attain a 288-kHz switched-capacitor filter clock. When the filter clock frequency is not 288 kHz, the filter transfer function is frequency-scaled by the ratio of the actual clock frequency to 288 kHz. The low-frequency roll-off of the high-pass section is 300 Hz. However, the high-pass section low-frequency roll-off is less steep for the TLC32042 than for the TLC32040 and TLC32041.

The Internal Timing Configuration and AIC DX Data Word Format sections of this data sheet indicate the many options for attaining a 288-kHz bandpass switched-capacitor filter clock. These sections indicate that the RX Counter A can be programmed to give a 288-kHz bandpass switched-capacitor filter clock for several Master Clock input frequencies.

The A/D conversion rate is then attained by frequency-dividing the 288-kHz bandpass switched-capacitor filter clock with the RX Counter B. Thus, unwanted aliasing is prevented because the A/D conversion rate is an integral submultiple of the bandpass switched-capacitor filter sampling rate, and the two rates are synchronously locked.

A/D converter performance specifications

Fundamental performance specifications for the A/D converter circuitry are presented in the A/D converter operating characteristics section of this data sheet. The realization of the A/D converter circuitry with switched-capacitor techniques provides an inherent sample-and-hold.

analog output

The analog output circuitry is an analog output power amplifier. Both noninverting and inverting amplifier outputs are brought out of the IC. This amplifier can drive transformer hybrids or low-impedance loads directly in either a differential or single-ended configuration.

D/A low-pass filter, D/A low-pass filter clocking, and D/A conversion timing

The frequency response of this filter is presented in the following pages. This response results when the low-pass switched-capacitor filter clock frequency is 288 kHz. Like the A/D filter, the transfer function of this filter is frequency-scaled when the clock frequency is not 288 kHz. A continuous-time filter is provided on the output of the D/A low-pass filter to greatly attenuate any switched-capacitor clock feedthrough.

The D/A conversion rate is then attained by frequency-dividing the 288-kHz switched-capacitor filter clock with TX Counter B. Thus, unwanted aliasing is prevented because the D/A conversion rate is an integral submultiple of the switched-capacitor low-pass filter sampling rate, and the two rates are synchronously locked.

PRINCIPLES OF OPERATION (continued)

asynchronous versus synchronous operation

If the transmit section of the AIC (low-pass filter and DAC) and receive section (bandpass filter and ADC) are operated asynchronously, the low-pass and band-pass filter clocks are independently generated from the Master Clock signal. Also, the D/A and A/D conversion rates are independently determined. If the transmit and receive sections are operated synchronously, the low-pass filter clock drives both low-pass and bandpass filters. In synchronous operation, the A/D conversion timing is derived from, and is equal to, the D/A conversion timing. (See description of the WORD/$\overline{\text{BYTE}}$ pin in the Pin Functional Description Section.)

D/A converter performance specifications

Fundamental performance specifications for the D/A converter circuitry are presented in the D/A converter operating characteristics section of the data sheet. The D/A converter has a sample-and-hold that is realized with a switched-capacitor ladder.

system frequency response correction

Sin x/x correction circuitry is performed in digital signal processor software. The system frequency response can be corrected via DSP software to ± 0.1 dB accuracy to a band-edge of 3000 Hz for all sampling rates. This correction is accomplished with a first-order digital correction filter, which requires only seven TMS320 instruction cycles. With a 200-ns instruction cycle, seven instructions represent an overhead factor of only 1.1% and 1.3% for sampling rates of 8 and 9.6 kHz, respectively (see the sin x/x Correction Section for more details).

serial port

The serial port has four possible modes that are described in detail in the Functional Pin Description Section. These modes are briefly described below and in the Functional Description for Pin 13, WORD/$\overline{\text{BYTE}}$.

1. The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS32011 and TMS320C17.
2. The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS32020 and the TMS320C25.
3. The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS32011 and TMS320C17.
4. The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS32020, TMS320C25, or two SN74299 serial-to-parallel shift registers, which can then interface in parallel to the TMS32010, TMS320C15, to any other digital signal processor, or to external FIFO circuitry.

operation of TLC32040 or TLC32042 with internal voltage reference

The internal reference of the TLC32040 and TLC32042 eliminates the need for an external voltage reference and provides overall circuit cost reduction. Thus, the internal reference eases the design task and provides complete control over the performance of the IC. The internal reference is brought out to a pin and is available to the designer. To keep the amount of noise on the reference signal to a minimum, an external capacitor may be connected between REF and ANLG GND.

PRINCIPLES OF OPERATION (continued)

operation of TLC32040, TLC32041, or TLC32042 with external voltage reference

The REF pin may be driven from an external reference circuit if so desired. This external circuit must be capable of supplying 250 μA and must be adequately protected from noise such as crosstalk from the analog input.

reset

A reset function is provided to initiate serial communications between the AIC and DSP and to allow fast, cost-effective testing during manufacturing. The reset function will initialize all AIC registers, including the control register. After a negative-going pulse on the $\overline{\text{RESET}}$ pin, the AIC will be initialized. This initialization allows normal serial port communications activity to occur between AIC and DSP (see AIC DX Data Word Format section).

loopback

This feature allows the user to test the circuit remotely. In loopback, the OUT + and OUT – pins are internally connected to the IN + and IN – pins. Thus, the DAC bits (d15 to d2), which are transmitted to the DX pin, can be compared with the ADC bits (d15 to d2), which are received from the DR pin. An ideal comparison would be that the bits on the DR pin equal the bits on the DX pin. However, in practice there will be some difference in these bits due to the ADC and DAC output offsets.

In loopback, if the IN + and IN – pins are enabled, the external signals on the IN + and IN – pins are ignored. If the AUX IN + and AUX IN – pins are enabled, the external signals on these pins are added to the OUT + and OUT – signals in loopback operation.

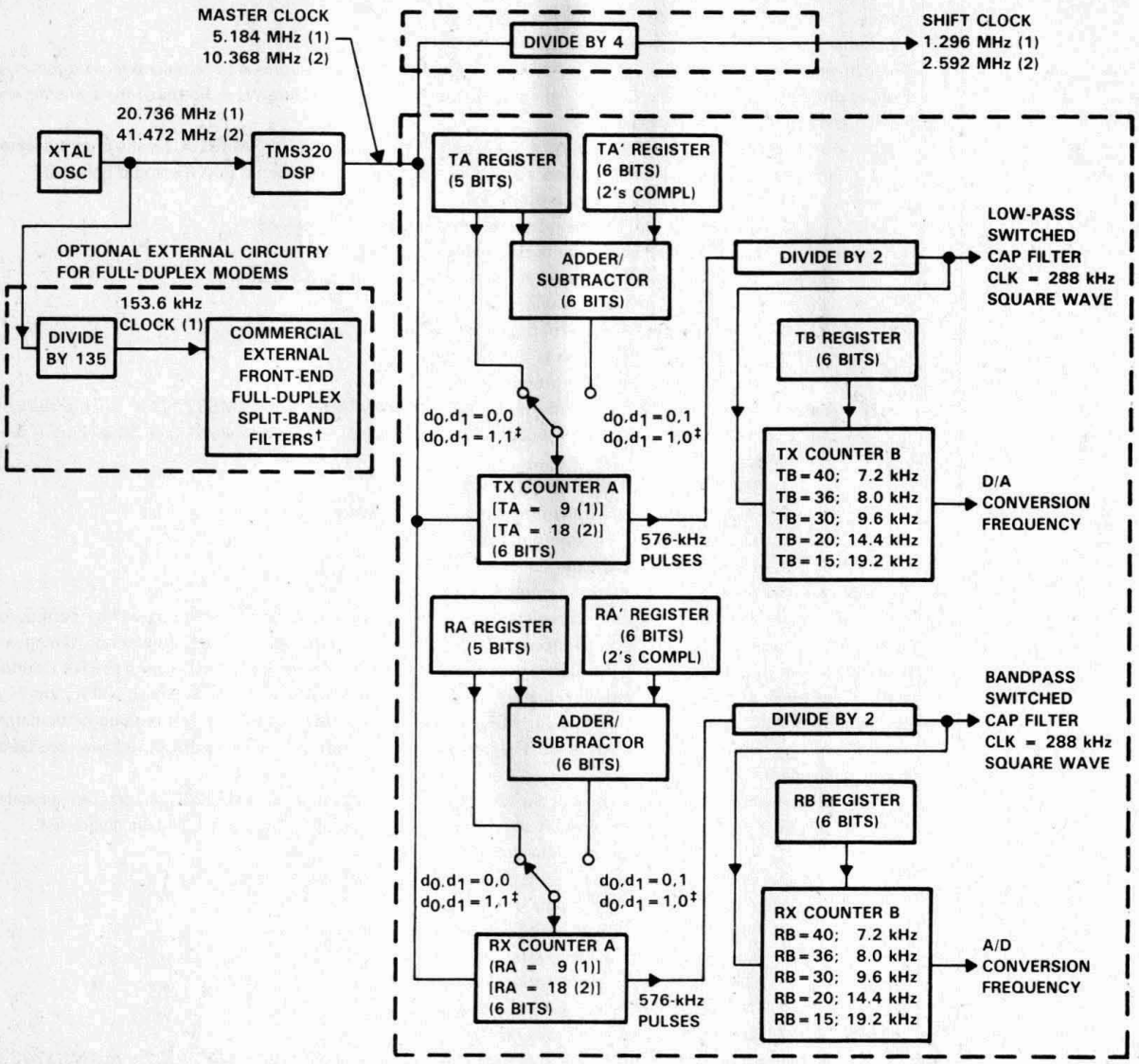
The loopback feature is implemented with digital signal processor control by transmitting the appropriate serial port bit to the control register (see AIC Data Word Format section).

PIN NAME	PIN NO.	I/O	DESCRIPTION
ANLG GND	17,18		Analog ground return for all internal analog circuits. Not internally connected to DGTL GND.
AUX IN +	24	I	Noninverting auxiliary analog input stage. This input can be switched into the bandpass filter and A/D converter path via software control. If the appropriate bit in the Control register is a 1, the auxiliary inputs will replace the IN + and IN – inputs. If the bit is a 0, the IN + and IN – inputs will be used (see the AIC DX Data Word Format section).
AUX IN –	23	I	Inverting auxiliary analog input (see the above AUX IN + pin description).
DGTL GND	9		Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
DR	5	O	This pin is used to transmit the ADC output bits from the AIC to the TMS320 serial port. This transmission of bits from the AIC to the TMS320 serial port is synchronized with the SHIFT CLK signal.
DX	12	I	This pin is used to receive the DAC input bits and timing and control information from the TMS320. This serial transmission from the TMS320 serial port to the AIC is synchronized with the SHIFT CLK signal.
$\overline{\text{EODR}}$	3	O	End of Data Receive. See the WORD/$\overline{\text{BYTE}}$ pin description and the Serial Port Timing diagram. During the word-mode timing, this signal is a low-going pulse that occurs immediately after the 16 bits of A/D information have been transmitted from the AIC to the TMS320 serial port. This signal can be used to interrupt a microprocessor upon completion of serial communications. Also, this signal can be used to strobe and enable external serial-to-parallel shift registers, latches, or external FIFO RAM, and to facilitate parallel data bus communications between the AIC and the serial-to-parallel shift registers. During the byte-mode timing, this signal goes low after the first byte has been transmitted from the AIC to the TMS320 serial port and is kept low until the second byte has been transmitted. The TMS32011 or TMS320C17 can use this low-going signal to differentiate between the two bytes as to which is first and which is second. $\overline{\text{EODR}}$ does not occur after secondary communication.

PIN NAME	PIN NO.	I/O	DESCRIPTION
$\overline{\text{EODX}}$	11	O	End of Data Transmit. See the WORD/$\overline{\text{BYTE}}$ pin description and the Serial Port Timing diagram. During the word-mode timing, this signal is a low-going pulse that occurs immediately after the 16 bits of D/A converter and control or register information have been transmitted from the TMS320 serial port to the AIC. This signal can be used to interrupt a microprocessor upon the completion of serial communications. Also, this signal can be used to strobe and enable external serial-to-parallel shift registers, latches, or an external FIFO RAM, and to facilitate parallel data-bus communications between the AIC and the serial-to-parallel shift registers. During the byte-mode timing, this signal goes low after the first byte has been transmitted from the TMS320 serial port to the AIC and is kept low until the second byte has been transmitted. The TMS32011 or TMS320C17 can use this low-going signal to differentiate between the two bytes as to which is first and which is second.
$\overline{\text{FSR}}$	4	O	Frame Sync Receive. In the serial transmission modes, which are described in the WORD/$\overline{\text{BYTE}}$ pin description, the $\overline{\text{FSR}}$ pin is held low during bit transmission. When the $\overline{\text{FSR}}$ pin goes low, the TMS320 serial port will begin receiving bits from the AIC via the DR pin of the AIC. The most significant DR bit will be present on the DR pin before $\overline{\text{FSR}}$ goes low. (See Serial Port Timing and Internal Timing Configuration diagrams.) $\overline{\text{FSR}}$ does not occur after secondary communication.
$\overline{\text{FSX}}$	14	O	Frame Sync Transmit. When this pin goes low, the TMS320 serial port will begin transmitting bits to the AIC via the DX pin of the AIC. In all serial transmission modes, which are described in the WORD/$\overline{\text{BYTE}}$ pin description, the $\overline{\text{FSX}}$ pin is held low during bit transmission (see Serial Port Timing and Internal Timing Configuration diagrams).
IN+	26	I	Noninverting input to analog input amplifier stage
IN−	25	I	Inverting input to analog input amplifier stage
MSTR CLK	6	I	The Master Clock signal is used to derive all the key logic signals of the AIC, such as the Shift Clock, the switched-capacitor filter clocks, and the A/D and D/A timing signals. The Internal Timing Configuration diagram shows how these key signals are derived. The frequencies of these key signals are synchronous submultiples of the Master Clock frequency to eliminate unwanted aliasing when the sampled analog signals are transferred between the switched-capacitor filters and the A/D and D/A converters (see the Internal Timing Configuration).
OUT+	22	O	Noninverting output of analog output power amplifier. Can drive transformer hybrids or high-impedance loads directly in either a differential or a single-ended configuration.
OUT−	21	O	Inverting output of analog output power amplifier. Functionally identical with and complementary to OUT+.
REF	8	I/O	For the TLC32040 and TLC32042, the internal voltage reference is brought out on this pin. For the TLC32040, TLC32041, and TLC32042, an external voltage reference can be applied to this pin.
$\overline{\text{RESET}}$	2	I	A reset function is provided to initialize the TA, TA′, TB, RA, RA′, RB, and control registers. This reset function initiates serial communications between the AIC and DSP. The reset function will initialize all AIC registers including the control register. After a negative-going pulse on the $\overline{\text{RESET}}$ pin, the AIC registers will be initialized to provide an 8-kHz data conversion rate for a 5.184-MHz master clock input signal. The conversion rate adjust registers, TA′ and RA′, will be reset to 1. The CONTROL register bits will be reset as follows (see AIC DX Data Word Format section). d7 = 1, d6 = 1, d5 = 1, d4 = 0, d3 = 0, d2 = 1 This initialization allows normal serial-port communication to occur between AIC and DSP.
SHIFT CLK	10	O	The Shift Clock signal is obtained by dividing the Master Clock signal frequency by four. This signal is used to clock the serial data transfers of the AIC, described in the WORD/$\overline{\text{BYTE}}$ pin description below (see the Serial Port Timing and Internal Timing Configuration diagram).
V_{DD}	7		Digital supply voltage, 5 V ±5%
V_{CC+}	20		Positive analog supply voltage, 5 V ±5%
V_{CC-}	19		Negative analog supply voltage −5 V ±5%

PIN NAME	NO.	I/O	DESCRIPTION
WORD/$\overline{\text{BYTE}}$	13	I	This pin, in conjunction with a bit in the CONTROL register, is used to establish one of four serial modes. These four serial modes are described below. *AIC transmit and receive sections are operated asynchronously.* The following description applies when the AIC is configured to have asynchronous transmit and receive sections. If the appropriate data bit in the Control register is a 0 (see the AIC DX Data Word Format), the transmit and receive sections will be asynchronous. L Serial port directly interfaces with the serial port of the TMS32011 or TMS320C17 and communicates in two 8-bit bytes. The operation sequence is as follows (see Serial Port Timing diagrams). 1. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought low. 2. One 8-bit byte is transmitted or one 8-bit byte is received. 3. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pin is brought low. 4. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin emits a positive frame-sync pulse that is four Shift Clock cycles wide. 5. One 8-bit byte is transmitted or one 8-bit byte is received. 6. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pin is brought high. 7. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought high. H Serial port directly interfaces with the serial port of the TMS32020, TMS320C25, or TMS320C30 and communicates in one 16-bit word. The operation sequence is as follows (see Serial Port Timing diagrams): 1. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought low. 2. One 16-bit word is transmitted or one 16-bit word is received. 3. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought high. 4. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pin emits a low-going pulse. *AIC transmit and receive sections are operated synchronously.* If the appropriate data bit in the Control register is a 1, the transmit and receive sections will be configured to be synchronous. In this case, the bandpass switched-capacitor filter and the A/D conversion timing will be derived from the TX Counter A, TX Counter B, and TA, TA′, and TB registers, rather than the RX Counter A, RX Counter B, and RA, RA′, and RB registers. In this case, the AIC $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ timing will be identical during primary data communication; however, $\overline{\text{FSR}}$ will not be asserted during secondary data communication since there is no new A/D conversion result. The synchronous operation sequences are as follows (see Serial Port Timing diagrams). L Serial port directly interfaces with the serial port of the TMS32011 or TMS320C17 and communicates in two 8-bit bytes. The operation sequence is as follows (see Serial Port Timing diagrams): 1. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought low. 2. One 8-bit byte is transmitted and one 8-bit byte is received. 3. The $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ pins are brought low. 4. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins emit positive frame-sync pulses that are four Shift Clock cycles wide. 5. One 8-bit byte is transmitted and one 8-bit byte is received. 6. The $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ pins are brought high. 7. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought high. H Serial port directly interfaces with the serial port of the TMS32020, TMS320C25, or TMS320C30 and communicates in one 16-bit word. The operation sequence is as follows (see Serial Port Timing diagrams): 1. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought low. 2. One 16-bit word is transmitted and one 16-bit word is received. 3. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought high. 4. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pins emit low-going pulses. Since the transmit and receive sections of the AIC are now synchronous, the AIC serial port, with additional NOR and AND gates, will interface to two SN74299 serial-to-parallel shift registers. Interfacing the AIC to the SN74299 shift register allows the AIC to interface to an external FIFO RAM and facilitates parallel, data bus communications between the AIC and the digital signal processor. The operation sequence is the same as the above sequence (see Serial Port Timing diagrams).

INTERNAL TIMING CONFIGURATION



$$\text{SCF Clock Frequency} = \frac{\text{Master Clock Frequency}}{2 \times \text{Contents of Counter A}}$$

NOTE: Frequency 1, 20.736 MHz, is used to show how 153.6 kHz (for a commercially available modem split-band filter clock), popular speech and modem sampling signal frequencies, and an internal 288-kHz switched-capacitor filter clock can be derived synchronously and as submultiples of the crystal oscillator frequency. Since these derived frequencies are synchronous submultiples of the crystal frequency, aliasing does not occur as the sampled analog signal passes between the analog converter and switched-capacitor filter stages. Frequency 2, 41.472 MHz, is used to show that the AIC can work with high-frequency signals, which are used by high-speed digital signal processors.

†Split-band filtering can alternatively be performed after the analog input function via software in the TMS320.

‡These control bits are described in the AIC DX Data Word Format section.

explanation of internal timing configuration

All of the internal timing of the AIC is derived from the high-frequency clock signal that drives the Master Clock input pin. The Shift Clock signal, which strobes the serial port data between the AIC and DSP, is derived by dividing the Master Clock input signal frequency by four.

$$\text{SCF Clock Frequency} = \frac{\text{Master Clock Frequency}}{2 \times \text{Contents of Counter A}}$$

$$\text{Conversion Frequency} = \frac{\text{SCF Clock Frequency}}{\text{Contents of Counter B}}$$

$$\text{Shift Clock Frequency} = \frac{\text{Master Clock Frequency}}{4}$$

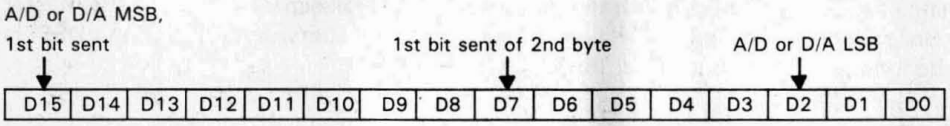
TX Counter A and TX Counter B, which are driven by the Master Clock signal, determine the D/A conversion timing. Similarly, RX Counter A and RX Counter B determine the A/D conversion timing. In order for the switched-capacitor low-pass and bandpass filters to meet their transfer function specifications, the frequency of the clock inputs of the switched-capacitor filters must be 288 kHz. If the frequencies of the clock inputs are not 288 kHz, the filter transfer function frequencies are scaled by the ratios of the clock frequencies to 288 kHz. Thus, to obtain the specified filter responses, the combination of Master Clock frequency and TX Counter A and RX Counter A values must yield 288-kHz switched-capacitor clock signals. These 288-kHz clock signals can then be divided by the TX Counter B and RX Counter B to establish the D/A and A/D conversion timings.

TX Counter A and TX Counter B are reloaded every D/A conversion period, while RX Counter A and RX Counter B are reloaded every A/D conversion period. The TX Counter B and RX Counter B are loaded with the values in the TB and RB Registers, respectively. Via software control, the TX Counter A can be loaded with either the TA Register, the TA Register less the TA' Register, or the TA Register plus the TA' Register. By selecting the TA Register less the TA' Register option, the upcoming conversion timing will occur earlier by an amount of time that equals TA' times the signal period of the Master Clock. By selecting the TA Register plus the TA' Register option, the upcoming conversion timing will occur later by an amount of time that equals TA' times the signal period of the Master Clock. Thus, the D/A conversion timing can be advanced or retarded. An identical ability to alter the A/D conversion timing is provided. In this case, however, the RX Counter A can be programmed via software control with the RA Register, the RA Register less the RA' Register, or the RA Register plus the RA' Register.

The ability to advance or retard conversion timing is particularly useful for modem applications. This feature allows controlled changes in the A/D and D/A conversion timing. This feature can be used to enhance signal-to-noise performance, to perform frequency-tracking functions, and to generate nonstandard modem frequencies.

If the transmit and receive sections are configured to be synchronous (see WORD/$\overline{\text{BYTE}}$ pin description), then both the low-pass and bandpass switched-capacitor filter clocks are derived from TX Counter A. Also, both the D/A and A/D conversion timing are derived from the TX Counter A and TX Counter B. When the transmit and receive sections are configured to be synchronous, the RX Counter A, RX Counter B, RA Register, RA' Register, and RB Registers are not used.

AIC DR or DX word bit pattern



AIC DX data word format section

d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d2	d1	d0	COMMENTS
primary DX serial communication protocol															
← d15 (MSB) through d2 go to the D/A converter register →													0	0	The TX and RX Counter A's are loaded with the TA and RA register values. The TX and RX Counter B's are loaded with TB and RB register values.
← d15 (MSB) through d2 go to the D/A converter register →													0	1	The TX and RX Counter A's are loaded with the TA + TA' and RA + RA' register values. The TX and RX Counter B's are loaded with the TB and RB register values. NOTE: d1 = 0, d0 = 1 will cause the next D/A and A/D conversion periods to be changed by the addition of TA' and RA' Master Clock cycles, in which TA' and RA' can be positive or negative or zero. Please refer to Table 1. AIC Responses to Improper Conditions.
← d15 (MSB) through d2 go to the D/A converter register →													1	0	The TX and RX Counter A's are loaded with the TA − TA' and RA − RA' register values. The TX and RX Counter B's are loaded with the TB and RB register values. NOTE: d1 = 1, d0 = 0 will cause the next D/A and A/D conversion periods to be changed by the subtraction of TA' and RA' Master Clock cycles, in which TA' and RA' can be positive or negative or zero. Please refer to Table 1. AIC Responses to Improper Conditions.
← d15 (MSB) through d2 go to the D/A converter register →													1	1	The TX and RX Counter A's are loaded with the TA and RA register values. The TX and RX Counter B's are loaded with the TB and RB register values. After a delay of four Shift Clock cycles, a secondary transmission will immediately follow to program the AIC to operate in the desired configuration.

NOTE: Setting the two least significant bits to 1 in the normal transmission of DAC information (Primary Communications) to the AIC will initiate Secondary Communications upon completion of the Primary Communications.

Upon completion of the Primary Communication, $\overline{FSX}$ will remain high for four SHIFT CLOCK cycles and will then go low and initiate the Secondary Communication. The timing specifications for the Primary and Secondary Communications are identical. In this manner, the Secondary Communication, if initiated, is interleaved between successive Primary Communications. This interleaving prevents the Secondary Communication from interfering with the Primary Communications and DAC timing, thus preventing the AIC from skipping a DAC output. It is important to note that in the synchronous mode, $\overline{FSR}$ will not be asserted during Secondary Communications.

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secondary DX serial communication protocol

x x | ← to TA register → | x x | ← to RA register → | 0 0	d13 and d6 are MSBs (unsigned binary)
x | ← to TA′ register → | x | ← to RA′ register → | 0 1	d14 and d7 are 2's complement sign bits
x | ← to TB register → | x | ← to RB register → | 1 0	d14 and d7 are MSBs (unsigned binary)
x x x x x x x x d7 d6 d5 d4 d3 d2 1 1 | ← CONTROL REGISTER → |	d2 = 0/1 deletes/inserts the bandpass filter d3 = 0/1 disables/enables the loopback function d4 = 0/1 disables/enables the AUX IN+ and AUX IN− pins d5 = 0/1 asynchronous/synchronous transmit and receive sections d6 = 0/1 gain control bits (see Gain Control Section) d7 = 0/1 gain control bits (see Gain Control Section)

reset function

A reset function is provided to initiate serial communications between the AIC and DSP. The reset function will initialize all AIC registers, including the control register. After power has been applied to the AIC, a negative-going pulse on the $\overline{\text{RESET}}$ pin will initialize the AIC registers to provide an 8-kHz A/D and D/A conversion rate for a 5.184 MHz master clock input signal. The AIC, excepting the CONTROL register, will be initialized as follows (see AIC DX Data Word Format section):

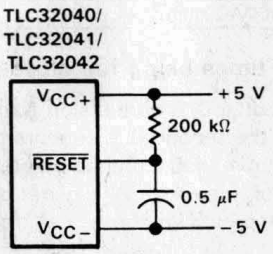
REGISTER	INITIALIZED REGISTER VALUE (HEX)
TA	9
TA′	1
TB	24
RA	9
RA′	1
RB	24

The CONTROL register bits will be reset as follows (see AIC DX Data Word Format section):

d7 = 1, d6 = 1, d5 = 1, d4 = 0, d3 = 0, d2 = 1

This initialization allows normal serial port communications to occur between AIC and DSP. If the transmit and receive sections are configured to operate synchronously and the user wishes to program different conversion rates, only the TA, TA′, and TB register need to be programmed, since both transmit and receive timing are synchronously derived from these registers (see the Pin Descriptions and AIC DX Word Format sections).

The circuit shown below will provide a reset on power-up when power is applied in the sequence given under Power-Up Sequence. The circuit depends on the power supplies' reaching their recommended values a minimum of 800 ns before the capacitor charges to 0.8 V above DGTL GND.



power-up sequence

To ensure proper operation of the AIC, and as a safeguard against latch-up, it is recommmended that a Schottky diode with a forward voltage less than or equal to 0.4 V be connected from V_{CC-} to ANLG GND (see Figure 17). In the absence of such a diode, power should be applied in the following sequence: ANLG GND and DGTL GND, V_{CC-}, then V_{CC+} and V_{DD}. Also, no input signal should be applied until after power-up.

AIC responses to improper conditions

The AIC has provisions for responding to improper conditions. These improper conditions and the response of the AIC to these conditions are presented in Table 1 below.

AIC register constraints

The following constraints are placed on the contents of the AIC registers:

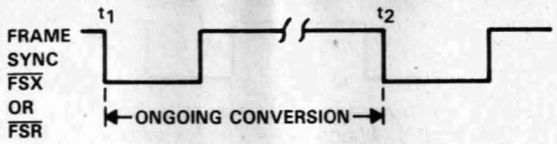
1. TA register must be ≥ 4 in word mode (WORD/$\overline{\text{BYTE}}$ = High).
2. TA register must be ≥ 5 in byte mode (WORD/$\overline{\text{BYTE}}$ = Low).
3. TA′ register can be either positive, negative, or zero.
4. RA register must be ≥ 4 in word mode (WORD/$\overline{\text{BYTE}}$ = High).
5. RA register must be ≥ 5 in byte mode (WORD/$\overline{\text{BYTE}}$ = Low).
6. RA′ register can be either positive, negative, or zero.
7. (TA register ± TA′ register) must be > 1.
8. (RA register ± RA′ register) must be > 1.
9. TB register must be > 1.

TABLE 1. AIC RESPONSES TO IMPROPER CONDITIONS

IMPROPER CONDITION	AIC RESPONSE
TA register + TA′ register = 0 or 1 TA register − TA′ register = 0 or 1	Reprogram TX Counter A with TA register value
TA register + TA′ register < 0	MODULO 64 arithmetic is used to ensure that a positive value is loaded into the TX Counter A, i.e., TA register + TA′ register + 40 HEX is loaded into TX Counter A.
RA register + RA′ register = 0 or 1 RA register − RA′ register = 0 or 1	Reprogram RX Counter A with RA register value
RA register + RA′ register = 0 or 1	MODULO 64 arithmetic is used to ensure that a positive value is loaded into RX Counter A, i.e., RA register + RA′ register + 40 HEX is loaded into RX Counter A.
TA register = 0 or 1 RA register = 0 or 1	AIC is shut down.
TA register < 4 in word mode TA register < 5 in byte mode RA register < 4 in word mode RA register < 5 in byte mode	The AIC serial port no longer operates.
TB register = 0 or 1	Reprogram TB register with 24 HEX
RB register = 0 or 1	Reprogram RB register with 24 HEX
AIC and DSP cannot communicate	Hold last DAC output

improper operation due to conversion times being too close together

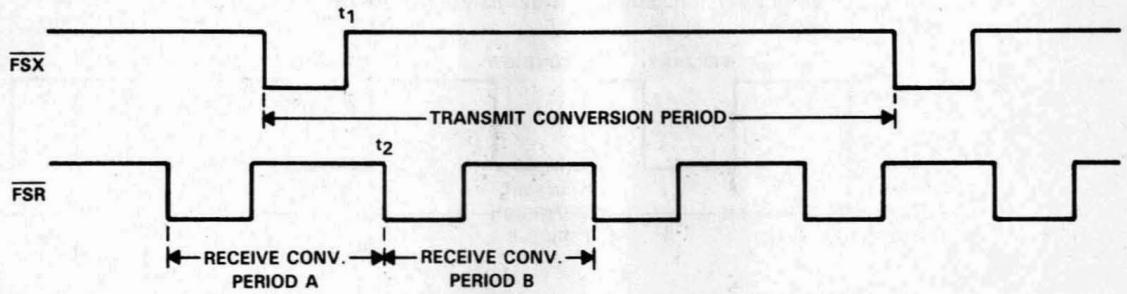
If the difference between two successive D/A conversion frame syncs is less that 1/19.2 kHz, the AIC operates improperly. In this situation, the second D/A conversion frame sync occurs too quickly and there is not enough time for the ongoing conversion to be completed. This situation can occur if the A and B registers are improperly programmed or if the A + A′ register or A − A′ register result is too small. When incrementally adjusting the conversion period via the A + A′ register options, the designer should be very careful not to violate this requirement (see following diagram).



$t_2 - t_1 \geq 1/19.2$ kHz

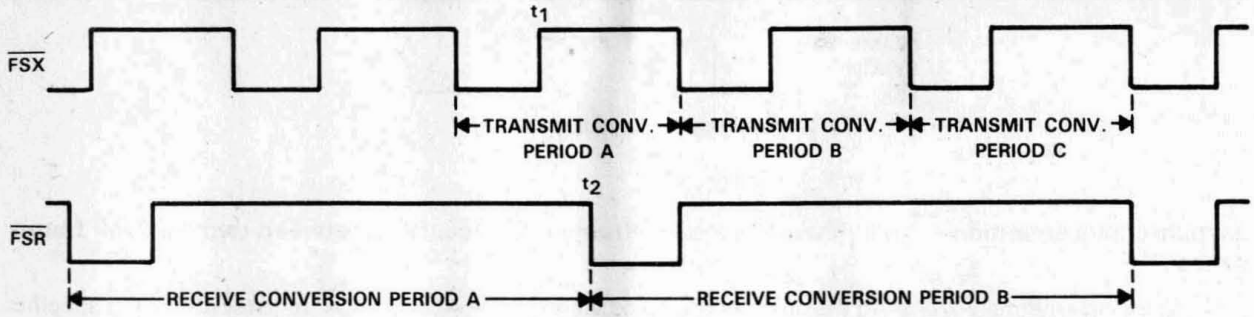
asynchronous operation — more than one receive frame sync occurring between two transmit frame syncs

When incrementally adjusting the conversion period via the A + A′ or A − A′ register options, a specific protocol is followed. The command to use the incremental conversion period adjust option is sent to the AIC during a $\overline{FSX}$ frame sync. The ongoing conversion period is then adjusted. However, either Receive Conversion Period A or B may be adjusted. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. Therefore, if there is sufficient time between t1 and t2, the receive conversion period adjustment will be performed during Receive Conversion Period A. Otherwise, the adjustment will be performed during Receive Conversion Period B. The adjustment command only adjusts one transmit conversion period and one receive conversion period. To adjust another pair of transmit and receive conversion periods, another command must be issued during a subsequent $\overline{FSX}$ frame (see figure below).



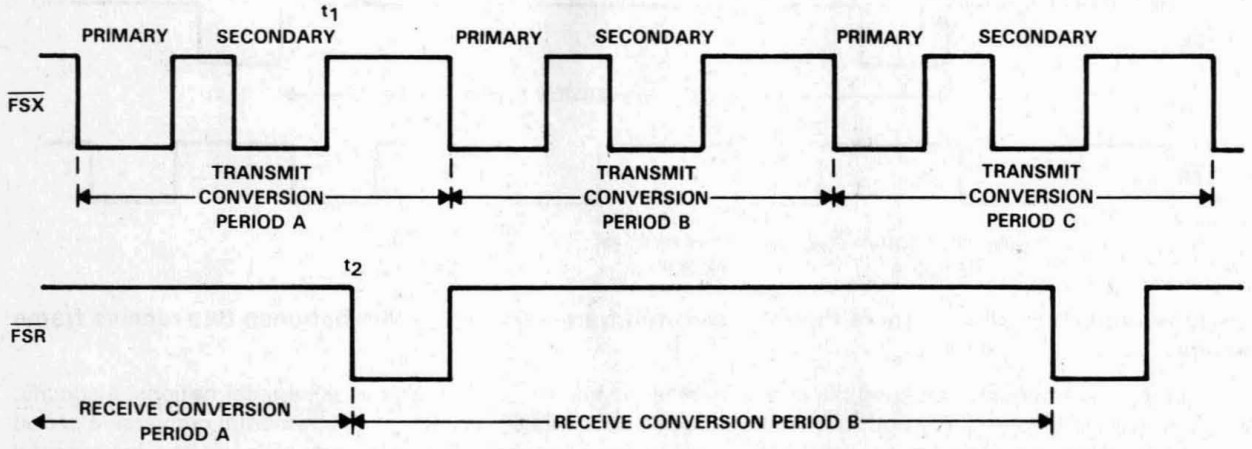
asynchronous operation — more than one transmit frame sync occurring between two receive frame syncs

When incrementally adjusting the conversion period via the A + A′ or A − A′ register options, a specific protocol is followed. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. The command to use the incremental conversion period adjust options is sent to the AIC during a $\overline{FSX}$ frame sync. The ongoing transmit conversion period is then adjusted. However, three possibilities exist for the receive conversion period adjustment in the diagram as shown in the following figure. If the adjustment command is issued during Transmit Conversion Period A, Receive Conversion Period A will be adjusted if there is sufficient time between t1 and t2. Or, if there is not sufficient time between t1 and t2, Receive Conversion Period B will be adjusted. Or, the receive portion of an adjustment command may be ignored if the adjustment command is sent during a receive conversion period, which is already being or will be adjusted due to a prior adjustment command. For example, if adjustment commands are issued during Transmit Conversion Periods A, B, and C, the first two commands may cause Receive Conversion Periods A and B to be adjusted, while the third receive adjustment command is ignored. The third adjustment command is ignored since it was issued during Receive Conversion Period B, which already will be adjusted via the Transmit Conversion Period B adjustment command.



asynchronous operation — more than one set of primary and secondary DX serial communication occurring between two receive frame sync (see AIC DX Data Word Format section)

The TA, TA′, TB, and control register information that is transmitted in the secondary communications is always accepted and is applied during the ongoing transmit conversion period. If there is sufficient time between t1 and t2, the TA, RA′, and RB register information, which is sent during Transmit Conversion Period A, will be applied to Receive Conversion Period A. Otherwise, this information will be applied during Receive Conversion Period B. If RA, RA′, and RB register information has already been received and is being applied during an ongoing conversion period, any subsequent RA, RA′, or RB information that is received during this receive conversion period will be disregarded (see diagram below).



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC+} (see Note 1)	−0.3 V to 15 V
Supply voltage range, V_{DD}	−0.3 V to 15 V
Output voltage range, V_O	−0.3 V to 15 V
Input voltage range, V_I	−0.3 V to 15 V
Digital ground voltage range	−0.3 V to 15 V
Operating free-air temperature range: TLC32040C, TLC32041C, TLC32042C	0°C to 70°C
TLC32040I, TLC32041I, TLC32042I	−40°C to 85°C
Storage temperature range	−40°C to 125°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package	260°C

NOTE 1: Voltage values for maximum ratings are with respect to VCC−.

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} (see Note 2)		4.75	5	5.25	V
Supply voltage, V_{CC-} (see Note 2)		−4.75	−5	−5.25	V
Digital supply voltage, V_{DD} (see Note 2)		4.75	5	5.25	V
Digital ground voltage with respect to ANLG GND, DGTL GND			0		V
Reference input voltage, $V_{ref(ext)}$ (see Note 2)		2		4	V
High-level input voltage, V_{IH}		2		V_{DD}+0.3	V
Low-level input voltage, V_{IL} (see Note 3)		−0.3		0.8	V
Load resistance at OUT+ and/or OUT−, R_L		300			Ω
Load capacitance at OUT+ and/or OUT−, C_L				100	pF
MSTR CLK frequency (see Note 4)		0.075	5	10.368	MHz
Analog input amplifier common mode input voltage (see Note 5)				±1.5	V
A/D or D/A conversion rate				20	kHz
Operating free-air temperature, T_A	TLC32040C, TLC32041C, TLC32042C	0		70	°C
	TLC32040I, TLC32041I, TLC32042I	−40		85	

NOTES: 2. Voltages at analog inputs and outputs, REF, V_{CC+}, and V_{CC-}, are with respect to the ANLG GND terminal. Voltages at digital inputs and outputs and V_{DD} are with respect to the DGTL GND terminal.

3. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels and temperature only.

4. The bandpass and low-pass switched-capacitor filter response specifications apply only when the switched-capacitor clock frequency is 288 kHz. For switched-capacitor filter clocks at frequencies other than 288 kHz, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 288 kHz.

5. This range applies when (IN+ − IN−) or (AUX IN+ − AUX IN−) equals ±6 V.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (unless otherwise noted)

total device, MSTR CLK frequency = 5.184 MHz, outputs not loaded

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 4.75 V, I_{OH} = −300 μA	2.4			V
V_{OL}	Low-level output voltage		V_{DD} = 4.75 V, I_{OL} = 2 mA			0.4	V
I_{CC+}	Supply current from V_{CC+}	TLC3204–C				35	mA
		TLC3204–I				40	
I_{CC-}	Supply current from V_{CC-}	TLC3204–C				−35	mA
		TLC3204–I				−40	
I_{DD}	Supply current from V_{DD}		$f_{MSTR\ CLK}$ = 5.184 MHz			7	mA
V_{ref}	Internal reference output voltage			3		3.3	V
αV_{ref}	Temperature coefficient of internal reference voltage				200		ppm/°C
r_o	Output resistance at REF				100		kΩ

receive amplifier input

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	A/D converter offset error (filters bypassed)			25	65	mV
	A/D converter offset error (filters in)			25	65	mV
CMRR	Common-mode rejection ratio at IN+, IN−, or AUX IN+, AUX IN−	See Note 6		55		dB
r_I	Input resistance at IN+, IN− or AUX IN+, AUX IN−, REF			100		kΩ

transmit filter output

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OO}	Output offset voltage at OUT+ or OUT− (single-ended relative to ANLG GND)			15	75	mV
V_{OM}	Maximum peak output voltage swing across R_L at OUT+ or OUT− (single-ended)	$R_L \geq 300\ \Omega$, Offset voltage = 0	±3			V
V_{OM}	Maximum peak output voltage swing between OUT+ and OUT− (differential output)	$R_L \geq 600\ \Omega$	±6			V

†All typical values are at T_A = 25°C.
NOTE 6: The test condition is a 0-dBm, 1-kHz input signal with an 8-kHz conversion rate.

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electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (unless otherwise noted) (continued)

system distortion specifications, SCF clock frequency = 288 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Attenuation of second harmonic of A/D input signal	single-ended	V_{in} = −0.5 dB to −24 dB referred to V_{ref}, See Note 7		70		dB
	differential		62	70		
Attenuation of third and higher harmonics of A/D input signal	single-ended	V_{in} = −0.5 dB to −24 dB referred to V_{ref}, See Note 7		65		dB
	differential		57	65		
Attenuation of second harmonic of D/A input signal	single-ended	V_{in} = −0 dB to −24 dB referred to V_{ref}, See Note 7		70		dB
	differential		62	70		
Attenuation of third and higher harmonics of D/A input signal	single-ended	V_{in} = −0 dB to −24 dB referred to V_{ref}, See Note 7		65		dB
	differential		57	65		

A/D channel signal-to-distortion ratio

PARAMETER	TEST CONDITIONS (see Note 7)	A_V = 1‡		A_V = 2‡		A_V = 4‡		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
A/D channel signal-to-distortion ratio	V_{in} = −6 dB to −0.1 dB	58		>58§		>58§		dB
	V_{in} = −12 dB to −6 dB	58		58		>58§		
	V_{in} = −18 dB to −12 dB	56		58		58		
	V_{in} = −24 dB to −18 dB	50		56		58		
	V_{in} = −30 dB to −24 dB	44		50		56		
	V_{in} = −36 dB to −30 dB	38		44		50		
	V_{in} = −42 dB to −36 dB	32		38		44		
	V_{in} = −48 dB to −42 dB	26		32		38		
	V_{in} = −54 dB to −48 dB	20		26		32		

D/A channel signal-to-distortion ratio

PARAMETER	TEST CONDITIONS (see Note 7)	MIN	MAX	UNIT
D/A channel signal-to-distortion ratio	V_{in} = −6 dB to 0 dB	58		dB
	V_{in} = −12 dB to −6 dB	58		
	V_{in} = −18 dB to −12 dB	56		
	V_{in} = −24 dB to −18 dB	50		
	V_{in} = −30 dB to −24 dB	44		
	V_{in} = −36 dB to −30 dB	38		
	V_{in} = −42 dB to −36 dB	32		
	V_{in} = −48 dB to −42 dB	26		
	V_{in} = −54 dB to −48 dB	20		

†All typical values are at T_A = 25°C.
‡A_V is the programmable gain of the input amplifier.
§A value > 58 is overrange and signal clipping occurs.
NOTE 7: The test condition is a 1-kHz input signal with an 8-kHz conversion rate (0 dB relative to V_{ref}). The load impedance for the DAC is 600 Ω.

gain and dynamic range

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Absolute transmit gain tracking error while transmitting into 600 Ω	−48 dB to 0 dB signal range, See Note 8		±0.05	±0.15	dB
Absolute receive gain tracking error	−48 dB to 0 dB signal range, See Note 8		±0.05	±0.15	dB
Absolute gain of the A/D channel	Signal input is a −0.5-dB, 1-kHz sinewave		0.2		dB
Absolute gain of the D/A channel	Signal input is a 0-dB, 1-kHz sinewave		−0.3		dB

†All typical values are at T_A = 25°C.
NOTE 8: Gain tracking is relative to the absolute gain at 1 kHz and 0 dB (0 dB relative to V_{ref}).

power supply rejection and crosstalk attenuation

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{CC+} or V_{CC-} supply voltage rejection ratio, receive channel	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at DR (ADC output)		30		dB
	f = 30 kHz to 50 kHz			45		
V_{CC+} or V_{CC-} supply voltage rejection ratio, transmit channel (single-ended)	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at OUT+		30		dB
	f = 30 kHz to 50 kHz			45		
Crosstalk attenuation, transmit-to-receive (single-ended)				80		dB

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

delay distortion, SCF clock frequency = 288 kHz ±2%, input (IN+ – IN–) is ±3-V sinewave

Please refer to filter response graphs for delay distortion specifications.

TLC32040 and TLC32041 bandpass filter transfer function (see curves), SCF clock frequency = 288 kHz ±2%, input (IN+ – IN–) is a ±3-V sinewave (see Note 9)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Filter Gain (see Note 10)	Input signal reference is 0 dB	f = 100 Hz		–42	dB
		f = 170 Hz		–25	
		300 Hz ≤ f ≤ 3.4 kHz	–0.5	0.5	
		f = 4 kHz		–16	
		f ≥ 4.6 kHz		–58	

TLC32042 bandpass filter transfer function (see curves), SCF clock frequency = 288 kHz ±2%, input (IN+ – IN–) is a ±3-V sinewave (see Note 9)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Filter Gain (see Note 10)	Input signal reference is 0 dB	f = 100 Hz		–27	dB
		f = 170 Hz		–2	
		300 Hz ≤ f ≤ 3.4 kHz	–0.5	0.5	
		f = 4 kHz		–16	
		f ≥ 4.6 kHz		–58	

low-pass filter transfer function, SCF clock frequency = 288 kHz ±2% (see Note 9)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Filter Gain (see Note 10)	Output signal reference is 0 dB	f ≤ 3.4 kHz	–0.5	0.5	dB
		f = 3.6 kHz		–4	
		f = 4 kHz		–30	
		f ≥ 4.4 kHz		–58	

serial port

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –300 μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4	V
I_I	Input current				±10	μA
C_I	Input capacitance			15		pF
C_O	Output capacitance			15		pF

† All typical values are at T_A = 25°C.

NOTES: 9. The above filter specifications are for a switched-capacitor filter clock range of 288 kHz ±2%. For switched-capacitor filter clocks at frequencies other than 288 kHz ±2%, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 288 kHz.

10. The filter gain outside of the passband is measured with respect to the gain at 1 kHz. The filter gain within the passband is measured with respect to the average gain within the passband. The passbands are 300 to 3400 Hz and 0 to 3400 Hz for the bandpass and lowpass filters respectively.

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V

noise (measurement includes low-pass and bandpass switched-capacitor filters)

PARAMETER		TEST CONDITIONS	TYP†	MAX	UNIT
Transmit noise	single-ended	DX input = 00000000000000, constant input code	200		μV rms
	differential		300	500	μV rms
			20		dBrnc0
Receive noise (see Note 11)		Inputs grounded, gain = 1	300	475	μV rms
			20		dBrnc0

timing requirements

serial port recommended input signals

PARAMETER		MIN	MAX	UNIT
$t_{c(MCLK)}$	Master clock cycle time	95		ns
$t_{r(MCLK)}$	Master clock rise time		10	ns
$t_{f(MCLK)}$	Master clock fall time		10	ns
	Master clock duty cycle	42%	58%	
	$\overline{RESET}$ pulse duration (see Note 12)	800		ns
$t_{su(DX)}$	DX setup time before SCLK↓	20		ns
$t_{h(DX)}$	DX hold time after SCLK↓	$t_{c(SCLK)}/4$		ns

NOTES: 11. This noise is referred to the input with a buffer gain of one. If the buffer gain is two or four, the noise figure will be correspondingly reduced. The noise is computed by statistically evaluating the digital output of the A/D converter.

12. $\overline{RESET}$ pulse duration is the amount of time that the reset pin is held below 0.8 V after the power supplies have reached their recommended values.

serial port—AIC output signals, C_L = 30 pF for SHIFT CLK output, C_L = 15 pF for all other outputs

PARAMETER		MIN	TYP†	MAX	UNIT
$t_{c(SCLK)}$	Shift clock (SCLK) cycle time	380			ns
$t_{f(SCLK)}$	Shift clock (SCLK) fall time		3	8	ns
$t_{r(SCLK)}$	Shift clock (SCLK) rise time		3	8	ns
	Shift clock (SCLK) duty cycle	45		55	%
$t_{d(CH-FL)}$	Delay from SCLK↑ to $\overline{FSR}/\overline{FSX}/\overline{FSD}$↓		30		ns
$t_{d(CH-FH)}$	Delay from SCLK↑ to $\overline{FSR}/\overline{FSX}/\overline{FSD}$↑		35	90	ns
$t_{d(CH-DR)}$	DR valid after SCLK↑			90	ns
$t_{dw(CH-EL)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↓ in word mode			90	ns
$t_{dw(CH-EH)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↑ in word mode			90	ns
$t_{f(EODX)}$	$\overline{EODX}$ fall time		2	8	ns
$t_{f(EODR)}$	$\overline{EODR}$ fall time		2	8	ns
$t_{db(CH-EL)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↓ in byte mode			90	ns
$t_{db(CH-EH)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↑ in byte mode			90	ns
$t_{d(MH-SL)}$	Delay from MSTR CLK↑ to SCLK↓		65	170	ns
$t_{d(MH-SH)}$	Delay from MSTR CLK↑ to SCLK↑		65	170	ns

†Typical values are at T_A = 25°C.

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (continued)

serial port — AIC output signals

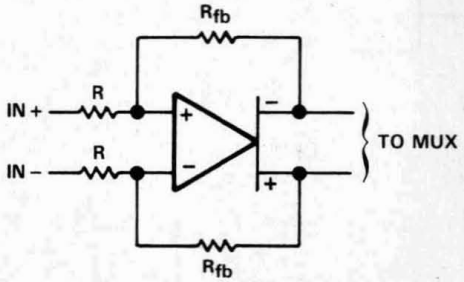
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{c(SCLK)}$	Shift clock (SCLK) cycle time		380			ns
$t_{f(SCLK)}$	Shift clock (SCLK) fall time				50	ns
$t_{r(SCLK)}$	Shift clock (SCLK) rise time				50	ns
	Shift clock (SCLK) duty cycle		45		55	%
$t_{d(CH-FL)}$	Delay from SCLK↑ to $\overline{FSR}/\overline{FSX}$↓	C_L = 50 pF			52	ns
$t_{d(CH-FH)}$	Delay from SCLK↑ to $\overline{FSR}/\overline{FSX}$↑	C_L = 50 pF			52	ns
$t_{d(CH-DR)}$	DR valid after SCLK↑				90	ns
$t_{dw(CH-EL)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↓ in word mode				90	ns
$t_{dw(CH-EH)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↑ in word mode				90	ns
$t_{f(EODX)}$	$\overline{EODX}$ fall time				15	ns
$t_{f(EODR)}$	$\overline{EODR}$ fall time				15	ns
$t_{db(CH-EL)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↓ in byte mode				100	ns
$t_{db(CH-EH)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↑ in byte mode				100	ns
$t_{d(MH-SL)}$	Delay from MSTR CLK↑ to SCLK↓			65		ns
$t_{d(MH-SH)}$	Delay from MSTR CLK↑ to SCLK↑			65		ns

†Typical values are at T_A = 25°C.

**TABLE 2. GAIN CONTROL TABLE
(ANALOG INPUT SIGNAL REQUIRED FOR FULL-SCALE A/D CONVERSION)**

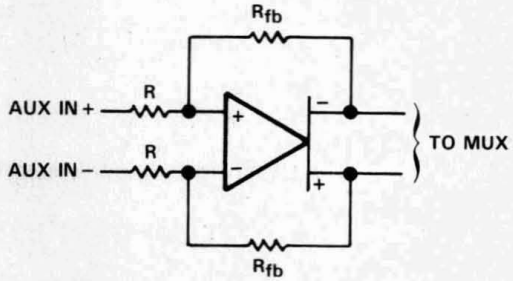
INPUT CONFIGURATIONS	CONTROL REGISTER BITS		ANALOG INPUT‡	A/D CONVERSION RESULT
	d6	d7		
Differential configuration Analog input = IN+ − IN−	1	1	±6 V	full-scale
	0	0		
= AUX IN+ − AUX IN−	1	0	±3 V	full-scale
	0	1	±1.5 V	full-scale
Single-ended configuration Analog input = IN+ − ANLG GND	1	1	±3 V	half-scale
	0	0		
= AUX IN+ − ANLG GND	1	0	±3 V	full-scale
	0	1	±1.5 V	full-scale

‡In this example, V_{ref} is assumed to be 3 V. In order to minimize distortion, it is recommended that the analog input not exceed 0.1 dB below full scale.



R_{fb} = R for d6 = 1, d7 = 1
d6 = 0, d7 = 0
R_{fb} = 2R for d6 = 1, d7 = 0
R_{fb} = 4R for d6 = 0, d7 = 1

FIGURE 1. IN+ AND IN− GAIN CONTROL CIRCUITRY



R_{fb} = R for d6 = 1, d7 = 1
d6 = 0, d7 = 0
R_{fb} = 2R for d6 = 1, d7 = 0
R_{fb} = 4R for d6 = 0, d7 = 1

FIGURE 2. AUX IN+ AND AUX IN− GAIN CONTROL CIRCUITRY

sin x/x correction section

The AIC does not have sin x/x correction circuitry after the digital-to-analog converter. Sin x/x correction can be accomplished easily and efficiently in digital signal processor (DSP) software. Excellent correction accuracy can be achieved to a band edge of 3000 Hz by using a first-order digital correction filter. The results, which are shown below, are typical of the numerical correction accuracy that can be achieved for sample rates of interest. The filter requires only seven instruction cycles per sample on the TMS320 DSPs. With a 200-ns instruction cycle, nine instructions per sample represents an overhead factor of 1.4% and 1.7% for sampling rates of 8000 Hz and 9600 Hz, respectively. This correction will add a slight amount of group delay at the upper edge of the 300—3000-Hz band.

sin x/x roll-off for a zero-order hold function

The sin x/x roll-off for the AIC DAC zero-order hold function at a band-edge frequency of 3000 Hz for the various sampling rates is shown in the table below.

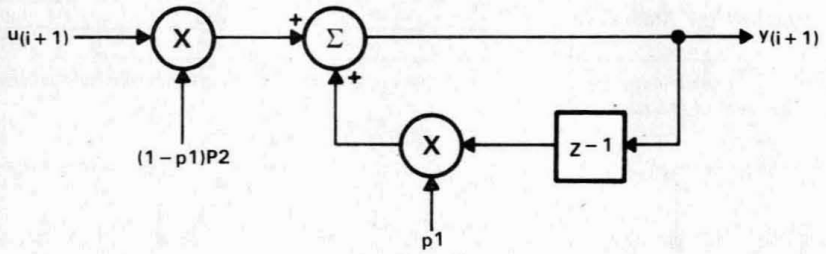
TABLE 3. sin x/x ROLL-OFF

f_s (Hz)	$20 \log \frac{\sin \pi f/f_s}{\pi f/f_s}$ (f = 3000 Hz) (dB)
7200	−2.64
8000	−2.11
9600	−1.44
14400	−0.63
19200	−0.35

Note that the actual AIC sin x/x roll-off will be slightly less than the above figures, because the AIC has less than a 100-% duty cycle hold interval.

correction filter

To compensate for the sin x/x roll-off of the AIC, a first-order correction filter shown below, is recommended.



The difference equation for this correction filter is:

$$y_{i+1} = p2(1-p1)\,(u_{i+1}) + p1\,y_i$$

where the constant p1 determines the pole locations.

The resulting squared magnitude transfer function is:

$$|H(f)|^2 = \frac{p2^2\,(1-p1)^2}{1 - 2p1\cos(2\pi f/f_S) + p1^2}$$

correction results

Table 4 below shows the optimum p values and the corresponding correction results for 8000-Hz and 9600-Hz sampling rates.

TABLE 4

f (Hz)	ERROR (dB) f_s = 8000 Hz p1 = −0.14813 p2 = 0.9888	ERROR (dB) f_s = 9600 Hz p1 = −0.1307 p2 = 0.9951
300	−0.099	−0.043
600	−0.089	−0.043
900	−0.054	0
1200	−0.002	0
1500	0.041	0
1800	0.079	0.043
2100	0.100	0.043
2400	0.091	0.043
2700	−0.043	0
3000	−0.102	−0.043

TMS320 software requirements

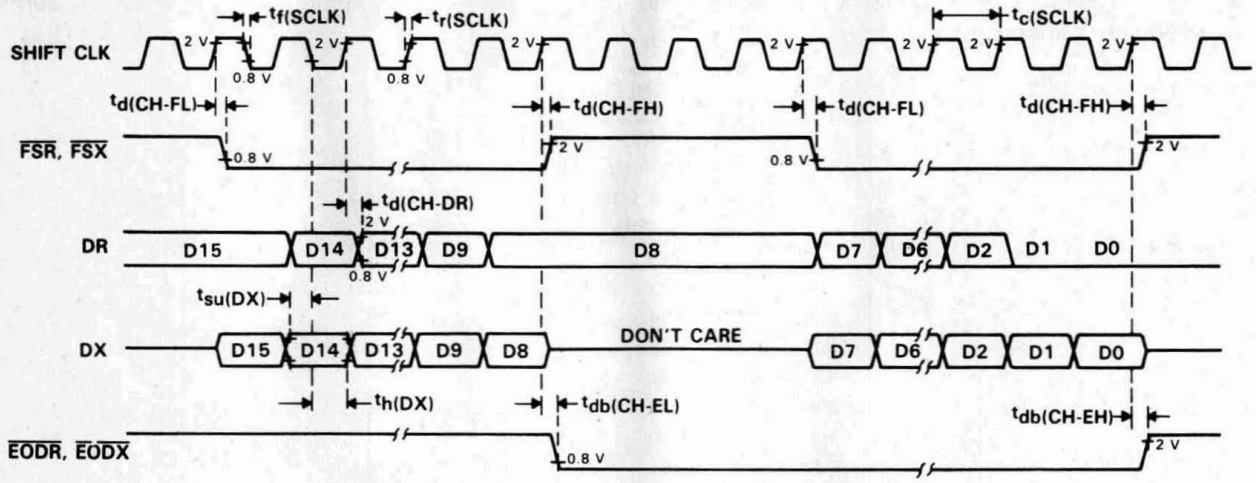
The digital correction filter equation can be written in state variable form as follows:

$$Y = k1Y + k2U$$

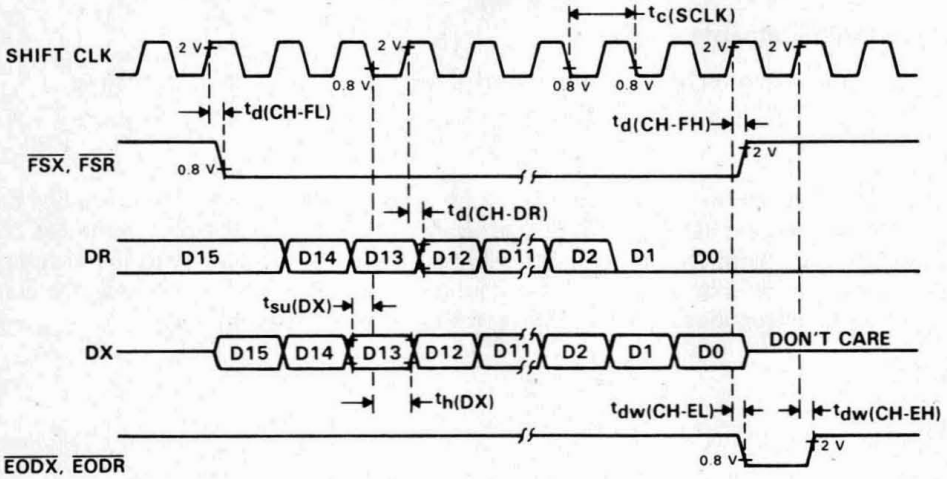
where k1 equals p1 (from the preceding page), k2 equals (1 − p1)p2 (from the preceding page), Y is the filter state, and U is the next I/O sample. The coefficients k1 and k2 must be represented as 16-bit integers. The SACH instruction (with the proper shift) will yield the correct result. With the assumption that the TMS320 processor page pointer and memory configuration are properly initialized, the equation can be executed in seven instructions or seven cycles with the following program:

```
ZAC
LT K2
MPY U
LTA K1
MPY Y
APAC
SACH (dma), (shift)
```

byte-mode timing



word-mode timing



shift-clock timing

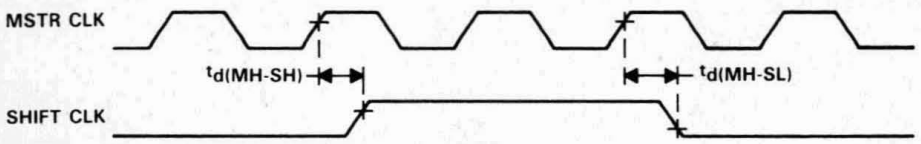


FIGURE 3. SERIAL PORT TIMING

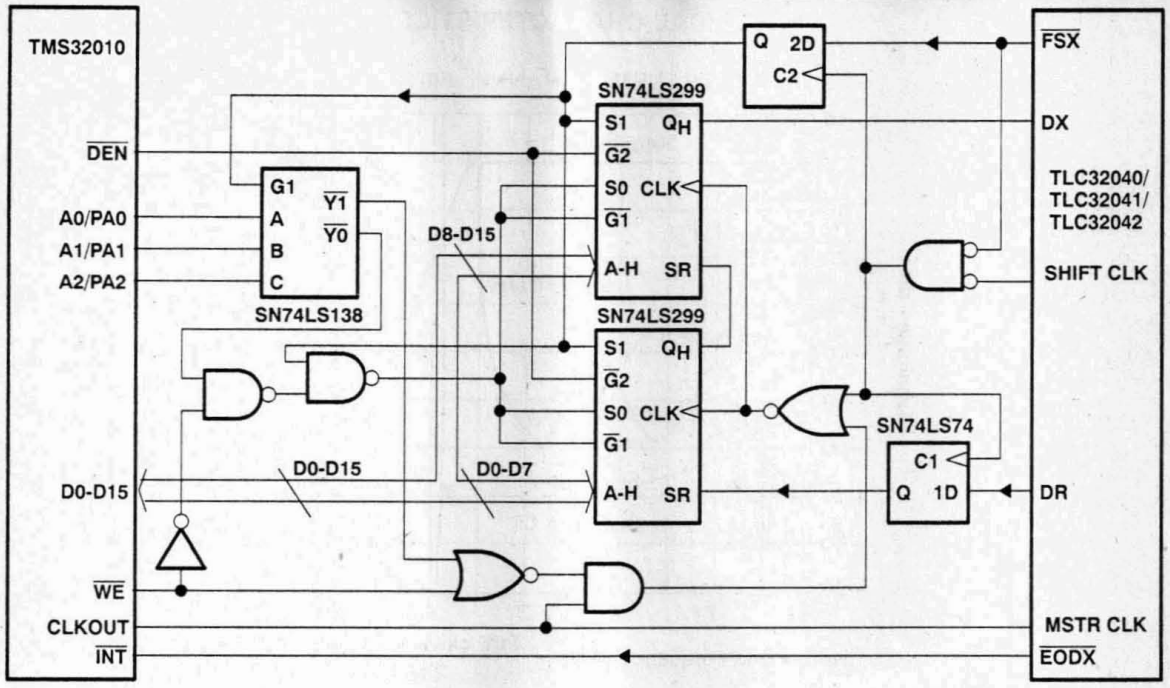
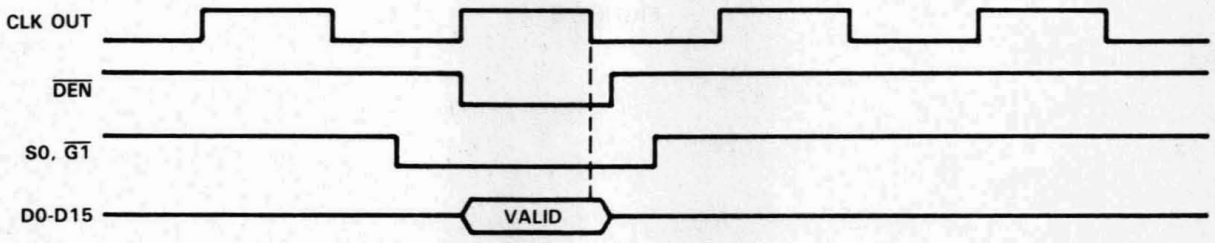


FIGURE 4. TMS32010-TLC32040/TLC32041/TLC32042 INTERFACE CIRCUIT

in instruction timing



out instruction timing

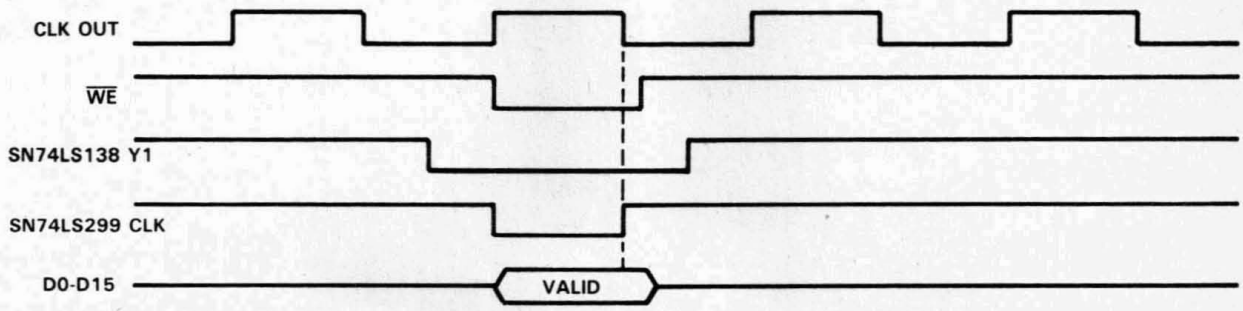
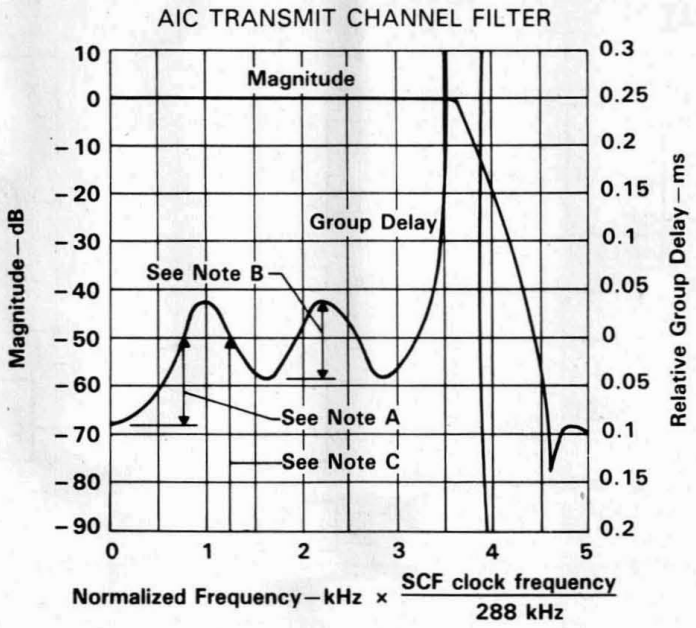


FIGURE 5. TMS32010-TLC32040/TLC32041/TLC32042 INTERFACE TIMING

TYPICAL CHARACTERISTICS

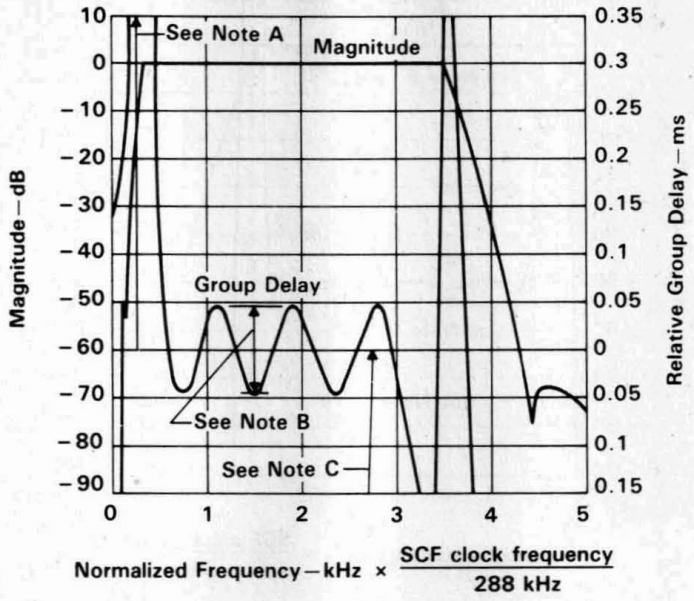


NOTES: A. Maximum relative delay (0 Hz to 600 Hz) = 125 μs.
B. Maximum relative delay (600 Hz to 3000 Hz) = ±50 μs.
C. Absolute delay (600 Hz to 3000 Hz) = 700 μs.
D. Test conditions are V_{CC+}, V_{CC-}, and V_{DD} within recommended operating conditions, SCF clock f = 288 kHz ±2%, input = ±3-V sinewave, and T_A = 25°C.

FIGURE 6

TYPICAL CHARACTERISTICS

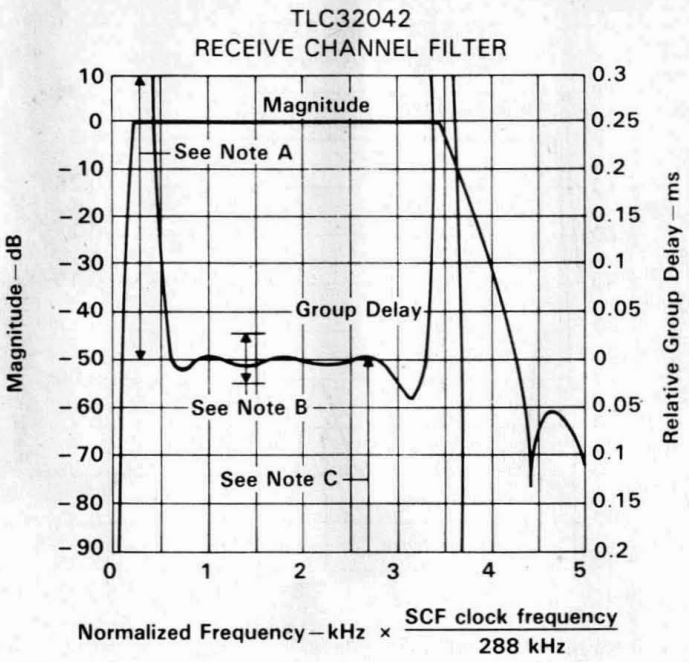
TLC32040 and TLC32041
RECEIVE CHANNEL FILTER



NOTES: A. Maximum relative delay (200 Hz to 600 Hz) = 3350 μs.
B. Maximum relative delay (600 Hz to 3000 Hz) = ±50 μs.
C. Absolute delay (600 Hz to 3000 Hz) = 1230 μs
D. Test conditions are V_{CC+}, V_{CC-}, and V_{DD} within recommended operating conditions, SCF clock f = 288 kHz ±2%, input = ±3-V sinewave, and T_A = 25°C.

FIGURE 7

TYPICAL CHARACTERISTICS



NOTES: A. Maximum relative delay (200 Hz to 600 Hz) = 3350 μs.
B. Maximum relative delay (600 Hz to 3000 Hz) = ±50 μs.
C. Absolute delay (600 Hz to 3000 Hz) = 1080 μs.
D. Test conditions are V_{CC+}, V_{CC-}, and V_{DD} within recommended operating conditions, SCF clock f = 288 kHz ±2%, input = ±3-V sinewave, and T_A = 25°C.

FIGURE 8

TYPICAL CHARACTERISTICS

A/D SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL

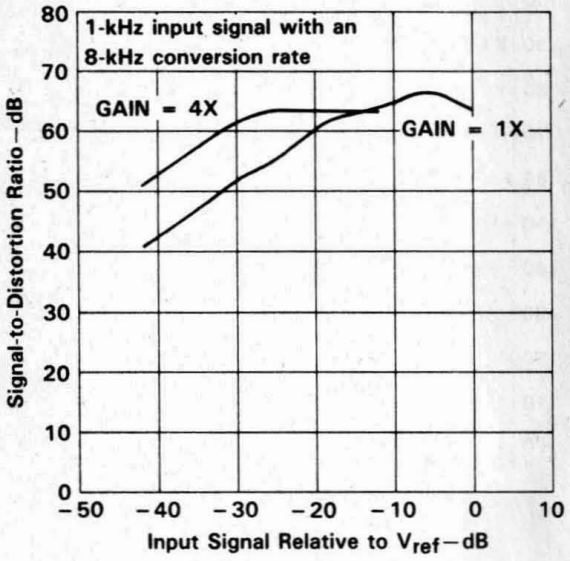


FIGURE 9

A/D GAIN TRACKING
(GAIN RELATIVE TO GAIN
AT 0 dB INPUT SIGNAL)

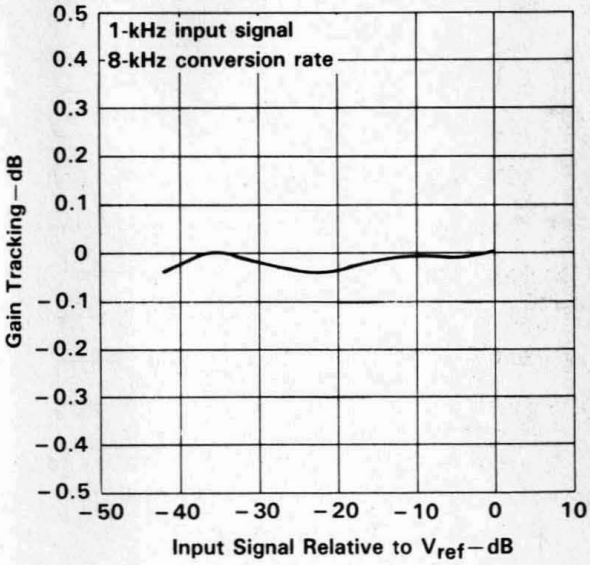


FIGURE 10

D/A CONVERTER SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL

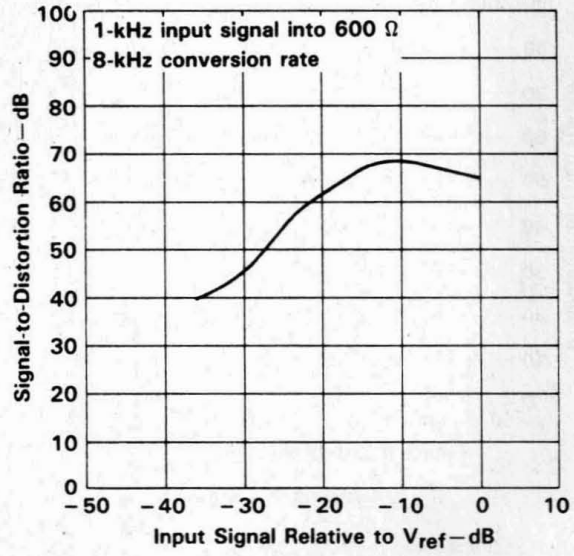


FIGURE 11

D/A GAIN TRACKING
vs
(GAIN RELATIVE TO GAIN
AT 0 dB INPUT SIGNAL)

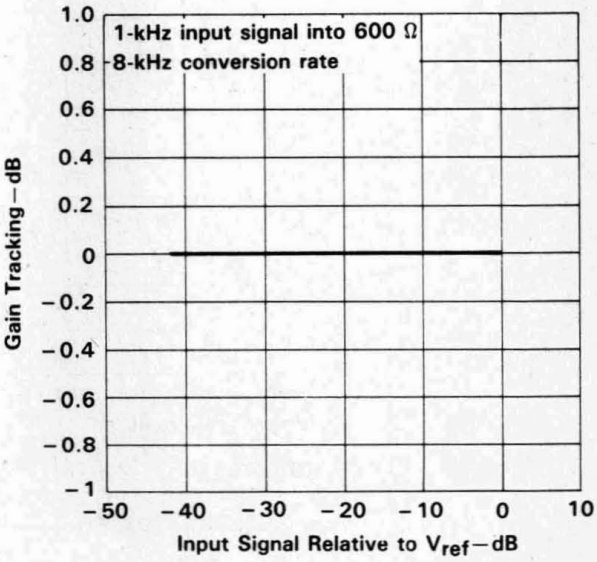


FIGURE 12

NOTE: Test conditions are V_{CC+}, V_{CC-}, and V_{DD} within recommended operating conditions set clock f = 288 kHz ± 2%, and T_A = 25°C.

TYPICAL CHARACTERISTICS

ATTENUATION OF SECOND HARMONIC OF A/D INPUT
vs
INPUT SIGNAL

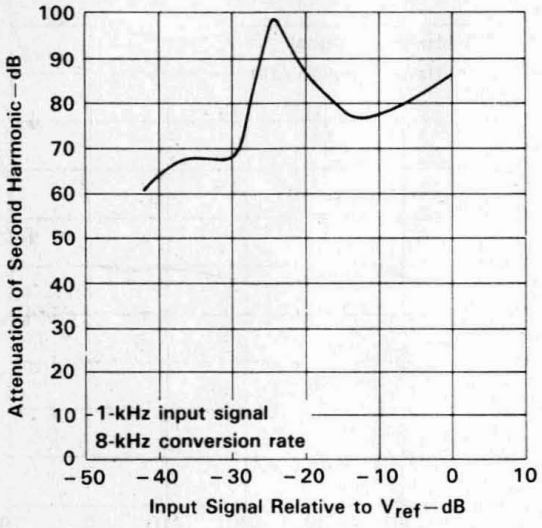


FIGURE 13

ATTENUATION OF THIRD HARMONIC OF A/D INPUT
vs
INPUT SIGNAL

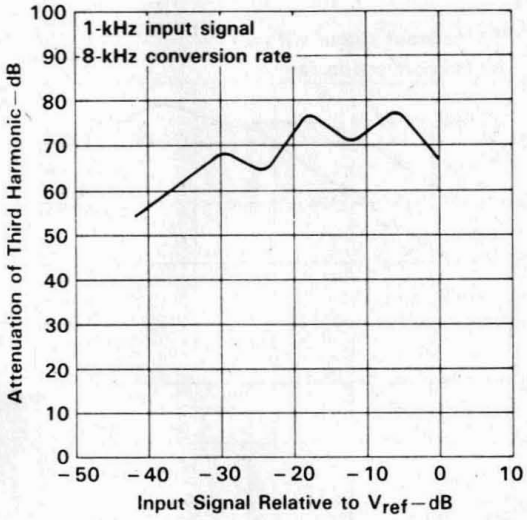


FIGURE 14

ATTENUATION OF SECOND HARMONIC OF D/A INPUT
vs
INPUT SIGNAL

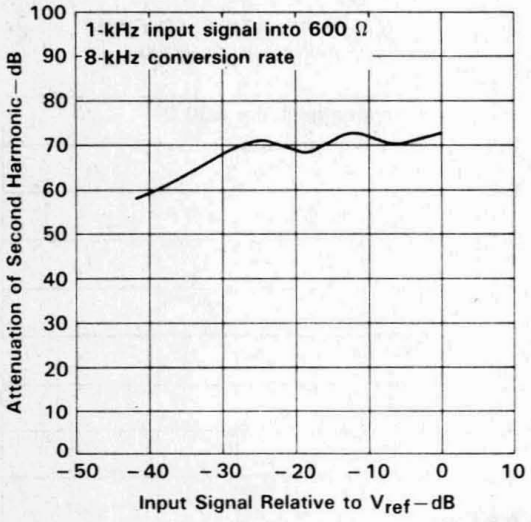


FIGURE 15

ATTENUATION OF THIRD HARMONIC OF D/A INPUT
vs
INPUT SIGNAL

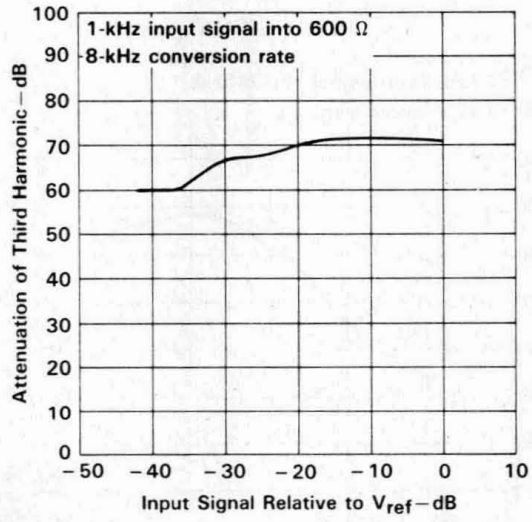
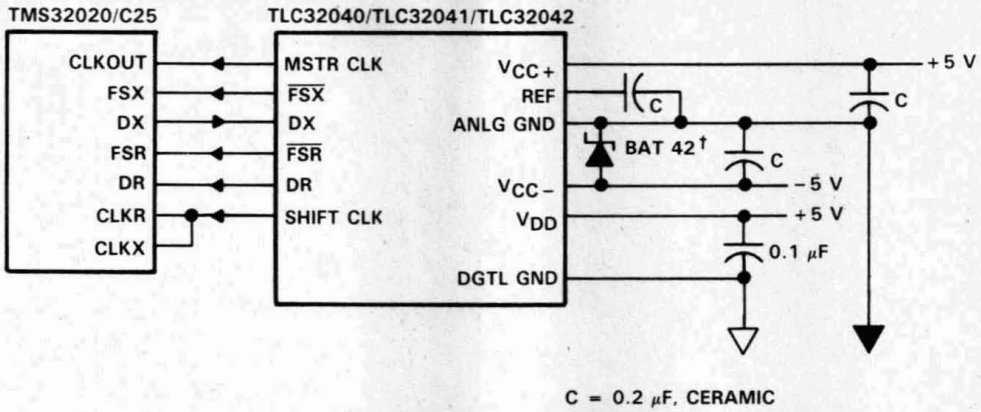


FIGURE 16

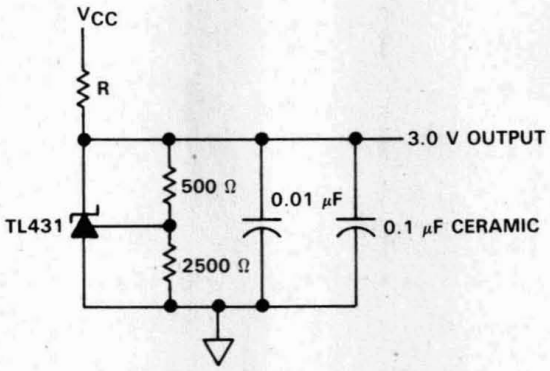
NOTE: Test conditions are V_{CC+}, V_{CC-}, and V_{DD} within recommended operating conditions set clock f = 288 kHz ±2%, and T_A = 25°C.

TYPICAL APPLICATION INFORMATION



C = 0.2 μF, CERAMIC

FIGURE 17. AIC INTERFACE TO THE TMS32020/C25 SHOWING DECOUPLING CAPACITORS AND SCHOTTKY DIODE†



FOR: V_{CC} = 12 V, R = 7200 Ω
V_{CC} = 10 V, R = 5600 Ω
V_{CC} = 5 V, R = 1600 Ω

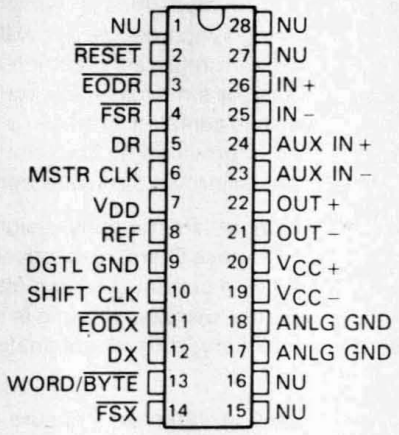
FIGURE 18. EXTERNAL REFERENCE CIRCUIT FOR TLC32041

†Thomson Semiconductors

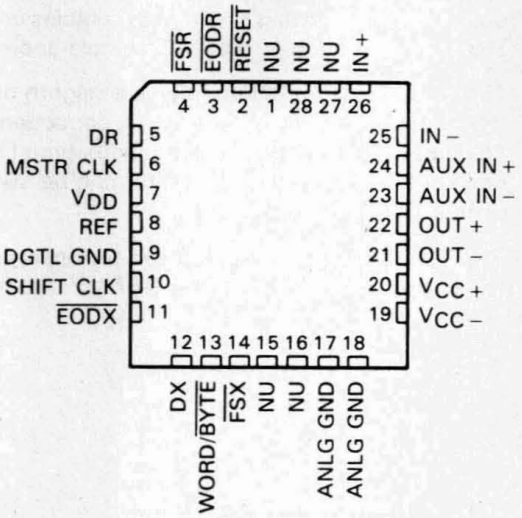
D3098, MARCH 1988—REVISED MAY 1991

- **Advanced LinCMOS™ Silicon-Gate Process Technology**
- **14-Bit Dynamic Range ADC and DAC**
- **16-Bit Dynamic Range Input with Programmable Gain**
- **Variable ADC and DAC Sampling Rate Up to 19,200 Samples per Second**
- **Switched-Capacitor Antialiasing Input Filter and Output-Reconstruction Filter**
- **Serial Port for Direct Interface to TMS320C17, TMS32020, TMS320C25, and TMS320C30 Digital Processors**
- **Synchronous or Asynchronous ADC and DAC Conversion Rates with Programmable Incremental ADC and DAC Conversion Timing Adjustments**
- **Serial Port Interface to SN74299 Serial-to-Parallel Shift Register for Parallel Interface to TMS32010, TMS320C15, or Other Digital Processors**
- **Internal Reference for Normal Operation and External Purposes, or Can Be Overridden by External Reference**
- **600-mil Wide N Package (C_L to C_L)**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NU—Nonusable; no external connection should be made to these pins. See Table 2.

description

The TLC32044 is a complete analog-to-digital and digital-to-analog input/output system on a single monolithic CMOS chip. This device integrates a bandpass switched-capacitor antialiasing input filter, a 14-bit-resolution A/D converter, four microprocessor-compatible serial port modes, a 14-bit-resolution D/A converter, and a low-pass switched-capacitor output-reconstruction filter. The device offers numerous combinations of Master Clock input frequencies and conversion/sampling rates, which can be changed via digital processor control.

Typical applications for this IC include speech encryption for digital transmission, speech recognition/storage systems, speech synthesis, modems (7.2-, 8-, 9.6-, 14.4-, and 19.2-kHz sampling rate), analog interface for digital signal processors (DSPs), industrial process control, biomedical instrumentation, acoustical signal processing, spectral analysis, data acquisition, and instrumentation recorders. Four serial modes, which allow direct interface to the TMS320C17, TMS32020, TMS320C25, and TMS320C30 digital signal

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description (continued)

processors, are provided. Also, when the transmit and receive sections of the Analog Interface Circuit (AIC) are operating synchronously, it will interface to two SN74299 serial-to-parallel shift registers. These serial-to-parallel shift registers can then interface in parallel to the TMS32010, TMS320C15, other digital signal processors, or external FIFO circuitry. Output data pulses are emitted to inform the processor that data transmission is complete or to allow the DSP to differentiate between two transmitted bytes. A flexible control scheme is provided so that the functions of the IC can be selected and adjusted coincidentally with signal processing via software control.

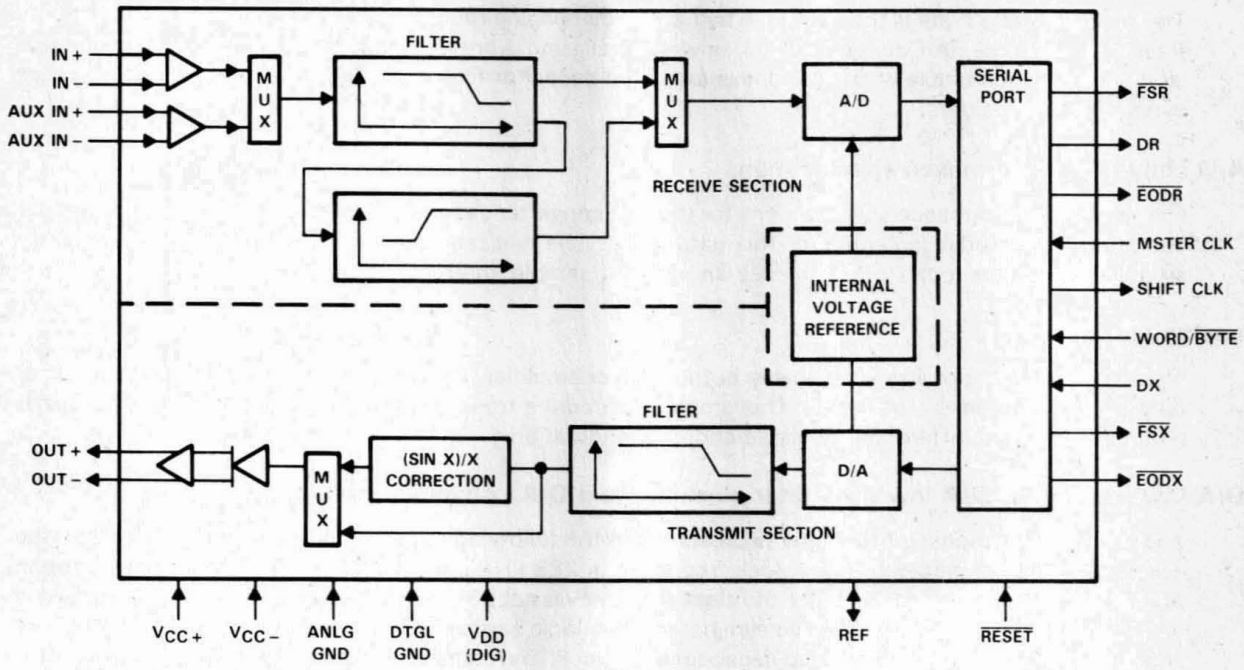
The antialiasing input filter comprises eighth-order and fourth-order CC-type (Chebyshev/elliptic transitional) low-pass and high-pass filters, respectively. The input filter is implemented in switched-capacitor technology and is preceded by a continuous time filter to eliminate any possibility of aliasing caused by sampled data filtering. When only low-pass filtering is desired, the high-pass filter can be switched out of the signal path. A selectable, auxiliary, differential analog input is provided for applications where more than one analog input is required.

The A/D and D/A architectures ensure no missing codes and monotonic operation. An internal voltage reference is provided to ease the design task and to provide complete control over the performance of the IC. The internal voltage reference is brought out to a pin and is available to the designer. Separate analog and digital voltage supplies and grounds are provided to minimize noise and ensure a wide dynamic range. Also, the analog circuit path contains only differential circuitry to keep noise to an absolute minimum. The only exception is the DAC sample-and-hold, which utilizes pseudo-differential circuitry.

The output-reconstruction filter is an eighth-order CC-type (Chebyshev/elliptic transitional low-pass filter) followed by a second-order (sin x)/x correction filter) and is implemented in switched-capacitor technology. This filter is followed by a continuous-time filter to eliminate images of the digitally encoded signal. The on-board (sin x)/x correction filter can be switched out of the signal path using digital signal processor control, if desired.

The TLC32044C is characterized for operation from 0°C to 70°C and the TLC32044I is characterized for operation from −40°C to 85°C.

functional block diagram



PRINCIPLES OF OPERATION

analog input

Two sets of analog inputs are provided. Normally, the IN + and IN – input set is used; however, the auxiliary input set, AUX IN + and AUX IN –, can be used if a second input is required. Each input set can be operated in either differential or single-ended modes, since sufficient common-mode range and rejection are provided. The gain for the IN +, IN –, AUX IN +, and AUX IN – inputs can be programmed to be either 1, 2, or 4 (see Table 2). Either input circuit can be selected via software control. It is important to note that a wide dynamic range is assured by the differential internal analog architecture and by the separate analog and digital voltage supplies and grounds.

A/D bandpass filter, A/D bandpass filter clocking, and A/D conversion timing

The A/D high-pass filter can be selected or bypassed via software control. The frequency response of this filter is presented in the following pages. This response results when the switched-capacitor filter clock frequency is 288 kHz and the A/D sample rate is 8 kHz. Several possible options can be used to attain a 288-kHz switched-capacitor filter clock. When the filter clock frequency is not 288 kHz, the low-pass filter transfer function is frequency-scaled by the ratio of the actual clock frequency to 288 kHz. The ripple bandwidth and 3-dB low-frequency roll-off points of the high-pass section are 150 and 100 Hz, respectively. However, the high-pass section low-frequency roll-off is frequency-scaled by the ratio of the A/D sample rate to 8 kHz.

The Internal Timing Configuration and AIC DX Data Word Format sections of this data sheet indicate the many options for attaining a 288-kHz bandpass switched-capacitor filter clock. These sections indicate that the RX Counter A can be programmed to give a 288-kHz bandpass switched-capacitor filter clock for several Master Clock input frequencies.

PRINCIPLES OF OPERATION (continued)

The A/D conversion rate is then attained by frequency-dividing the 288-kHz bandpass switched-capacitor filter clock with the RX Counter B. Thus, unwanted aliasing is prevented because the A/D conversion rate is an integral submultiple of the bandpass switched-capacitor filter sampling rate, and the two rates are synchronously locked.

A/D converter performance specifications

Fundamental performance specifications for the A/D converter circuitry are presented in the A/D converter operating characteristics section of this data sheet. The realization of the A/D converter circuitry with switched-capacitor techniques provides an inherent sample-and-hold.

analog output

The analog output circuitry is an analog output power amplifier. Both noninverting and inverting amplifier outputs are brought out of the IC. This amplifier can drive transformer hybrids or low-impedance loads directly in either a differential or single-ended configuration.

D/A low-pass filter, D/A low-pass filter clocking, and D/A conversion timing

The frequency response of this filter is presented in the following pages. This response results when the low-pass switched-capacitor filter clock frequency is 288 kHz. Like the A/D filter, the transfer function of this filter is frequency-scaled when the clock frequency is not 288 kHz. A continuous-time filter is provided on the output of the (sin x)/x filter to eliminate the periodic sample data signal information, which occurs at multiples of the 288-kHz switched-capacitor filter clock. The continuous time filter also greatly attenuates any switched-capacitor clock feedthrough.

The D/A conversion rate is attained by frequency-dividing the 288-kHz switched-capacitor filter clock with TX Counter B. Thus, unwanted aliasing is prevented because the D/A conversion rate is an integral submultiple of the switched-capacitor low-pass filter sampling rate, and the two rates are synchronously locked.

asynchronous versus synchronous operation

If the transmit section of the AIC (low-pass filter and DAC) and receive section (bandpass filter and ADC) are operated asynchronously, the low-pass and bandpass filter clocks are independently generated from the Master Clock signal. Also, the D/A and A/D conversion rates are independently determined. If the transmit and receive sections are operated synchronously, the low-pass filter clock drives both low-pass and bandpass filters. In synchronous operation, the A/D conversion timing is derived from, and is equal to, the D/A conversion timing. (See description of the WORD/$\overline{\text{BYTE}}$ pin in the Pin Functional Description Section.)

D/A converter performance specifications

Fundamental performance specifications for the D/A converter circuitry are presented in the D/A converter operating characteristics section of the data sheet. The D/A converter has a sample-and-hold that is realized with a switched-capacitor ladder.

system frequency response correction

(Sin x)/x correction for the D/A converter's zero-order sample-and-hold output can be provided by an on-board second-order (sin x)/x correction filter. This (sin x)/x correction filter can be inserted into or deleted from the signal path by digital signal processor control. When inserted, the (sin x)/x correction filter follows the switched-capacitor low-pass filter. When the TB register (see Internal Timing Configuration section) equals 36, the correction results of Figures 11 and 12 will be obtained.

PRINCIPLES OF OPERATION (continued)

(Sin x)/x correction can also be accomplished by deleting the on-board second-order correction filter and performing the (sin x)/x correction in digital signal processor software. The system frequency response can be corrected via DSP software to ±0.1 dB accuracy to a band-edge of 3000 Hz for all sampling rates. This correction is accomplished with a first-order digital correction filter, which requires only seven TMS320 instruction cycles. With a 200-ns instruction cycle, seven instructions represent an overhead factor of only 1.1% and 1.3% for sampling rates of 8 and 9.6 kHz, respectively (see the (sin x)/x Correction Section for more details).

serial port

The serial port has four possible modes that are described in detail in the Functional Pin Description Section. These modes are briefly described below and in the Functional Description for Pin 13, WORD/$\overline{\text{BYTE}}$.

1. The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS320C17.
2. The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS32020, TMS320C25, and the TMS320C30.
3. The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS320C17.
4. The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS32020, TMS320C25, TMS320C30, or two SN74299 serial-to-parallel shift registers, which can then interface in parallel to the TMS32010, TMS320C15, to any other digital signal processor, or to external FIFO circuitry.

operation of TLC32044 with internal voltage reference

The internal reference of the TLC32044 eliminates the need for an external voltage reference and provides overall circuit cost reduction. Thus, the internal reference eases the design task and provides complete control over the performance of the IC. The internal reference is brought out to a pin and is available to the designer. To keep the amount of noise on the reference signal to a minimum, an external capacitor may be connected between REF and ANLG GND.

operation of TLC32044 with external voltage reference

The REF pin may be driven from an external reference circuit if so desired. This external circuit must be capable of supplying 250 μA and must be adequately protected from noise such as crosstalk from the analog input.

reset

A reset function is provided to initiate serial communications between the AIC and DSP and to allow fast, cost-effective testing during manufacturing. The reset function will initialize all AIC registers, including the control register. After a negative-going pulse on the $\overline{\text{RESET}}$ pin, the AIC will be initialized. This initialization allows normal serial port communications activity to occur between AIC and DSP (see AIC DX Data Word Format section).

PRINCIPLES OF OPERATION (continued)

loopback

This feature allows the user to test the circuit remotely. In loopback, the OUT + and OUT − pins are internally connected to the IN + and IN − pins. Thus, the DAC bits (d15 to d2), which are transmitted to the DX pin, can be compared with the ADC bits (d15 to d2), which are received from the DR pin. An ideal comparison would be that the bits on the DR pin equal the bits on the DX pin. However, in practice there will be some difference in these bits due to the ADC and DAC output offsets.

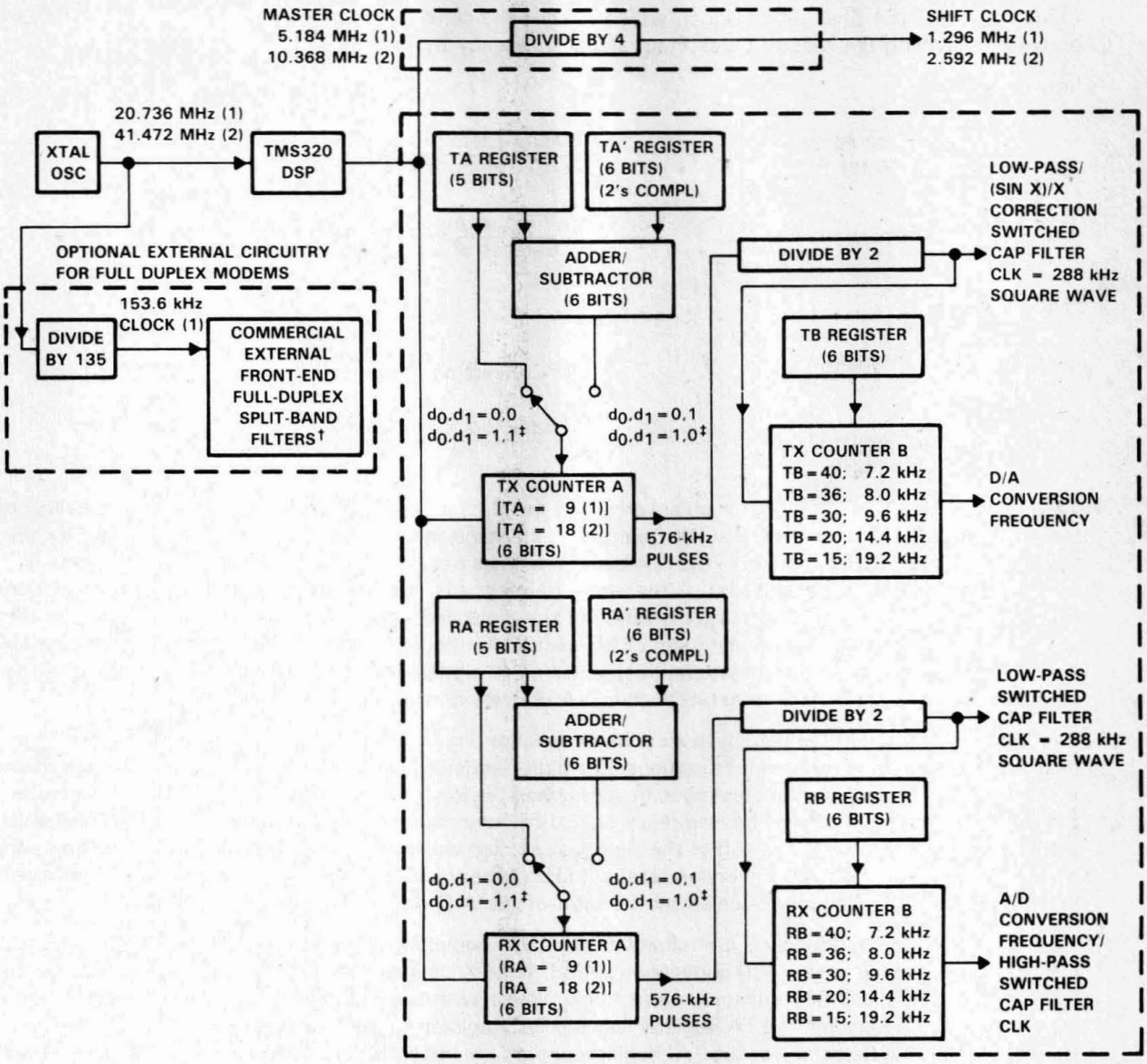
The loopback feature is implemented with digital signal processor control by transmitting the appropriate serial port bit to the control register (see AIC Data Word Format section).

PIN NAME	PIN NO.	I/O	DESCRIPTION
ANLG GND	17,18		Analog ground return for all internal analog circuits. Not internally connected to DGTL GND.
AUX IN +	24	I	Noninverting auxiliary analog input stage. This input can be switched into the bandpass filter and A/D converter path via software control. If the appropriate bit in the Control register is a 1, the auxiliary inputs will replace the IN + and IN − inputs. If the bit is a 0, the IN + and IN − inputs will be used (see the AIC DX Data Word Format section).
AUX IN −	23	I	Inverting auxiliary analog input (see the above AUX IN + pin description).
DGTL GND	9		Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
DR	5	O	This pin is used to transmit the ADC output bits from the AIC to the TMS320 serial port. This transmission of bits from the AIC to the TMS320 serial port is synchronized with the SHIFT CLK signal.
DX	12	I	This pin is used to receive the DAC input bits and timing and control information from the TMS320. This serial transmission from the TMS320 serial port to the AIC is synchronized with the SHIFT CLK signal.
$\overline{\text{EODR}}$	3	O	End of data receive. (See the WORD/$\overline{\text{BYTE}}$ pin description and the Serial Port Timing Diagram.) During the word-mode timing, this signal is a low-going pulse that occurs immediately after the 16 bits of A/D information have been transmitted from the AIC to the TMS320 serial port. This signal can be used to interrupt a microprocessor upon completion of serial communications. Also, this signal can be used to strobe and enable external serial-to-parallel shift registers, latches, or external FIFO RAM, and to facilitate parallel data bus communications between the AIC and the serial-to-parallel shift registers. During the byte-mode timing, this signal goes low after the first byte has been transmitted from the AIC to the TMS320 serial port and is kept low until the second byte has been transmitted. The TMS320C17 can use this low-going signal to differentiate between the two bytes as to which is first and which is second. $\overline{\text{EODR}}$ does not occur after secondary communication.

PIN NAME	PIN NO.	I/O	DESCRIPTION
$\overline{\text{EODX}}$	11	O	End of data transmit. (See the WORD/$\overline{\text{BYTE}}$ pin description and the Serial Port Timing Diagram.) During the word-mode timing, this signal is a low-going pulse that occurs immediately after the 16 bits of D/A converter and control or register information have been transmitted from the TMS320 serial port to the AIC. This signal can be used to interrupt a microprocessor upon the completion of serial communications. Also, this signal can be used to strobe and enable external serial-to-parallel shift registers, latches, or an external FIFO RAM, and to facilitate parallel data-bus communications between the AIC and the serial-to-parallel shift registers. During the byte-mode timing, this signal goes low after the first byte has been transmitted from the TMS320 serial port to the AIC and is kept low until the second byte has been transmitted. The TMS320C17 can use this low-going signal to differentiate between the two bytes as to which is first and which is second.
$\overline{\text{FSR}}$	4	O	Frame sync receive. In the serial transmission modes, which are described in the WORD/$\overline{\text{BYTE}}$ pin description, the $\overline{\text{FSR}}$ pin is held low during bit transmission. When the $\overline{\text{FSR}}$ pin goes low, the TMS320 serial port will begin receiving bits from the AIC via the DR pin of the AIC. The most significant DR bit will be present on the DR pin before $\overline{\text{FSR}}$ goes low. (See Serial Port Timing and Internal Timing Configuration Diagrams.) $\overline{\text{FSR}}$ does not occur after secondary communications.
$\overline{\text{FSX}}$	14	O	Frame sync transmit. When this pin goes low, the TMS320 serial port will begin transmitting bits to the AIC via the DX pin of the AIC. In all serial transmission modes, which are described in the WORD/$\overline{\text{BYTE}}$ pin description, the $\overline{\text{FSX}}$ pin is held low during bit transmission (see Serial Port Timing and Internal Timing Configuration Diagrams).
IN+	26	I	Noninverting input to analog input amplifier stage
IN−	25	I	Inverting input to analog input amplifier stage
MSTR CLK	6	I	The Master Clock signal is used to derive all the key logic signals of the AIC, such as the Shift Clock, the switched-capacitor filter clocks, and the A/D and D/A timing signals. The Internal Timing Configuration diagram shows how these key signals are derived. The frequencies of these key signals are synchronous submultiples of the Master Clock frequency to eliminate unwanted aliasing when the sampled analog signals are transferred between the switched-capacitor filters and the A/D and D/A converters (see the Internal Timing Configuration).
OUT+	22	O	Noninverting output of analog output power amplifier. Can drive transformer hybrids or high-impedance loads directly in either a differential or a single-ended configuration.
OUT−	21	O	Inverting output of analog output power amplifier. Functionally identical with and complementary to OUT+.
REF	8	I/O	The internal voltage reference is brought out on this pin. An external voltage reference can also be applied to this pin.
$\overline{\text{RESET}}$	2	I	A reset function is provided to initialize the TA, TA′, TB, RA, RA′, RB, and control registers. This reset function initiates serial communications between the AIC and DSP. The reset function will initialize all AIC registers including the control register. After a negative-going pulse on the $\overline{\text{RESET}}$ pin, the AIC registers will be initialized to provide an 8-kHz data conversion rate for a 5.184-MHz master clock input signal. The conversion rate adjust registers, TA′ and RA′, will be reset to 1. The CONTROL register bits will be reset as follows (see AIC DX Data Word Format section). d9 = 1, d7 = 1, d6 = 1, d5 = 1, d4 = 0, d3 = 0, d2 = 1 This initialization allows normal serial-port communication to occur between AIC and DSP.
SHIFT CLK	10	O	The Shift Clock signal is obtained by dividing the Master Clock signal frequency by four. This signal is used to clock the serial data transfers of the AIC, described in the WORD/$\overline{\text{BYTE}}$ pin description below (see the Serial Port Timing and Internal Timing Configuration diagram).
V_{DD}	7		Digital supply voltage, 5 V ±5%
V_{CC+}	20		Positive analog supply voltage, 5 V ±5%
V_{CC-}	19		Negative analog supply voltage, −5 V ±5%

PIN NAME	NO.	I/O	DESCRIPTION
WORD/$\overline{\text{BYTE}}$	13	I	This pin, in conjunction with a bit in the CONTROL register, is used to establish one of four serial modes. These four serial modes are described below. *AIC transmit and receive sections are operated asynchronously.* The following description applies when the AIC is configured to have asynchronous transmit and receive sections. If the appropriate data bit in the Control register is a 0 (see the AIC DX Data Word Format), the transmit and receive sections will be asynchronous. L Serial port directly interfaces with the serial port of the TMS320C17 and communicates in two 8-bit bytes. The operation sequence is as follows (see Serial Port Timing diagrams). 1. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought low. 2. One 8-bit byte is transmitted or one 8-bit byte is received. 3. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pin is brought low. 4. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin emits a positive frame-sync pulse that is four Shift Clock cycles wide. 5. One 8-bit byte is transmitted or one 8-bit byte is received. 6. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pin is brought high. 7. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought high. H Serial port directly interfaces with the serial ports of the TMS32020, TMS320C25, and TMS320C30, and communicates in one 16-bit word. The operation sequence is as follows (see Serial Port Timing diagrams): 1. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought low. 2. One 16-bit word is transmitted or one 16-bit word is received. 3. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought high. 4. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pin emits a low-going pulse. *AIC transmit and receive sections are operated synchronously.* If the appropriate data bit in the Control register is a 1, the transmit and receive sections will be configured to be synchronous. In this case, the bandpass switched-capacitor filter and the A/D conversion timing will be derived from the TX Counter A, TX Counter B, and TA, TA', and TB registers, rather than the RX Counter A, RX Counter B, and RA, RA', and RB registers. In this case, the AIC $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ timing will be identical during primary data communication; however, $\overline{\text{FSR}}$ will not be asserted during secondary data communication since there is no new A/D conversion result. The synchronous operation sequences are as follows (see Serial Port Timing diagrams). L Serial port directly interfaces with the serial port of the TMS320C17 and communicates in two 8-bit bytes. The operation sequence is as follows (see Serial Port Timing diagrams): 1. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought low. 2. One 8-bit byte is transmitted and one 8-bit byte is received. 3. The $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ pins are brought low. 4. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins emit positive frame-sync pulses that are four Shift Clock cycles wide. 5. One 8-bit byte is transmitted and one 8-bit byte is received. 6. The $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ pins are brought high. 7. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought high. H Serial port directly interfaces with the serial ports of the TMS32020, TMS320C25, and TMS320C30, and communicates in one 16-bit word. The operation sequence is as follows (see Serial Port Timing diagrams): 1. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought low. 2. One 16-bit word is transmitted and one 16-bit word is received. 3. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought high. 4. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pins emit low-going pulses. Since the transmit and receive sections of the AIC are now synchronous, the AIC serial port, with additional NOR and AND gates, will interface to two SN74299 serial-to-parallel shift registers. Interfacing the AIC to the SN74299 shift register allows the AIC to interface to an external FIFO RAM and facilitates parallel, data bus communications between the AIC and the digital signal processor. The operation sequence is the same as the above sequence (see Serial Port Timing diagrams).

INTERNAL TIMING CONFIGURATION



NOTE: Frequency 1, 20.736 MHz, is used to show how 153.6 kHz (for a commercially available modem split-band filter clock), popular speech and modem sampling signal frequencies, and an internal 288-kHz switched-capacitor filter clock can be derived synchronously and as submultiples of the crystal oscillator frequency. Since these derived frequencies are synchronous submultiples of the crystal frequency, aliasing does not occur as the sampled analog signal passes between the analog converter and switched-capacitor filter stages. Frequency 2, 41.472 MHz, is used to show that the AIC can work with high-frequency signals, which are used by high-speed digital signal processors.

†Split-band filtering can alternatively be performed after the analog input function via software in the TMS320.

‡These control bits are described in the AIC DX Data Word Format section.

explanation of internal timing configuration

All of the internal timing of the AIC is derived from the high-frequency clock signal that drives the Master Clock input pin. The Shift Clock signal, which strobes the serial port data between the AIC and DSP, is derived by dividing the Master Clock input signal frequency by four.

Low-pass:

$$\text{SCF Clock Frequency (D/A or A/D Path)} = \frac{\text{Master Clock Frequency}}{2 \times \text{Contents of Counter A}}$$

$$\text{Conversion Frequency} = \frac{\text{SCF Clock Frequency (D/A or A/D Path)}}{\text{Contents of Counter B}}$$

High-pass:

$$\text{SCF Clock Frequency (A/D Path)} = \text{A/D Conversion Frequency}$$

$$\text{Shift Clock Frequency} = \frac{\text{Master Clock Frequency}}{4}$$

TX Counter A and TX Counter B, which are driven by the Master Clock signal, determine the D/A conversion timing. Similarly, RX Counter A and RX Counter B determine the A/D conversion timing. In order for the low-pass switched-capacitor filter in the D/A path to meet its transfer function specifications, the frequency of its clock input must be 288 kHz. If the clock frequency is not 288 kHz, the filter transfer function frequencies are frequency-scaled by the ratios of the clock frequency to 288 kHz. Thus, to obtain the specified filter response, the combination of Master Clock frequency and TX Counter A and RX Counter A values must yield a 288-kHz switched-capacitor clock signal. This 288-kHz clock signal can then be divided by the TX Counter B to establish the D/A conversion timing.

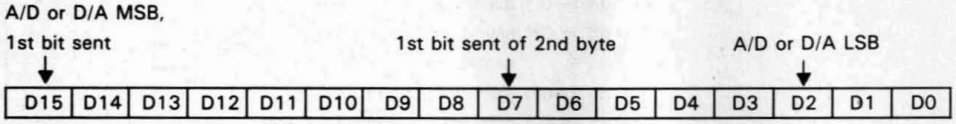
The transfer function of the bandpass switched-capacitor filter in the A/D path is a composite of its high-pass and low-pass section transfer functions. The high-frequency roll-off of the low-pass section will meet the bandpass filter transfer function specification when the low-pass section SCF is 288 kHz. Otherwise, the high-frequency roll-off will be frequency-scaled by the ratio of the high-pass section's SCF clock to 288 kHz. The low-frequency roll-off of the high-pass section will meet the bandpass filter transfer function specification when the A/D conversion rate is 8 kHz. Otherwise, the low-frequency roll-off of the high-pass section will be frequency-scaled by the ratio of the A/D conversion rate to 8 kHz.

TX Counter A and TX Counter B are reloaded every D/A conversion period, while RX Counter A and RX Counter B are reloaded every A/D conversion period. The TX Counter B and RX Counter B are loaded with the values in the TB and RB Registers, respectively. Via software control, the TX Counter A can be loaded with either the TA Register, the TA Register less the TA' Register, or the TA Register plus the TA' Register. By selecting the TA Register less the TA' Register option, the upcoming conversion timing will occur earlier by an amount of time that equals TA' times the signal period of the Master Clock. By selecting the TA Register plus the TA' Register option, the upcoming conversion timing will occur later by an amount of time that equals TA' times the signal period of the Master Clock. Thus, the D/A conversion timing can be advanced or retarded. An identical ability to alter the A/D conversion timing is provided. In this case, however, the RX Counter A can be programmed via software control with the RA Register, the RA Register less the RA' Register, or the RA Register plus the RA' Register.

The ability to advance or retard conversion timing is particularly useful for modem applications. This feature allows controlled changes in the A/D and D/A conversion timing. This feature can be used to enhance signal-to-noise performance, to perform frequency-tracking functions, and to generate nonstandard modem frequencies.

If the transmit and receive sections are configured to be synchronous (see WORD/$\overline{\text{BYTE}}$ pin description), then both the low-pass and bandpass switched-capacitor filter clocks are derived from TX Counter A. Also, both the D/A and A/D conversion timing are derived from the TX Counter A and TX Counter B. When the transmit and receive sections are configured to be synchronous, the RX Counter A, RX Counter B, RA Register, RA′ Register, and RB Registers are not used.

AIC DR or DX word bit pattern



AIC DX data word format section

d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	COMMENTS
primary DX serial communication protocol																
← d15 (MSB) through d2 go to the D/A converter register →														0	0	The TX and RX Counter A's are loaded with the TA and RA register values. The TX and RX Counter B's are loaded with TB and RB register values.
← d15 (MSB) through d2 go to the D/A converter register →														0	1	The TX and RX Counter A's are loaded with the TA + TA′ and RA + RA′ register values. The TX and RX Counter B's are loaded with the TB and RB register values. NOTE: d1 = 0, d0 = 1 will cause the next D/A and A/D conversion periods to be changed by the addition of TA′ and RA′ Master Clock cycles, in which TA′ and RA′ can be positive or negative or zero. Please refer to Table 1. AIC Responses to Improper Conditions.
← d15 (MSB) through d2 go to the D/A converter register →														1	0	The TX and RX Counter A's are loaded with the TA − TA′ and RA − RA′ register values. The TX and RX Counter B's are loaded with the TB and RB register values. NOTE: d1 = 1, d0 = 0 will cause the next D/A and A/D conversion periods to be changed by the subtraction of TA′ and RA′ Master Clock cycles, in which TA′ and RA′ can be positive or negative or zero. Please refer to Table 1. AIC Responses to Improper Conditions.
← d15 (MSB) through d2 go to the D/A converter register →														1	1	The TX and RX Counter A's are loaded with the TA and RA register converter register values. The TX and RX Counter B's are loaded with the TB and RB register values. After a delay of four Shift Clock cycles, a secondary transmission will immediately follow to program the AIC to operate in the desired configuration.

NOTE: Setting the two least significant bits to 1 in the normal transmission of DAC information (Primary Communications) to the AIC will initiate Secondary Communications upon completion of the Primary Communications.

Upon completion of the Primary Communication, $\overline{\text{FSX}}$ will remain high for four SHIFT CLOCK cycles and will then go low and initiate the Secondary Communication. The timing specifications for the Primary and Secondary Communications are identical. In this manner, the Secondary Communication, if initiated, is interleaved between successive Primary Communications. This interleaving prevents the Secondary Communication from interfering with the Primary Communications and DAC timing, thus preventing the AIC from skipping a DAC output. It is important to note that in the synchronous mode, $\overline{\text{FSR}}$ will not be asserted during Secondary Communications.

secondary DX serial communication protocol

x x | ← to TA register → | x x | ← to RA register → | 0 0	d13 and d6 are MSBs (unsigned binary)
x | ← to TA′ register → | x | ← to RA′ register → | 0 1	d14 and d7 are 2's complement sign bits
x | ← to TB register → | x | ← to RB register → | 1 0	d14 and d7 are MSBs (unsigned binary)
x x x x x x d9 x d7 d6 d5 d4 d3 d2 1 1 CONTROL REGISTER	d2 = 0/1 deletes/inserts the A/D high-pass filter d3 = 0/1 disables/enables the loopback function d4 = 0/1 disables/enables the AUX IN+ and AUX IN− pins d5 = 0/1 asynchronous/synchronous transmit and receive sections d6 = 0/1 gain control bits (see Gain Control Section) d7 = 0/1 gain control bits (see Gain Control Section) d9 = 0/1 delete/insert on-board second-order (sin x)/x correction filter

reset function

A reset function is provided to initiate serial communications between the AIC and DSP. The reset function will initialize all AIC registers, including the control register. After power has been applied to the AIC, a negative-going pulse on the $\overline{\text{RESET}}$ pin will initialize the AIC registers to provide an 8-kHz A/D and D/A conversion rate for a 5.184 MHz master clock input signal. The AIC, excepting the CONTROL register, will be initialized as follows (see AIC DX Data Word Format section):

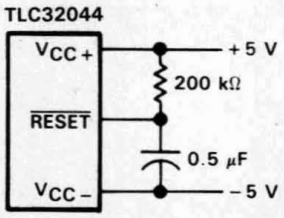
REGISTER	INITIALIZED REGISTER VALUE (HEX)
TA	9
TA′	1
TB	24
RA	9
RA′	1
RB	24

The CONTROL register bits will be reset as follows (see AIC DX Data Word Format section):

d9 = 1, d7 = 1, d6 = 1, d5 = 1, d4 = 0, d3 = 0, d2 = 1

This initialization allows normal serial port communications to occur between AIC and DSP. If the transmit and receive sections are configured to operate synchronously and the user wishes to program different conversion rates, only the TA, TA′, and TB register need to be programmed, since both transmit and receive timing are synchronously derived from these registers (see the Pin Descriptions and AIC DX Word Format sections).

The circuit shown below will provide a reset on power-up when power is applied in the sequence given under Power-Up Sequence. The circuit depends on the power supplies' reaching their recommended values a minimum of 800 ns before the capacitor charges to 0.8 V above DGTL GND.



power-up sequence

To ensure proper operation of the AIC, and as a safeguard against latch-up, it is recommmended that Schottky diodes with forward voltages less than or equal to 0.4 V be connected from V_{CC-} to ANLG GND and from V_{CC-} to DGTL GND (see Figure 21). In the absence of such diodes, power should be applied in the following sequence: ANLG GND and DGTL GND, V_{CC-}, then V_{CC+} and V_{DD}. Also, no input signal should be applied until after power-up.

AIC responses to improper conditions

The AIC has provisions for responding to improper conditions. These improper conditions and the response of the AIC to these conditions are presented in Table 1 below.

AIC register constraints

The following constraints are placed on the contents of the AIC registers:

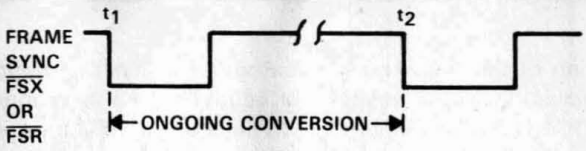
1. TA register must be ≥ 4 in word mode (WORD/$\overline{\text{BYTE}}$ = High).
2. TA register must be ≥ 5 in byte mode (WORD/$\overline{\text{BYTE}}$ = Low).
3. TA′ register can be either positive, negative, or zero.
4. RA register must be ≥ 4 in word mode (WORD/$\overline{\text{BYTE}}$ = High).
5. RA register must be ≥ 5 in byte mode (WORD/$\overline{\text{BYTE}}$ = Low).
6. RA′ register can be either positive, negative, or zero.
7. (TA register ± TA′ register) must be > 1.
8. (RA register ± RA′ register) must be > 1.
9. TB register must be > 1.

TABLE 1. AIC RESPONSES TO IMPROPER CONDITIONS

IMPROPER CONDITION	AIC RESPONSE
TA register + TA′ register = 0 or 1 TA register − TA′ register = 0 or 1	Reprogram TX Counter A with TA register value
TA register + TA′ register < 0	MODULO 64 arithmetic is used to ensure that a positive value is loaded into the TX Counter A, i.e., TA register + TA′ register + 40 HEX is loaded into TX Counter A.
RA register + RA′ register = 0 or 1 RA register − RA′ register = 0 or 1	Reprogram RX Counter A with RA register value
RA register + RA′ register = 0 or 1	MODULO 64 arithmetic is used to ensure that a positive value is loaded into RX Counter A, i.e., RA register + RA′ register + 40 HEX is loaded into RX Counter A.
TA register = 0 or 1 RA register = 0 or 1	AIC is shut down.
TA register < 4 in word mode TA register < 5 in byte mode RA register < 4 in word mode RA register < 5 in byte mode	The AIC serial port no longer operates.
TB register = 0 or 1	Reprogram TB register with 24 HEX
RB register = 0 or 1	Reprogram RB register with 24 HEX
AIC and DSP cannot communicate	Hold last DAC output

improper operation due to conversion times being too close together

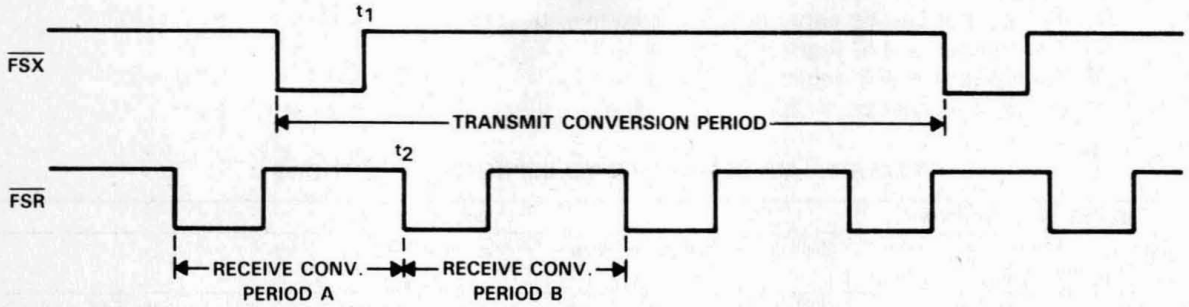
If the difference between two successive D/A conversion frame syncs is less that 1/19.2 kHz, the AIC operates improperly. In this situation, the second D/A conversion frame sync occurs too quickly and there is not enough time for the ongoing conversion to be completed. This situation can occur if the A and B registers are improperly programmed or if the A + A′ register or A − A′ register result is too small. When incrementally adjusting the conversion period via the A + A′ register options, the designer should be very careful not to violate this requirement (see following diagram).



$t_2 - t_1 \geq 1/19.2$ kHz

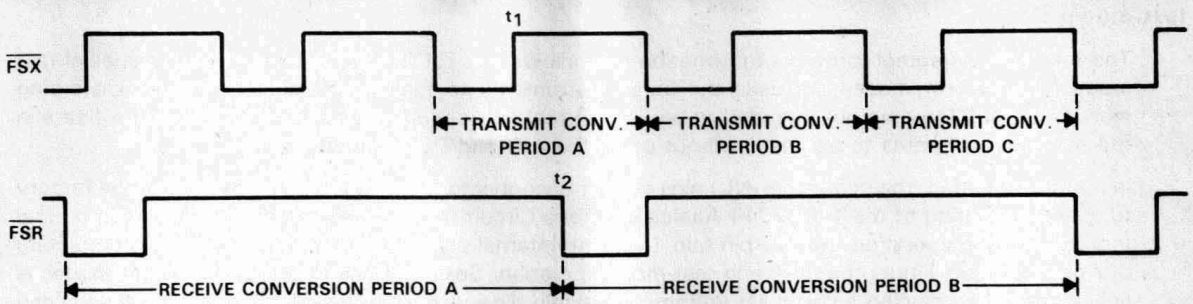
asynchronous operation — more than one receive frame sync occurring between two transmit frame syncs

When incrementally adjusting the conversion period via the A + A′ or A − A′ register options, a specific protocol is followed. The command to use the incremental conversion period adjust option is sent to the AIC during a $\overline{\text{FSX}}$ frame sync. The ongoing conversion period is then adjusted. However, either Receive Conversion Period A or B may be adjusted. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. Therefore, if there is sufficient time between t1 and t2, the receive conversion period adjustment will be performed during Receive Conversion Period A. Otherwise, the adjustment will be performed during Receive Conversion Period B. The adjustment command only adjusts one transmit conversion period and one receive conversion period. To adjust another pair of transmit and receive conversion periods, another command must be issued during a subsequent $\overline{\text{FSX}}$ frame (see figure below).



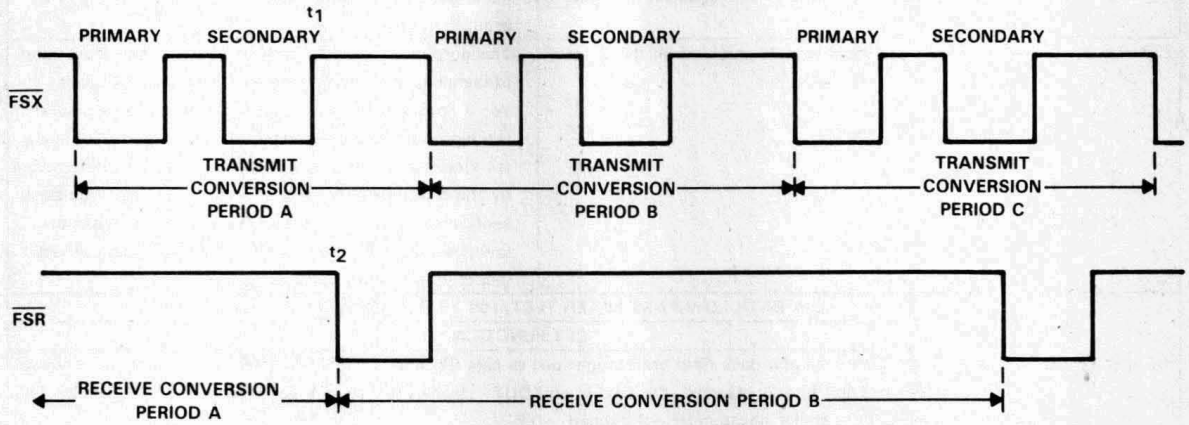
asynchronous operation — more than one transmit frame sync occurring between two receive frame syncs

When incrementally adjusting the conversion period via the A + A′ or A − A′ register options, a specific protocol is followed. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. The command to use the incremental conversion period adjust options is sent to the AIC during a $\overline{\text{FSX}}$ frame sync. The ongoing transmit conversion period is then adjusted. However, three possibilities exist for the receive conversion period adjustment in the diagram as shown in the following figure. If the adjustment command is issued during Transmit Conversion Period A, Receive Conversion Period A will be adjusted if there is sufficient time between t1 and t2. Or, if there is not sufficient time between t1 and t2, Receive Conversion Period B will be adjusted. Or, the receive portion of an adjustment command may be ignored if the adjustment command is sent during a receive conversion period, which is already being or will be adjusted due to a prior adjustment command. For example, if adjustment commands are issued during Transmit Conversion Periods A, B, and C, the first two commands may cause Receive Conversion Periods A and B to be adjusted, while the third receive adjustment command is ignored. The third adjustment command is ignored since it was issued during Receive Conversion Period B, which already will be adjusted via the Transmit Conversion Period B adjustment command.



asynchronous operation — more than one set of primary and secondary DX serial communication occurring between two receive frame sync (see AIC DX Data Word Format section)

The TA, TA′, TB, and control register information that is transmitted in the secondary communications is always accepted and is applied during the ongoing transmit conversion period. If there is sufficient time between t1 and t2, the TA, RA′, and RB register information, which is sent during Transmit Conversion Period A, will be applied to Receive Conversion Period A. Otherwise, this information will be applied during Receive Conversion Period B. If RA, RA′, and RB register information has already been received and is being applied during an ongoing conversion period, any subsequent RA, RA′, or RB information that is received during this receive conversion period will be disregarded (see diagram below).



test modes†

The following paragraph provides information that allows the TLC32044 to be operated in special test modes. These test modes are used by Texas Instruments to facilitate testing of the device during manufacturing. They are not intended to be used in real applications, however, they allow the filters in the A/D and D/A paths to be used without using the A/D and D/A converters.

In normal operation, the nonusable (NU) pins are left unconnected. These NU pins are used by the factory to speed up testing of the TLC32044 Analog Interface Circuit (AIC). When the device is used in normal (non-test-mode) operation, the NU pin (pin 1) has an internal pull-down to −5 V. Externally connecting 0 V or 5 V to pin 1 puts the device in test-mode operation. Selecting one of the possible test modes is accomplished by placing a particular voltage on certain pins. A description of these modes is provided in Table 2 and Figures 1 and 2.

TABLE 2. LIST OF TEST MODES

TEST PINS	D/A PATH TEST (PIN 1 to 5 V)	A/D PATH TEST (PIN 1 to 0)
	TEST FUNCTION	TEST FUNCTION
5	The low-pass switched-capacitor filter clock is brought out to pin 5. This clock signal is normally internal.	The bandpass switched-capacitor filter clock is brought out to pin 5. This clock signal is normally internal.
11	No change from normal operation. The $\overline{\text{EODX}}$ signal is brought out to pin 11.	The pulse that initiates the A/D conversion is brought out here. This signal is normally internal.
3	The pulse that initiates the D/A conversion is brought out here.	No change from normal operation. The EODR signal is brought out.
27 and 28	There are no test output signals provided on these pins.	The outputs of the A/D path low-pass or bandpass filter (depending upon control bit d2 — see AIC DX Data Word Format section) are brought out to these pins. If the high-pass section is inserted, the output will have a (sinx)/x droop. The slope of the droop will be determined by the ADC sampling frequency, which is the high-pass section clock frequency (see diagram of bandpass or low-pass filter test for receive section). These outputs will drive small (30-pF) loads.
	D/A PATH LOW-PASS FILTER TEST; PIN 13 (WORD/$\overline{\text{BYTE}}$) to −5 V	
	TEST FUNCTION	
I5 and 16	The inputs of the D/A path low-pass filter are brought out to pins 15 and 16. The D/A input to this filter is removed. If the (sin x)/x correction filter is inserted, the OUT+ and OUT− signals will have a flat response (see Figure 2). The common-mode range of these inputs must not exceed ±0.5 V.	

† In the test mode, the AIC responds to the setting of Pin 13 to −5 V, as if Pin 13 were set to 0 V. Thus, the byte mode is selected for communicating between DSP and AIC. Either of the path tests (D/A or A/D) can be performed simultaneously with the D/A low-pass filter test. In this situation, Pin 13 must be connected to −5 V, which initiates byte-mode communications.

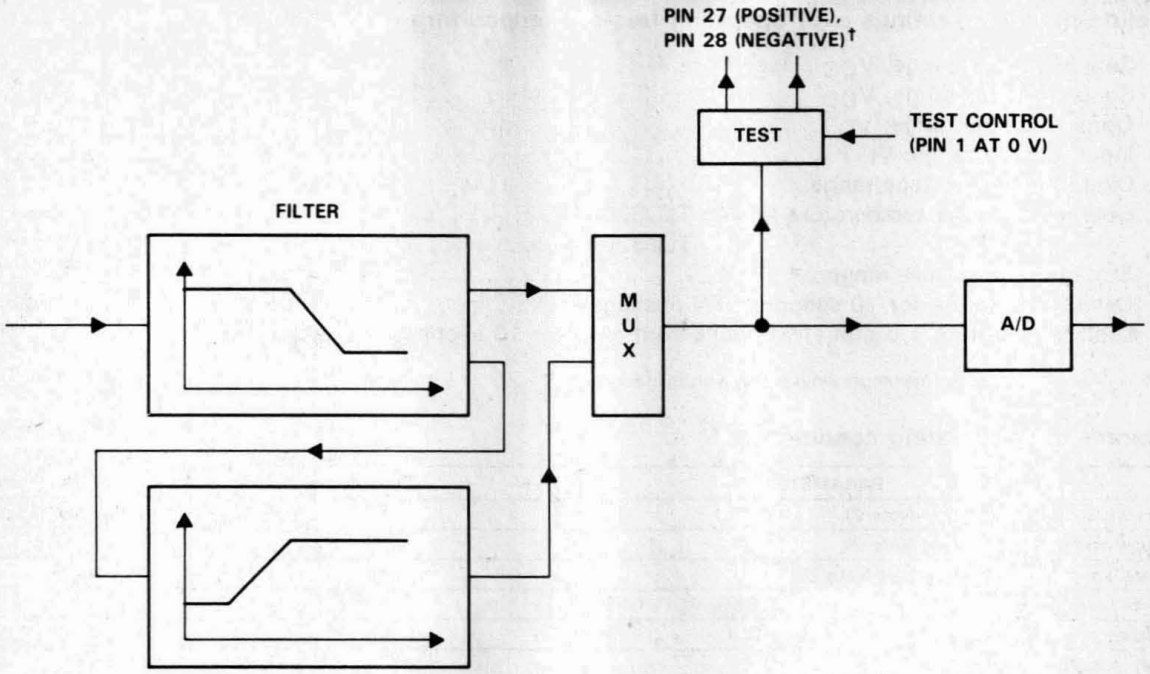


FIGURE 1. BANDPASS OR LOW-PASS FILTER TEST FOR RECEIVER SECTION

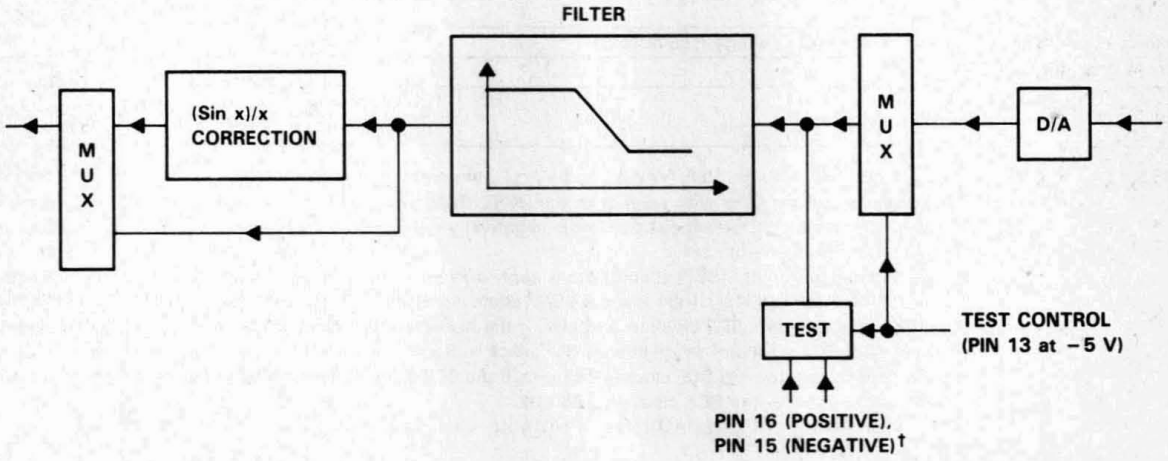


FIGURE 2. LOW-PASS FILTER TEST FOR TRANSMIT SECTION

†All analog signal paths have differential architecture and hence have positive and negative components.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC+} (see Note 1) . . . . . −0.3 V to 15 V
Supply voltage range, V_{DD} . . . . . −0.3 V to 15 V
Output voltage range, V_O . . . . . −0.3 V to 15 V
Input voltage range, V_I . . . . . −0.3 V to 15 V
Digital ground voltage range . . . . . −0.3 V to 15 V
Operating free-air temperature range: TLC32044C . . . . . 0°C to 70°C
TLC32044I . . . . . −40°C to 85°C
Storage temperature range . . . . . −40°C to 125°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTE 1: Voltage values for maximum ratings are with respect to VCC−.

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} (see Note 2)		4.75	5	5.25	V
Supply voltage, V_{CC-} (see Note 2)		−4.75	−5	−5.25	V
Digital supply voltage, V_{DD} (see Note 2)		4.75	5	5.25	V
Digital ground voltage with respect to ANLG GND, DGTL GND			0		V
Reference input voltage, $V_{ref(ext)}$ (see Note 2)		2		4	V
High-level input voltage, V_{IH}		2		V_{DD}+0.3	V
Low-level input voltage, V_{IL} (see Note 3)		−0.3		0.8	V
Load resistance at OUT+ and/or OUT−, R_L		300			Ω
Load capacitance at OUT+ and/or OUT−, C_L				100	pF
MSTR CLK frequency (see Note 4)		0.075	5	10.368	MHz
Analog input amplifier common mode input voltage (see Note 5)				±1.5	V
A/D or D/A conversion rate				20	kHz
Operating free-air temperature, T_A	TLC32044C	0		70	°C
	TLC32044I	−40		85	

NOTES: 2. Voltages at analog inputs and outputs, REF, V_{CC+}, and V_{CC-}, are with respect to the ANLG GND terminal. Voltages at digital inputs and outputs and V_{DD} are with respect to the DGTL GND terminal.
3. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels and temperature only.
4. The bandpass switched-capacitor filter (SCF) specifications apply only when the low-pass section SCF clock is 288 kHz and the high-pass section SCF clock is 8 kHz. If the low-pass SCF clock is shifted from 288 kHz, the low-pass roll-off frequency will shift by the ratio of the low-pass SCF clock to 288 kHz. If the high-pass SCF clock is shifted from 8 kHz, the high-pass roll-off frequency will shift by the ratio of the high-pass SCF clock to 8 kHz. Similarly, the low-pass switched-capacitor filter (SCF) specifications apply only when the SCF clock is 288 kHz. If the SCF clock is shifted from 288 kHz, the low-pass roll-off frequency will shift by the ratio of the SCF clock to 288 kHz.
5. This range applies when (IN+ − IN−) or (AUX IN+ − AUX IN−) equals ±6 V.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (unless otherwise noted)

total device, MSTR CLK frequency = 5.184 MHz, outputs not loaded

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 4.75 V, I_{OH} = −300 μA	2.4			V
V_{OL}	Low-level output voltage		V_{DD} = 4.75 V, I_{OL} = 2 mA			0.4	V
I_{CC+}	Supply current from V_{CC+}	TLC32044C				35	mA
		TLC32044I				40	
I_{CC-}	Supply current from V_{CC-}	TLC32044C				−35	mA
		TLC32044I				−40	
I_{DD}	Supply current from V_{DD}		$f_{MSTR\ CLK}$ = 5.184 MHz			7	mA
V_{ref}	Internal reference output voltage			3		3.3	V
αV_{ref}	Temperature coefficient of internal reference voltage				200		ppm/°C
r_o	Output resistance at REF				100		kΩ

receive amplifier input

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	A/D converter offset error (filters in)			10	70	mV
CMRR	Common-mode rejection ratio at IN+, IN−, or AUX IN+, AUX IN−	See Note 6		55		dB
r_i	Input resistance at IN+, IN− or AUX IN+, AUX IN−, REF			100		kΩ

transmit filter output

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OO}	Output offset voltage at OUT+ or OUT− (single-ended relative to ANLG GND)			15	80	mV
V_{OM}	Maximum peak output voltage swing across R_L at OUT+ or OUT− (single-ended)	$R_L \geq 300\ \Omega$, Offset voltage = 0	±3			V
V_{OM}	Maximum peak output voltage swing between OUT+ and OUT− (differential output)	$R_L \geq 600\ \Omega$	±6			V

†All typical values are at T_A = 25°C.
NOTE 6: The test condition is a 0-dBm, 1-kHz input signal with an 8-kHz conversion rate.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (unless otherwise noted)

system distortion specifications, SCF clock frequency = 288 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Attenuation of second harmonic of A/D input signal	single-ended	V_{in} = −0.5 dB to −24 dB referred to V_{ref}, See Note 7		70		dB
	differential		62	70		
Attenuation of third and higher harmonics of A/D input signal	single-ended	V_{in} = −0.5 dB to −24 dB referred to V_{ref}, See Note 7		65		dB
	differential		57	65		
Attenuation of second harmonic of D/A input signal	single-ended	V_{in} = −0 dB to −24 dB referred to V_{ref}, See Note 7		70		dB
	differential		62	70		
Attenuation of third and higher harmonics of D/A input signal	single-ended	V_{in} = −0 dB to −24 dB referred to V_{ref}, See Note 7		65		dB
	differential		57	65		

A/D channel signal-to-distortion ratio

PARAMETER	TEST CONDITIONS (see Note 7)	A_v = 1‡		A_v = 2‡		A_v = 4‡		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
A/D channel signal-to-distortion ratio	V_{in} = −6 dB to −0.1 dB	58		>58§		>58§		dB
	V_{in} = −12 dB to −6 dB	58		58		>58§		
	V_{in} = −18 dB to −12 dB	56		58		58		
	V_{in} = −24 dB to −18 dB	50		56		58		
	V_{in} = −30 dB to −24 dB	44		50		56		
	V_{in} = −36 dB to −30 dB	38		44		50		
	V_{in} = −42 dB to −36 dB	32		38		44		
	V_{in} = −48 dB to −42 dB	26		32		38		
	V_{in} = −54 dB to −48 dB	20		26		32		

†All typical values are at T_A = 25°C.
‡A_v is the programmable gain of the input amplifier.
§A value >60 is over range and signal clipping occurs.

D/A channel signal-to-distortion ratio

PARAMETER	TEST CONDITIONS (see Note 7)	MIN	MAX	UNIT
D/A channel signal-to-distortion ratio	V_{in} = −6 dB to 0 dB	58		dB
	V_{in} = −12 dB to −6 dB	58		
	V_{in} = −18 dB to −12 dB	56		
	V_{in} = −24 dB to −18 dB	50		
	V_{in} = −30 dB to −24 dB	44		
	V_{in} = −36 dB to −30 dB	38		
	V_{in} = −42 dB to −36 dB	32		
	V_{in} = −48 dB to −42 dB	26		
	V_{in} = −54 dB to −48 dB	20		

NOTE 7: The test condition is a 1-kHz input signal with an 8-kHz conversion rate (0 dB relative to V_{ref}). The load impedance for the DAC is 600 Ω.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (unless otherwise noted) (continued)

gain and dynamic range

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Absolute transmit gain tracking error while transmitting into 600 Ω	−48 dB to 0 dB signal range, See Note 8		±0.05	±0.15	dB
Absolute receive gain tracking error	−48 dB to 0 dB signal range, See Note 8		±0.05	±0.15	dB
Absolute gain of the A/D channel	Signal input is a −0.5-dB, 1-kHz sinewave		0.2		dB
Absolute gain of the D/A channel	Signal input is a 0-dB, 1-kHz sinewave		−0.3		dB

power supply rejection and crosstalk attenuation

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{CC+} or V_{CC-} supply voltage rejection ratio, receive channel	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at DR (ADC output)		30		dB
	f = 30 kHz to 50 kHz			45		
V_{CC+} or V_{CC-} supply voltage rejection ratio, transmit channel (single-ended)	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at OUT+		30		dB
	f = 30 kHz to 50 kHz			45		
Crosstalk attenuation, transmit-to-receive (single-ended)				80		dB

†All typical values are at T_A = 25°C.
NOTE 8: Gain tracking is relative to the absolute gain at 1 kHz and 0 dB (0 db relative to V_{ref}).

delay distortion

bandpass filter transfer function, SCF f_{clock} = 288 kHz IN+ – IN– is a ±3 V sinewave† (see Note 9)

PARAMETER	TEST CONDITION	FREQUENCY RANGE	ADJUSTMENT ADDEND‡	MIN	TYP§	MAX	UNIT
Filter gain	Input signal reference to 0 dB	f ≤ 50 Hz	K1 × 0 dB	–33	–29	–25	dB
		f = 100 Hz	K1 × – 0.26 dB	–4	–2	–1	
		f = 150 Hz to 3100 Hz	K1 × 0 dB	–0.25	0	0.25	
		f = 3100 Hz to 3300 Hz	K1 × 0 dB	–0.3	0	0.3	
		f = 3300 Hz to 3650 Hz	K1 × 0 dB	–0.5	0	0.5	
		f = 3800 Hz	K1 × 2.3 dB	–5	–3	–1	
		f = 4000 Hz	K1 × 2.7 dB	–20	–17	–16	
		f ≥ 4400 Hz	K1 × 3.2 dB			–40	
		f ≥ 5000 Hz	K1 × 0 dB			–65	

low-pass filter transfer function (see curves), SCF f_{clock} = 288 kHz (see Note 9)

PARAMETER	TEST CONDITION	FREQUENCY RANGE	ADJUSTMENT ADDEND‡	MIN	TYP§	MAX	UNIT
Filter gain	Input signal reference is 0 dB	f = 0 Hz to 3100 Hz	K1 × 0 dB	–0.25	0	0.25	dB
		f = 3100 Hz to 3300 Hz	K1 × 0 dB	–0.3	0	0.3	
		f = 3300 Hz to 3650 Hz	K1 × 0 dB	–0.5	0	0.5	
		f = 3800 Hz	K1 × 2.3 dB	–5	–3	–1	
		f = 4000 Hz	K1 × 2.7 dB	–20	–17	–16	
		f ≥ 4400 Hz	K1 × 3.2 dB			–40	
		f ≥ 5000 Hz	K1 × 0 dB			–65	

serial port

PARAMETER		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –300 μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4	V
I_I	Input current				±10	μA
C_i	Input capacitance			15		pF
C_o	Output capacitance			15		pF

† See filter curves in typical characteristics.

‡ The MIN, TYP, and MAX specifications are given for a 288-kHz SCF clock frequency. A slight error in the 288-kHz SCF may result from inaccuracies in the MSTR CLK frequency, resulting from crystal frequency tolerances. If this frequency error is less than 0.25%, the ADJUSTMENT ADDEND should be added to the MIN, TYP, and MAX specifications, where K1 = 100 • [(SCF frequency – 288 kHz)/288 kHz]. For errors greater than 0.25%, see Note 10.

§ All typical values are at T_A = 25°C.

NOTE 9: The filter gain outside of the passband is measured with respect to the gain at 1 kHz. The filter gain within the passband is measured with respect to the average gain within the passband. The passbands are 150 to 3600 Hz and 0 to 3600 Hz for the bandpass and low-pass filters respectively. For switched-capacitor filter clocks at frequencies other than 288 kHz, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 288 kHz.

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V

noise (measurement includes low-pass and bandpass switched-capacitor filters)

PARAMETER		TEST CONDITIONS	TYP†	MAX	UNIT
Transmit noise	with (sin x)/x	DX input = 00000000000000, constant input code		550	μV rms
	without (sin x)/x		325	425	μV rms
			18		dBrnc0
Receive noise (see Note 10)		Inputs grounded, gain = 1	300	500	μV rms
			18		dBrnc0

timing requirements

serial port recommended input signals

	PARAMETER	MIN	MAX	UNIT
$t_{c(MCLK)}$	Master clock cycle time	95		ns
$t_{r(MCLK)}$	Master clock rise time		10	ns
$t_{f(MCLK)}$	Master clock fall time		10	ns
	Master clock duty cycle	25%	75%	
	$\overline{RESET}$ pulse duration (see Note 11)	800		ns
$t_{su(DX)}$	DX setup time before SCLK↓	20		ns
$t_{h(DX)}$	DX hold time after SCLK↓	$t_{c(SCLK)}/4$		ns

NOTES: 10. The noise is computed by statistically evaluating the digital output of the A/D converter.
11. $\overline{RESET}$ pulse duration is the amount of time that the reset pin is held below 0.8 V after the power supplies have reached their recommended values.

serial port—AIC output signals, C_L = 30 pF for SHIFT CLK output, C_L = 15 pF for all other outputs

	PARAMETER	MIN	TYP†	MAX	UNIT
$t_{c(SCLK)}$	Shift clock (SCLK) cycle time	380			ns
$t_{f(SCLK)}$	Shift clock (SCLK) fall time		3	8	ns
$t_{r(SCLK)}$	Shift clock (SCLK) rise time		3	8	ns
	Shift clock (SCLK) duty cycle	45		55	%
$t_{d(CH-FL)}$	Delay from SCLK↑ to $\overline{FSR}/\overline{FSX}/\overline{FSD}$↓		30		ns
$t_{d(CH-FH)}$	Delay from SCLK↑ to $\overline{FSR}/\overline{FSX}/\overline{FSD}$↑		35	90	ns
$t_{d(CH-DR)}$	DR valid after SCLK↑			90	ns
$t_{dw(CH-EL)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↓ in word mode			90	ns
$t_{dw(CH-EH)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↑ in word mode			90	ns
$t_{f(EODX)}$	$\overline{EODX}$ fall time		2	8	ns
$t_{f(EODR)}$	$\overline{EODR}$ fall time		2	8	ns
$t_{db(CH-EL)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↓ in byte mode			90	ns
$t_{db(CH-EH)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↑ in byte mode			90	ns
$t_{d(MH-SL)}$	Delay from MSTR CLK↑ to SCLK↓		65	170	ns
$t_{d(MH-SH)}$	Delay from MSTR CLK↑ to SCLK↑		65	170	ns

†Typical values are at T_A = 25°C.

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (continued)

serial port — AIC output signals

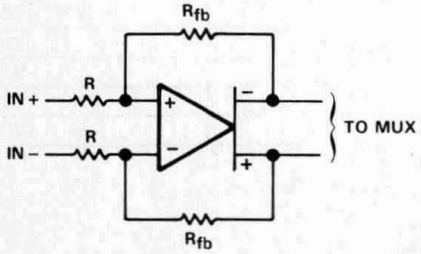
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{c(SCLK)}$	Shift clock (SCLK) cycle time		380			ns
$t_{f(SCLK)}$	Shift clock (SCLK) fall time				50	ns
$t_{r(SCLK)}$	Shift clock (SCLK) rise time				50	ns
	Shift clock (SCLK) duty cycle		45		55	%
$t_{d(CH-FL)}$	Delay from SCLK↑ to $\overline{FSR/FSX}$↓	C_L = 50 pF			52	ns
$t_{d(CH-FH)}$	Delay from SCLK↑ to $\overline{FSR/FSX}$↑	C_L = 50 pF			52	ns
$t_{d(CH-DR)}$	DR valid after SCLK↑				90	ns
$t_{dw(CH-EL)}$	Delay from SCLK↑ to $\overline{EODX/EODR}$↓ in word mode				90	ns
$t_{dw(CH-EH)}$	Delay from SCLK↑ to $\overline{EODX/EODR}$↑ in word mode				90	ns
$t_{f(EODX)}$	$\overline{EODX}$ fall time				15	ns
$t_{f(EODR)}$	$\overline{EODR}$ fall time				15	ns
$t_{db(CH-EL)}$	Delay from SCLK↑ to $\overline{EODX/EODR}$↓ in byte mode				100	ns
$t_{db(CH-EH)}$	Delay from SCLK↑ to $\overline{EODX/EODR}$↑ in byte mode				100	ns
$t_{d(MH-SL)}$	Delay from MSTR CLK↑ to SCLK↓			65		ns
$t_{d(MH-SH)}$	Delay from MSTR CLK↑ to SCLK↑			65		ns

†Typical values are at T_A = 25°C.

TABLE 3. GAIN CONTROL TABLE (ANALOG INPUT SIGNAL REQUIRED FOR FULL-SCALE A/D CONVERSION)

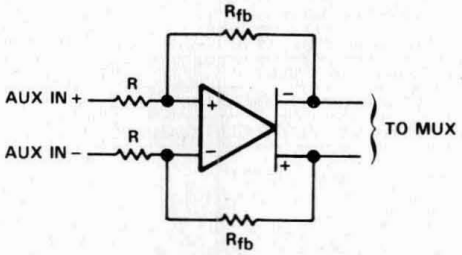
INPUT CONFIGURATIONS	CONTROL REGISTER BITS		ANALOG INPUT‡	A/D CONVERSION RESULT
	d6	d7		
Differential configuration	1	1	±6 V	full-scale
Analog input = IN+ − IN−	0	0		
= AUX IN+ − AUX IN−	1	0	±3 V	full-scale
	0	1	±1.5 V	full-scale
Single-ended configuration	1	1	±3 V	half-scale
Analog input = IN+ − ANLG GND	0	0		
= AUX IN+ − ANLG GND	1	0	±3 V	full-scale
	0	1	±1.5 V	full-scale

‡In this example, V_{ref} is assumed to be 3 V. In order to minimize distortion, it is recommended that the analog input not exceed 0.1 dB below full scale.



R_{fb} = R for d6 = 1, d7 = 1
d6 = 0, d7 = 0
R_{fb} = 2R for d6 = 1, d7 = 0
R_{fb} = 4R for d6 = 0, d7 = 1

FIGURE 3. IN+ AND IN− GAIN CONTROL CIRCUITRY



R_{fb} = R for d6 = 1, d7 = 1
d6 = 0, d7 = 0
R_{fb} = 2R for d6 = 1, d7 = 0
R_{fb} = 4R for d6 = 0, d7 = 1

FIGURE 4. AUX IN+ AND AUX IN− GAIN CONTROL CIRCUITRY

(sin x)/x correction section

If the designer does not wish to use the on-board second-order (sin x)/x correction filter, correction can be accomplished in digital signal processor (DSP) software. (Sin x)/x correction can be accomplished easily and efficiently in digital signal processor (DSP) software. Excellent correction accuracy can be achieved to a band edge of 3000 Hz by using a first-order digital correction filter. The results, which are shown below, are typical of the numerical correction accuracy that can be achieved for sample rates of interest. The filter requires only seven instruction cycles per sample on the TMS320 DSPs. With a 200-ns instruction cycle, nine instructions per sample represents an overhead factor of 1.4% and 1.7% for sampling rates of 8000 Hz and 9600 Hz, respectively. This correction will add a slight amount of group delay at the upper edge of the 300–3000-Hz band.

(sin x)/x roll-off for a zero-order hold function

The (sin x)/x roll-off for the AIC DAC zero-order hold function at a band-edge frequency of 3000 Hz for the various sampling rates is shown in the table below.

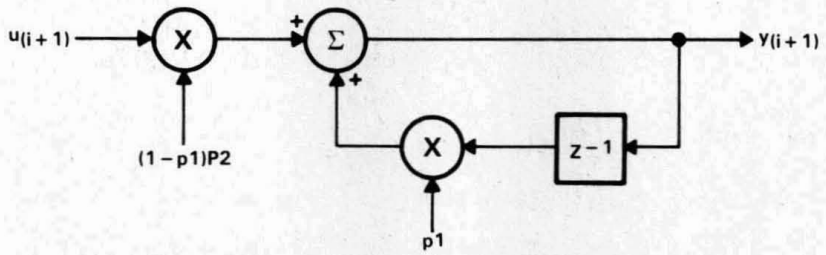
TABLE 4. (sin x)/x ROLL-OFF

f_s (Hz)	$20 \log \frac{\sin \pi f/f_s}{\pi f/f_s}$ (f = 3000 Hz) (dB)
7200	−2.64
8000	−2.11
9600	−1.44
14400	−0.63
19200	−0.35

Note that the actual AIC (sin x)/x roll-off will be slightly less than the above figures, because the AIC has less than a 100% duty cycle hold interval.

correction filter

To compensate for the (sin x)/x roll-off of the AIC, a first-order correction filter shown below, is recommended.



The difference equation for this correction filter is:

$$y_{i+1} = p2(1-p1)\,(u_{i+1}) + p1\,y_i$$

where the constant p1 determines the pole locations.

The resulting squared magnitude transfer function is:

$$|H(f)|^2 = \frac{p2^2\,(1-p1)^2}{1 - 2p1\cos(2\pi f/f_s) + p1^2}$$

correction results

Table 5 below shows the optimum p values and the corresponding correction results for 8000-Hz and 9600-Hz sampling rates.

TABLE 5

f (Hz)	ERROR (dB) f_S = 8000 Hz p1 = −0.14813 p2 = 0.9888	ERROR (dB) f_S = 9600 Hz p1 = −0.1307 p2 = 0.9951
300	−0.099	−0.043
600	−0.089	−0.043
900	−0.054	0
1200	−0.002	0
1500	0.041	0
1800	0.079	0.043
2100	0.100	0.043
2400	0.091	0.043
2700	−0.043	0
3000	−0.102	−0.043

TMS320 software requirements

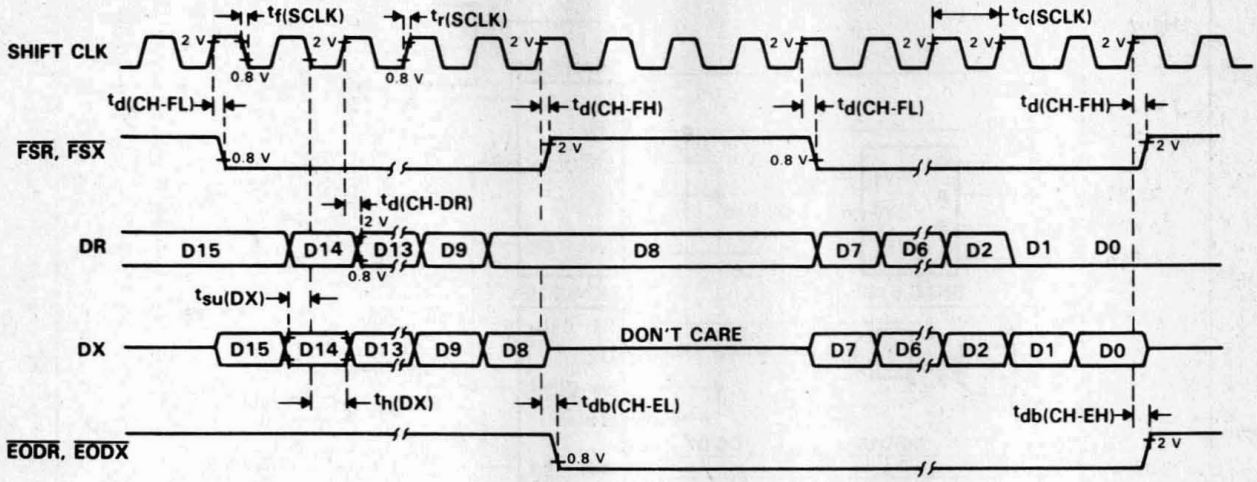
The digital correction filter equation can be written in state variable form as follows:

$$Y = k1Y + k2U$$

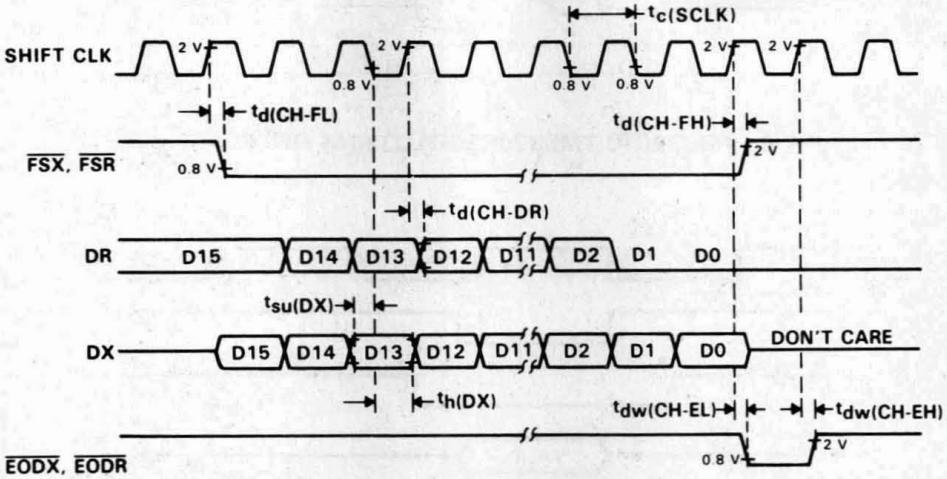
where k1 equals p1 (from the preceding page), k2 equals (1 − p1)p2 (from the preceding page), Y is the filter state, and U is the next I/O sample. The coefficients k1 and k2 must be represented as 16-bit integers. The SACH instruction (with the proper shift) will yield the correct result. With the assumption that the TMS320 processor page pointer and memory configuration are properly initialized, the equation can be executed in seven instructions or seven cycles with the following program:

```
ZAC
LT K2
MPY U
LTA K1
MPY Y
APAC
SACH (dma), (shift)
```

byte-mode timing



word-mode timing



shift-clock timing

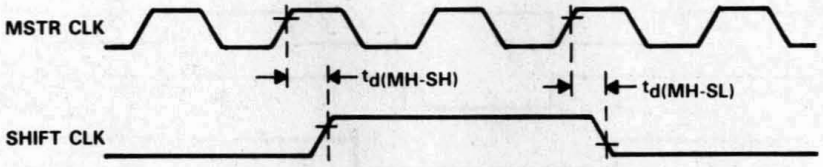


FIGURE 5. SERIAL PORT TIMING

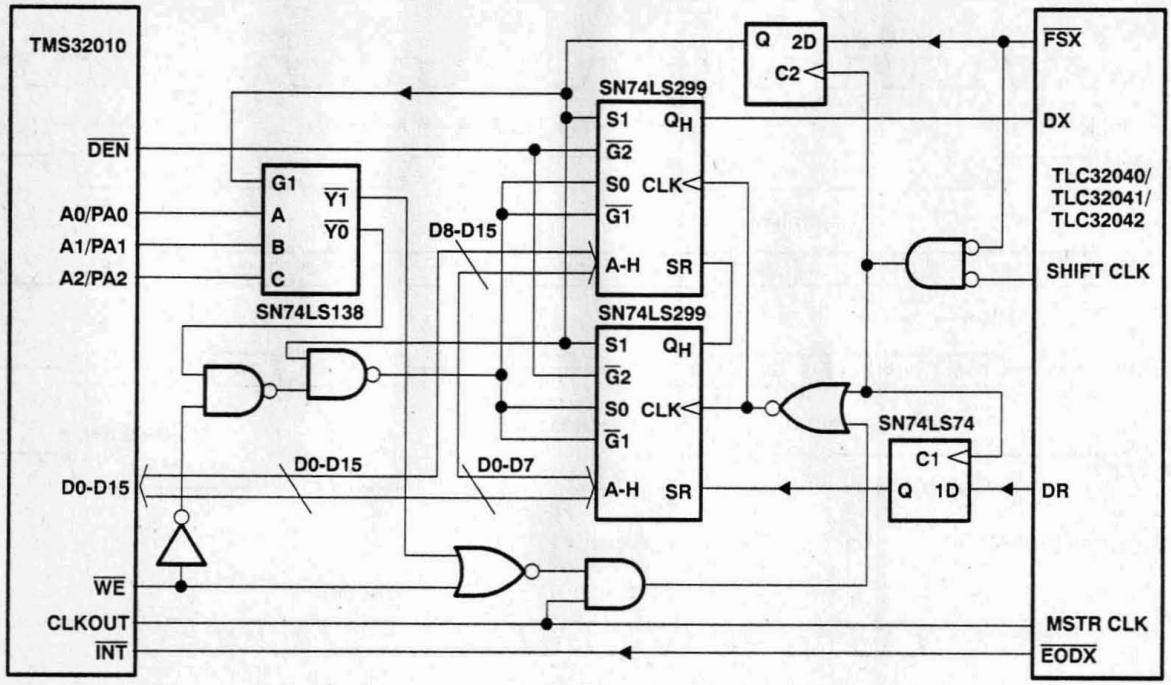
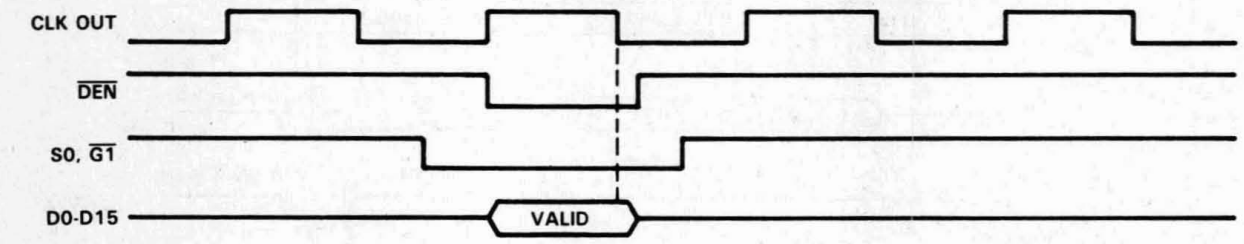


FIGURE 6. TMS32010/TMS320C15-TLC32044 INTERFACE CIRCUIT

in instruction timing



out instruction timing

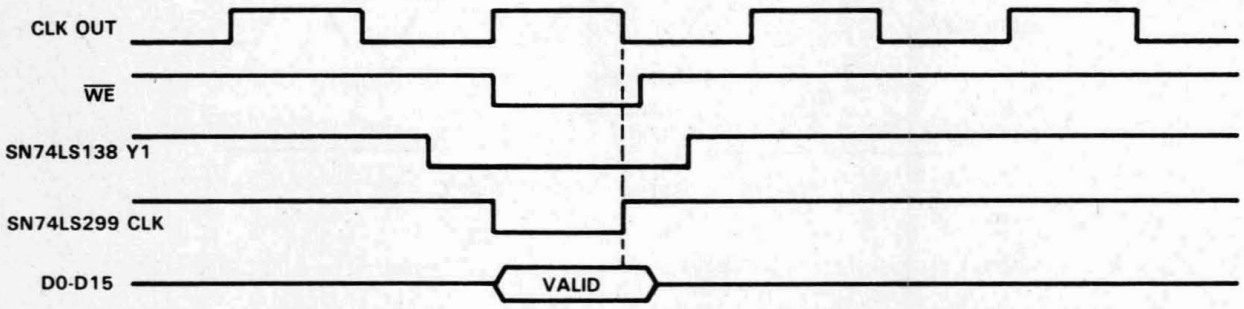


FIGURE 7. TMS32010/TMS320C15-TLC32044 INTERFACE TIMING

TYPICAL CHARACTERISTICS

AIC TRANSMIT AND RECEIVE LOW-PASS FILTER

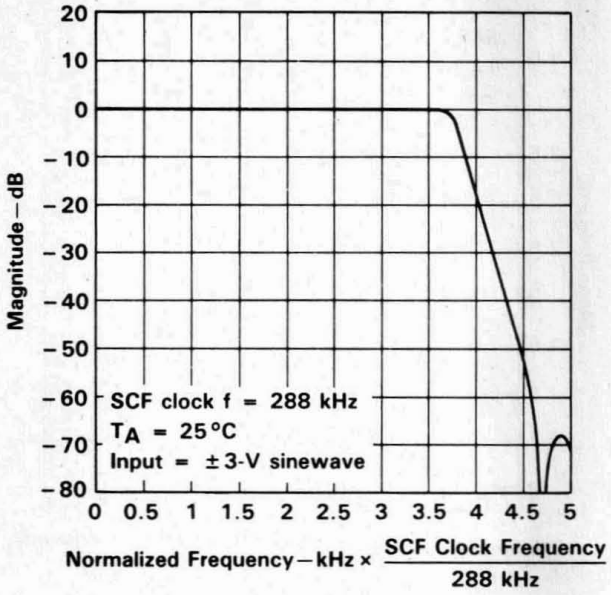


FIGURE 8

AIC TRANSMIT AND RECEIVE LOW-PASS FILTER

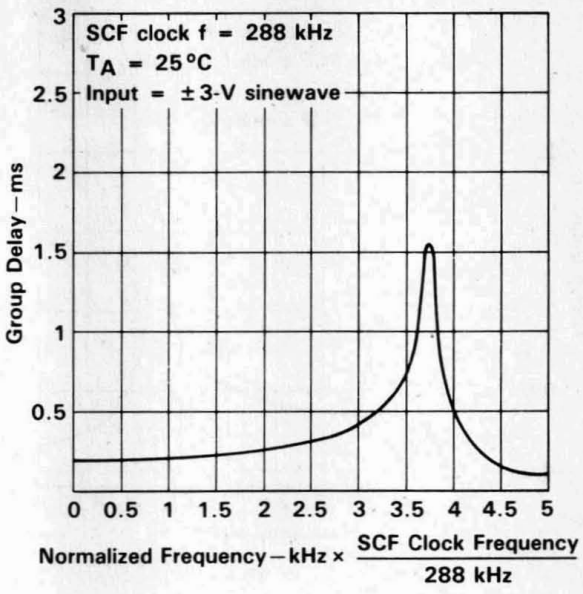


FIGURE 9

AIC RECEIVE-CHANNEL BANDPASS FILTER

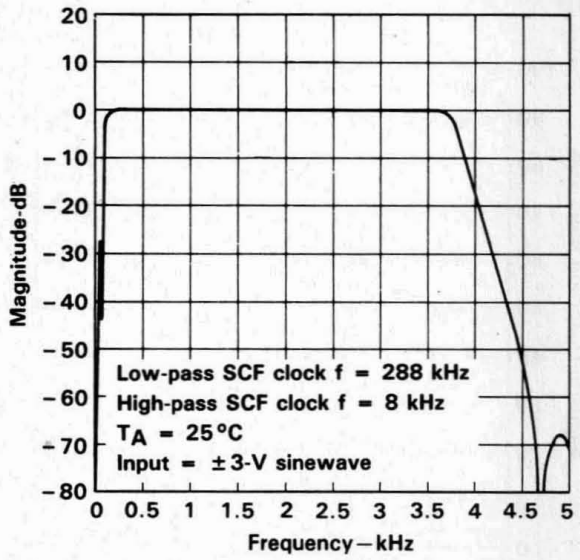


FIGURE 10

AIC RECEIVE-CHANNEL HIGH-PASS FILTER

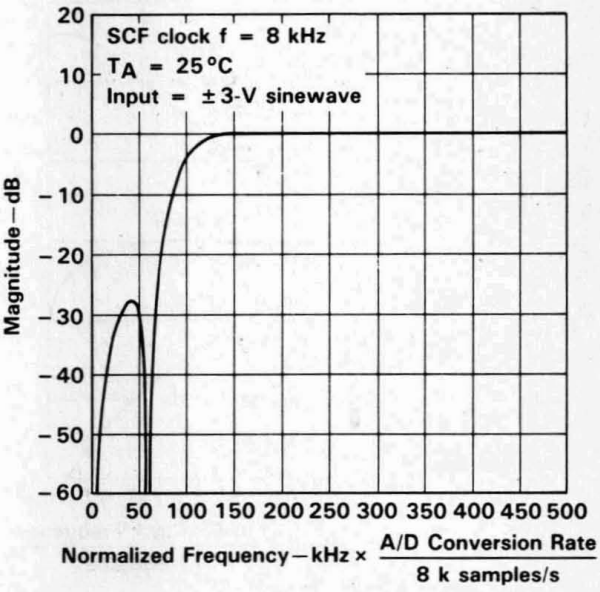


FIGURE 11

TYPICAL CHARACTERISTICS

AIC RECEIVE CHANNEL BANDPASS FILTER

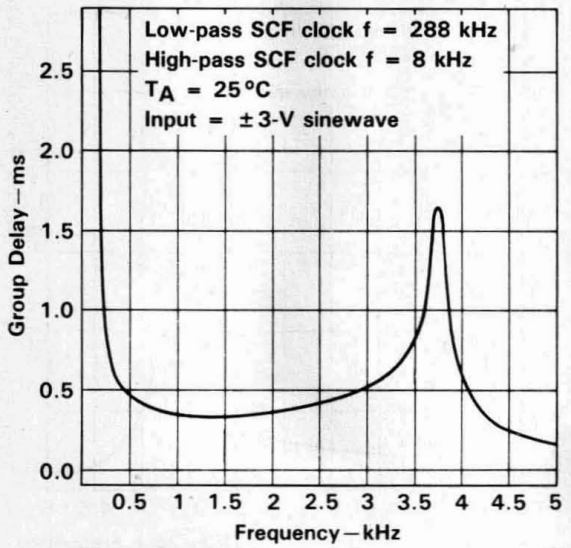


FIGURE 12

AIC (SIN X)/X CORRECTION FILTER

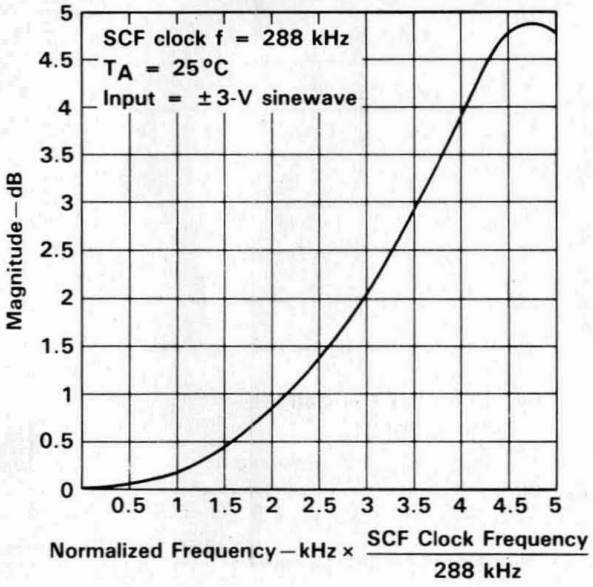


FIGURE 13

(SIN X)/X CORRECTION FILTER

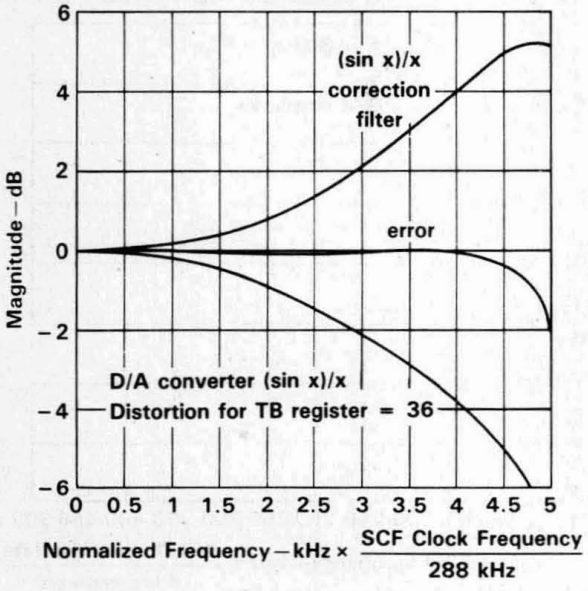


FIGURE 14

A/D SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL

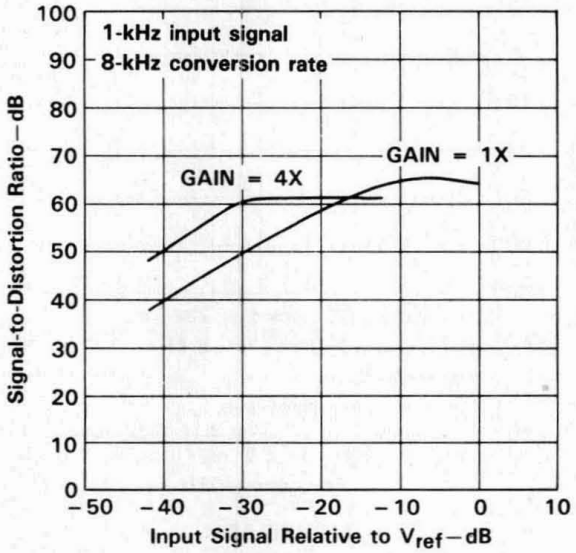


FIGURE 15

TYPICAL CHARACTERISTICS

A/D GAIN TRACKING
(GAIN RELATIVE TO GAIN AT 0 dB INPUT SIGNAL)

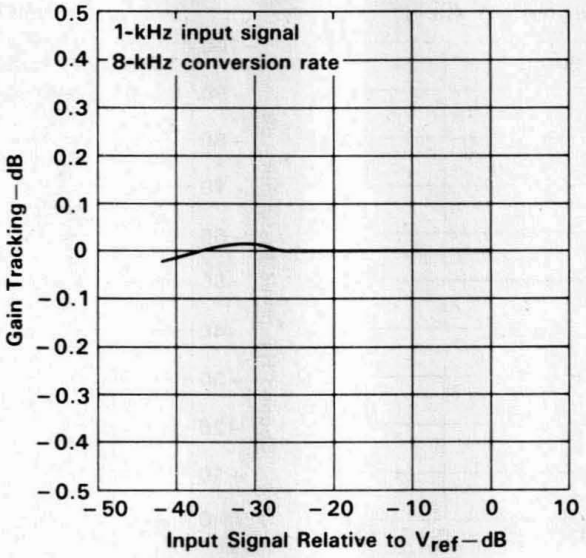


FIGURE 16

D/A CONVERTER SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL LEVEL

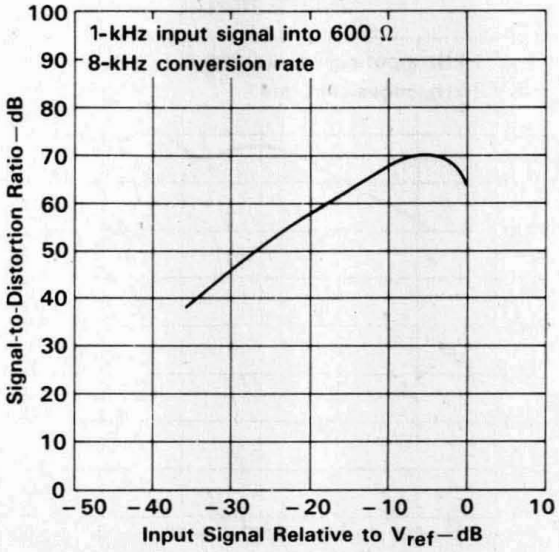


FIGURE 17

TYPICAL CHARACTERISTICS

D/A GAIN TRACKING
(GAIN RELATIVE TO GAIN
AT 0 dB INPUT SIGNAL LEVEL)

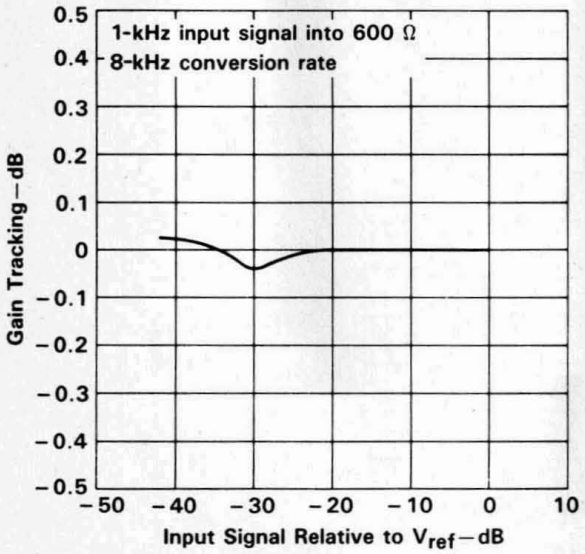


FIGURE 18

A/D SECOND HARMONIC DISTORTION
vs
INPUT SIGNAL

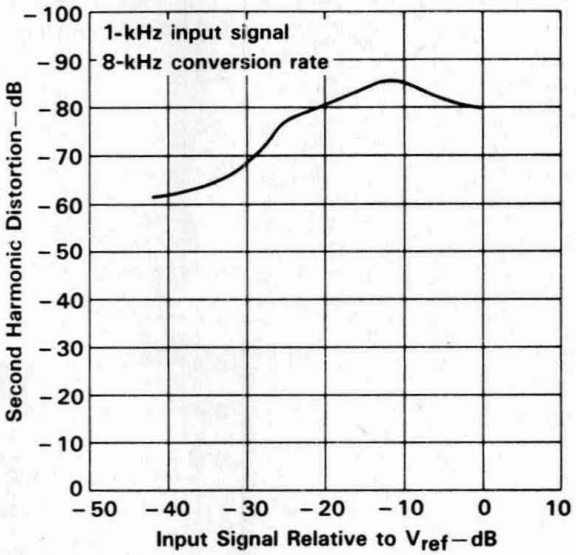


FIGURE 19

D/A SECOND HARMONIC DISTORTION
vs
INPUT SIGNAL

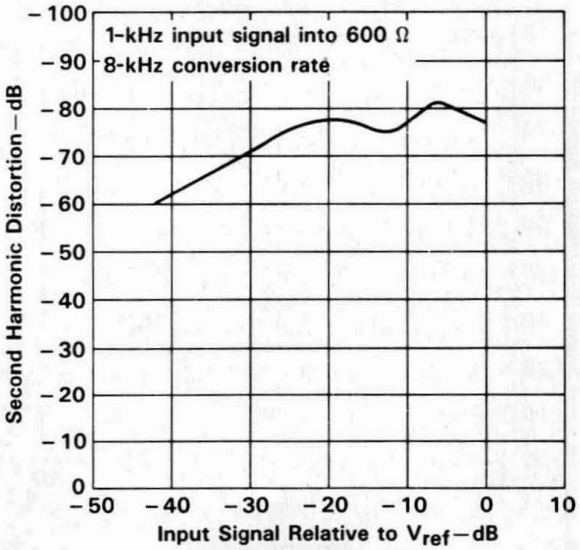


FIGURE 20

TYPICAL CHARACTERISTICS

A/D THIRD HARMONIC DISTORTION
vs
INPUT SIGNAL

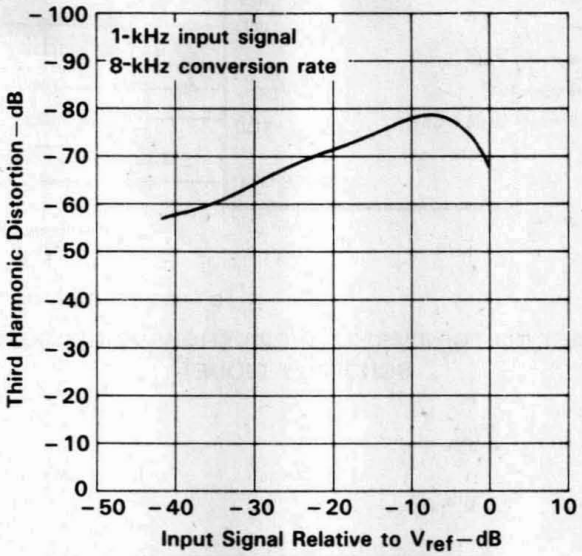


FIGURE 21

D/A THIRD HARMONIC DISTORTION
vs
INPUT SIGNAL

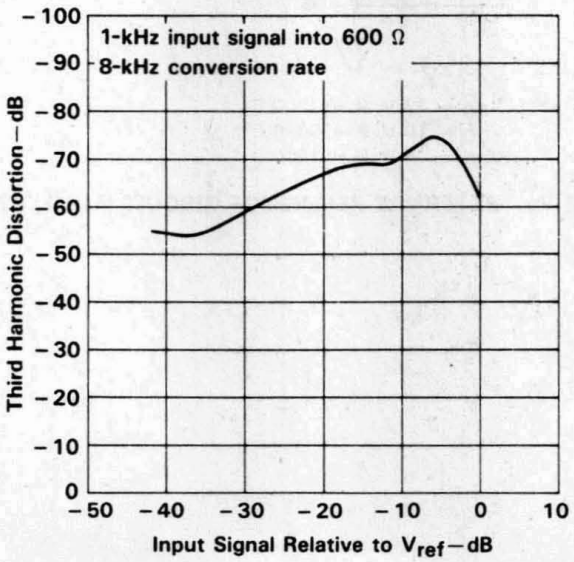
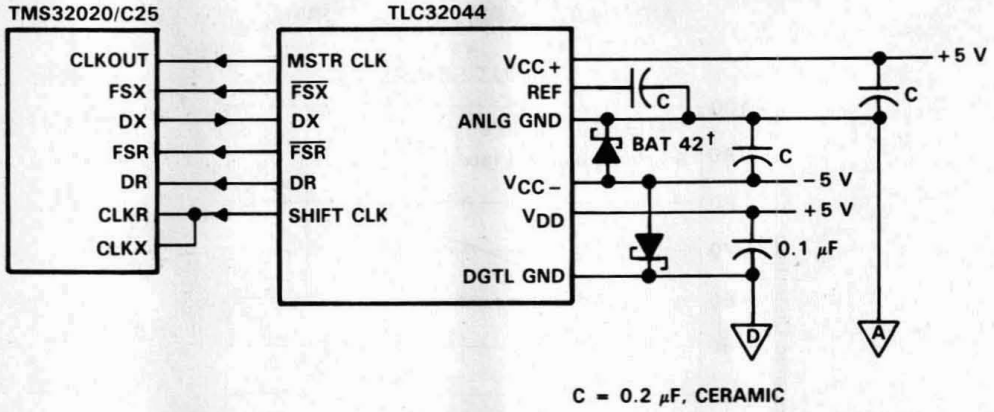


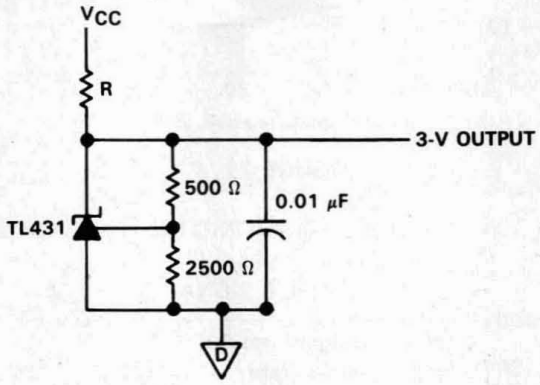
FIGURE 22

TYPICAL APPLICATION INFORMATION



C = 0.2 μF, CERAMIC

FIGURE 23. AIC INTERFACE TO THE TMS32020/C25 SHOWING DECOUPLING CAPACITORS AND SCHOTTKY DIODE†



FOR: V_{CC} = 12 V, R = 7200 Ω
V_{CC} = 10 V, R = 5600 Ω
V_{CC} = 5 V, R = 1600 Ω

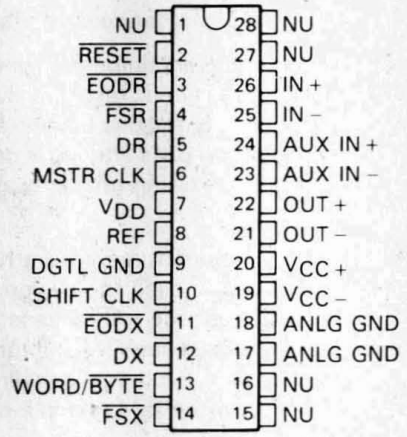
FIGURE 24. EXTERNAL REFERENCE CIRCUIT FOR TLC32044

†Thomson Semiconductors

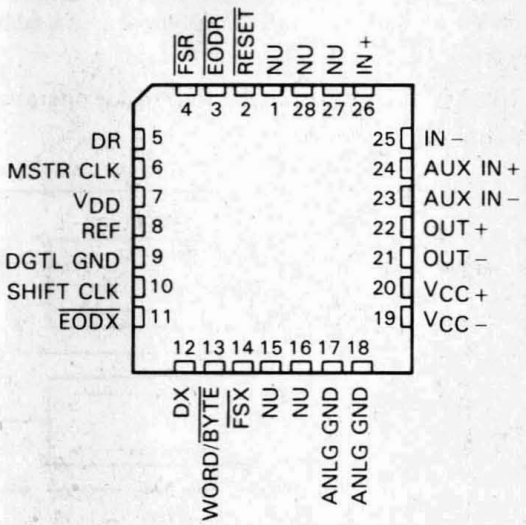
D3495, MAY 1990

- **Advanced LinCMOS™ Silicon-Gate Process Technology**
- **14-Bit Dynamic Range ADC and DAC**
- **16-Bit Dynamic Range Input with Programmable Gain**
- **Variable ADC and DAC Sampling Rate Up to 19,200 Samples per Second**
- **Switched-Capacitor Antialiasing Input Filter and Output-Reconstruction Filter**
- **Serial Port for Direct Interface to SMJ320E14, SMJ32020, SMJ320C25, and SMJ320C30 Digital Processors**
- **Synchronous or Asynchronous ADC and DAC Conversion Rates with Programmable Incremental ADC and DAC Conversion Timing Adjustments**
- **Serial Port Interface to SN54299 Serial-to-Parallel Shift Register for Parallel Interface to SMJ320C10, SMJ320C15, SMJ320E15 or Other Digital Processors**
- **Internal Reference for Normal Operation and External Purposes, or Can Be Overridden by External Reference**

J PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NU – Nonusable; no external connection should be made to these pins. See Table 2.

description

The TLC32044M is a complete analog-to-digital and digital-to-analog input/output system on a single monolithic CMOS chip. This device integrates a bandpass switched-capacitor antialiasing input filter, a 14-bit-resolution A/D converter, four microprocessor-compatible serial port modes, a 14-bit-resolution D/A converter, and a low-pass switched-capacitor output-reconstruction filter. The device offers numerous combinations of Master Clock input frequencies and conversion/sampling rates, which can be changed via digital processor control.

Typical applications for this IC include speech encryption for digital transmission, speech recognition/storage systems, speech synthesis, modems (7.2-, 8-, 9.6-, 14.4-, and 19.2-kHz sampling rate), analog interface for digital signal processors (DSPs), industrial process control, biomedical instrumentation, acoustical signal processing, spectral analysis, data acquisition, and instrumentation recorders. Four serial modes, which allow direct interface to the SMJ320E14, SMJ32020, SMJ320C25, and SMJ320C30 digital signal processors, are provided. Also, when the transmit and receive sections of the Analog Interface Circuit (AIC) are operating synchronously, it will interface to two SN54299 serial-to-parallel shift registers. These serial-to-parallel shift registers can then interface in parallel to the SMJ320C10, SMJ320C15, SMJ320E15 other digital signal processors, or external FIFO circuitry. Output data pulses are emitted to inform the processor that data transmission is complete or to allow the DSP to differentiate between two transmitted

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description (continued)

bytes. A flexible control scheme is provided so that the functions of the IC can be selected and adjusted coincidentally with signal processing via software control.

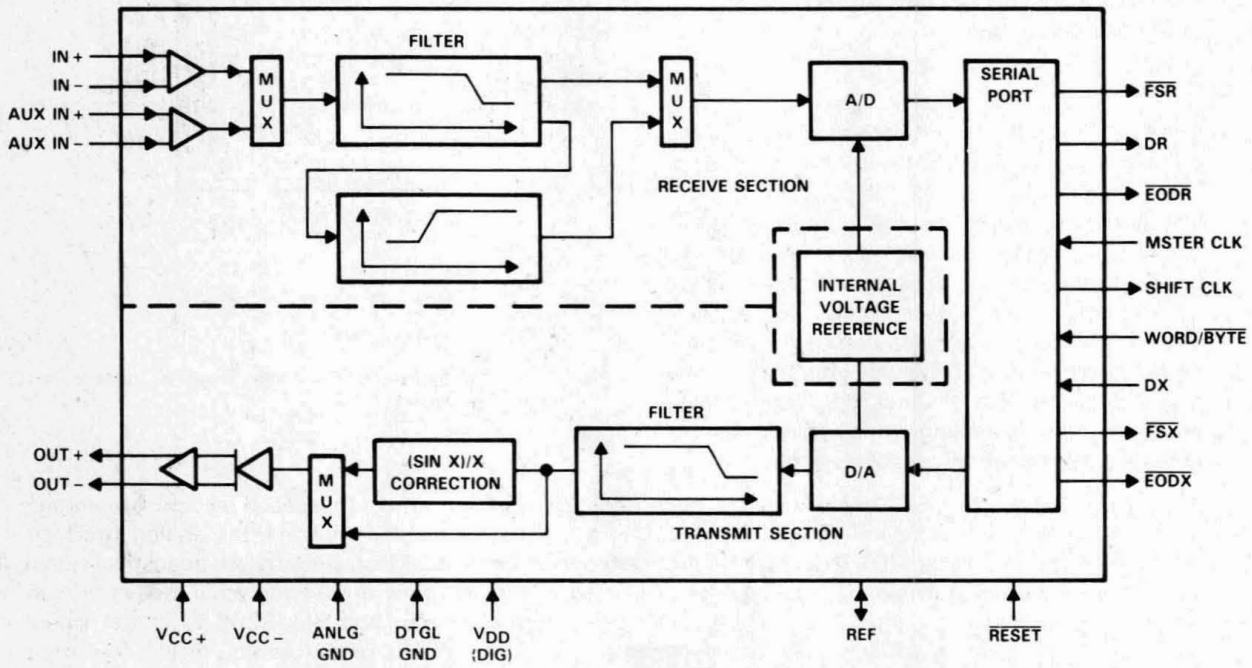
The antialiasing input filter comprises eighth-order and fourth-order CC-type (Chebyshev/elliptic transitional) low-pass and high-pass filters, respectively. The input filter is implemented in switched-capacitor technology and is preceded by a continuous time filter to eliminate any possibility of aliasing caused by sampled data filtering. When only low-pass filtering is desired, the high-pass filter can be switched out of the signal path. A selectable, auxiliary, differential analog input is provided for applications where more than one analog input is required.

The A/D and D/A architectures ensure no missing codes and monotonic operation. An internal voltage reference is provided to ease the design task and to provide complete control over the performance of the IC. The internal voltage reference is brought out to a pin and is available to the designer. Separate analog and digital voltage supplies and grounds are provided to minimize noise and ensure a wide dynamic range. Also, the analog circuit path contains only differential circuitry to keep noise to an absolute minimum. The only exception is the DAC sample-and-hold, which utilizes pseudo-differential circuitry.

The output-reconstruction filter is an eighth-order CC-type (Chebyshev/elliptic transitional low-pass filter) followed by a second-order (sin x)/x correction filter) and is implemented in switched-capacitor technology. This filter is followed by a continuous-time filter to eliminate images of the digitally encoded signal. The on-board (sin x)/x correction filter can be switched out of the signal path using digital signal processor control, if desired.

The TLC32044M is characterized for operation from −55°C to 125°C.

functional block diagram



PRINCIPLES OF OPERATION

analog input

Two sets of analog inputs are provided. Normally, the IN+ and IN− input set is used; however, the auxiliary input set, AUX IN+ and AUX IN−, can be used if a second input is required. Each input set can be operated in either differential or single-ended modes, since sufficient common-mode range and rejection are provided. The gain for the IN+, IN−, AUX IN+, and AUX IN− inputs can be programmed to be either 1, 2, or 4 (see Table 2). Either input circuit can be selected via software control. It is important to note that a wide dynamic range is assured by the differential internal analog architecture and by the separate analog and digital voltage supplies and grounds.

A/D bandpass filter, A/D bandpass filter clocking, and A/D conversion timing

The A/D high-pass filter can be selected or bypassed via software control. The frequency response of this filter is presented in the following pages. This response results when the switched-capacitor filter clock frequency is 288 kHz and the A/D sample rate is 8 kHz. Several possible options can be used to attain a 288-kHz switched-capacitor filter clock. When the filter clock frequency is not 288 kHz, the low-pass filter transfer function is frequency-scaled by the ratio of the actual clock frequency to 288 kHz. The ripple bandwidth and 3-dB low-frequency roll-off points of the high-pass section are 150 and 100 Hz, respectively. However, the high-pass section low-frequency roll-off is frequency-scaled by the ratio of the A/D sample rate to 8 kHz.

The A/D conversion rate is then attained by frequency-dividing the 288-kHz bandpass switched-capacitor filter clock with the RX Counter B. Thus, unwanted aliasing is prevented because the A/D conversion rate is an integral submultiple of the bandpass switched-capacitor filter sampling rate, and the two rates are synchronously locked.

A/D converter performance specifications

Fundamental performance specifications for the A/D converter circuitry are presented in the A/D converter operating characteristics section of this data sheet. The realization of the A/D converter circuitry with switched-capacitor techniques provides an inherent sample-and-hold.

analog output

The analog output circuitry is an analog output power amplifier. Both noninverting and inverting amplifier outputs are brought out of the IC. This amplifier can drive transformer hybrids or low-impedance loads directly in either a differential or single-ended configuration.

D/A low-pass filter, D/A low-pass filter clocking, and D/A conversion timing

The frequency response of this filter is presented in the following pages. This response results when the low-pass switched-capacitor filter clock frequency is 288 kHz. Like the A/D filter, the transfer function of this filter is frequency-scaled when the clock frequency is not 288 kHz. A continuous-time filter is provided on the output of the (sin x)/x filter to eliminate the periodic sample data signal information, which occurs at multiples of the 288-kHz switched-capacitor filter clock. The continuous time filter also greatly attenuates any switched-capacitor clock feedthrough.

The D/A conversion rate is attained by frequency-dividing the 288-kHz switched-capacitor filter clock with TX Counter B. Thus, unwanted aliasing is prevented because the D/A conversion rate is an integral submultiple of the switched-capacitor low-pass filter sampling rate, and the two rates are synchronously locked.

PRINCIPLES OF OPERATION (continued)

asynchronous versus synchronous operation

If the transmit section of the AIC (low-pass filter and DAC) and receive section (bandpass filter and ADC) are operated asynchronously, the low-pass and bandpass filter clocks are independently generated from the Master Clock signal. Also, the D/A and A/D conversion rates are independently determined. If the transmit and receive sections are operated synchronously, the low-pass filter clock drives both low-pass and bandpass filters. In synchronous operation, the A/D conversion timing is derived from, and is equal to, the D/A conversion timing. (See description of the WORD/$\overline{\text{BYTE}}$ pin in the Pin Functional Description Section.)

D/A converter performance specifications

Fundamental performance specifications for the D/A converter circuitry are presented in the D/A converter operating characteristics section of the data sheet. The D/A converter has a sample-and-hold that is realized with a switched-capacitor ladder.

system frequency response correction

(Sin x)/x correction for the D/A converter's zero-order sample-and-hold output can be provided by an on-board second-order (sin x)/x correction filter. This (sin x)/x correction filter can be inserted into or deleted from the signal path by digital signal processor control. When inserted, the (sin x)/x correction filter follows the switched-capacitor low-pass filter. When the TB register (see Internal Timing Configuration section) equals 36, the correction results of Figures 11 and 12 will be obtained.

(Sin x)/x correction can also be accomplished by deleting the on-board second-order correction filter and performing the (sin x)/x correction in digital signal processor software. The system frequency response can be corrected via DSP software to ± 0.1 dB accuracy to a band-edge of 3000 Hz for all sampling rates. This correction is accomplished with a first-order digital correction filter, which requires only seven SMJ320 instruction cycles. With a 200-ns instruction cycle, seven instructions represent an overhead factor of only 1.1% and 1.3% for sampling rates of 8 and 9.6 kHz, respectively (see the (sin x)/x Correction Section for more details).

serial port

The serial port has four possible modes that are described in detail in the Functional Pin Description Section. These modes are briefly described below and in the Functional Description for Pin 13, WORD/$\overline{\text{BYTE}}$.

1. The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the DSP in two 8-bit bytes.
2. The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the SMJ32020, SMJ320C25, and the SMJ320C30.
3. The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the DSP in two 8-bit bytes.
4. The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the SMJ32020, SMJ320C25, SMJ320C30, or two SN54299 serial-to-parallel shift registers, which can then interface in parallel to the SMJ320C10, SMJ320C15, SMJ320E15, to any other digital signal processor, or to external FIFO circuitry.

operation of TLC32044M with internal voltage reference

The internal reference of the TLC32044M eliminates the need for an external voltage reference and provides overall circuit cost reduction. Thus, the internal reference eases the design task and provides complete

PRINCIPLES OF OPERATION (continued)

control over the performance of the IC. The internal reference is brought out to a pin and is available to the designer. To keep the amount of noise on the reference signal to a minimum, an external capacitor may be connected between REF and ANLG GND.

operation of TLC32044M with external voltage reference

The REF pin may be driven from an external reference circuit if so desired. This external circuit must be capable of supplying 250 μA and must be adequately protected from noise such as crosstalk from the analog input.

reset

A reset function is provided to initiate serial communications between the AIC and DSP and to allow fast, cost-effective testing during manufacturing. The reset function will initialize all AIC registers, including the control register. After a negative-going pulse on the $\overline{\text{RESET}}$ pin, the AIC will be initialized. This initialization allows normal serial port communications activity to occur between AIC and DSP (see AIC DX Data Word Format section).

loopback

This feature allows the user to test the circuit remotely. In loopback, the OUT+ and OUT− pins are internally connected to the IN+ and IN− pins. Thus, the DAC bits (d15 to d2), which are transmitted to the DX pin, can be compared with the ADC bits (d15 to d2), which are received from the DR pin. An ideal comparison would be that the bits on the DR pin equal the bits on the DX pin. However, in practice there will be some difference in these bits due to the ADC and DAC output offsets.

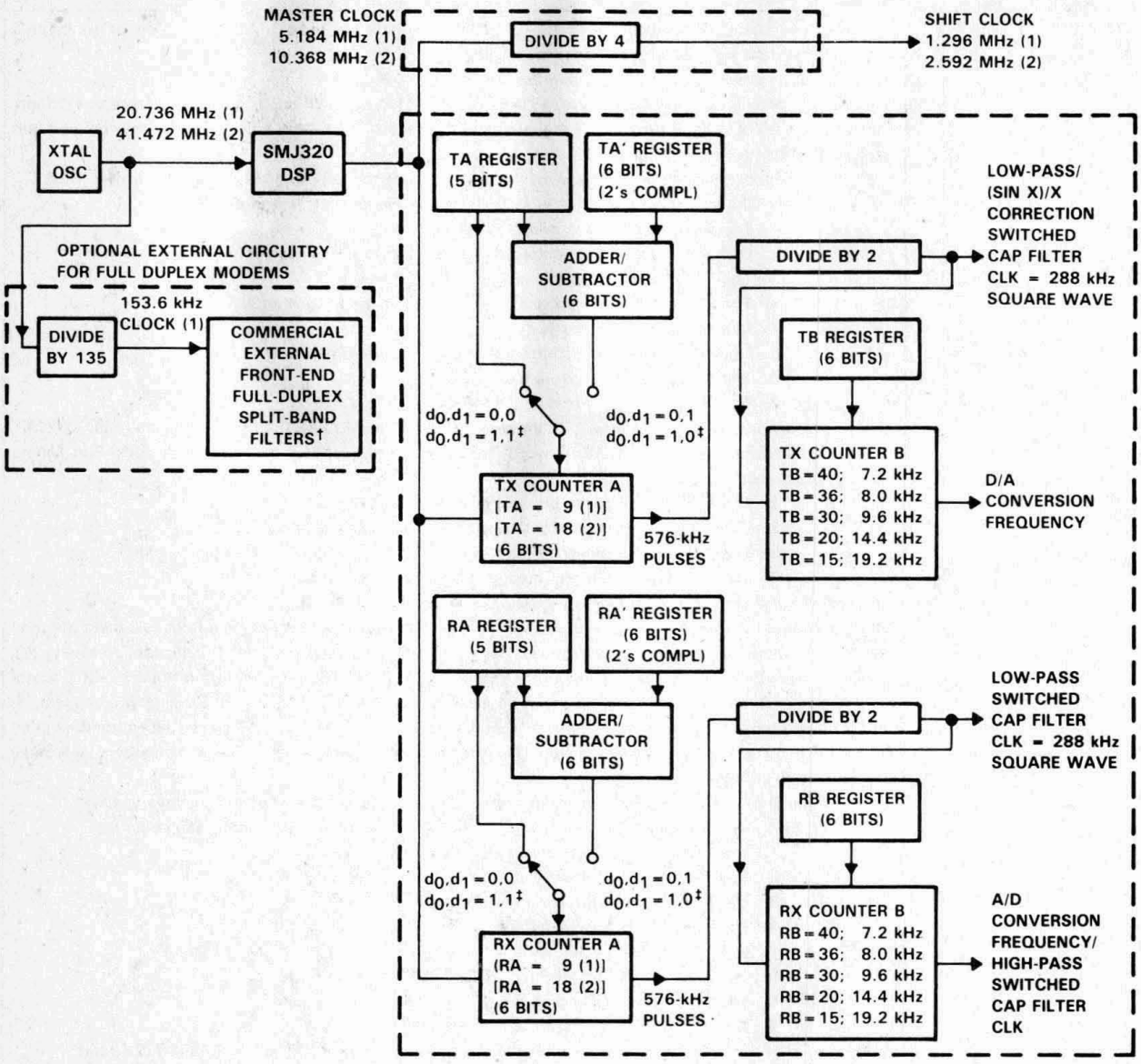
The loopback feature is implemented with digital signal processor control by transmitting the appropriate serial port bit to the control register (see AIC Data Word Format section).

PIN NAME	PIN NO.	I/O	DESCRIPTION
ANLG GND	17,18		Analog ground return for all internal analog circuits. Not internally connected to DGTL GND.
AUX IN+	24	I	Noninverting auxiliary analog input stage. This input can be switched into the bandpass filter and A/D converter path via software control. If the appropriate bit in the Control register is a 1, the auxiliary inputs will replace the IN+ and IN− inputs. If the bit is a 0, the IN+ and IN− inputs will be used (see the AIC DX Data Word Format section).
AUX IN−	23	I	Inverting auxiliary analog input (see the above AUX IN+ pin description).
DGTL GND	9		Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
DR	5	O	This pin is used to transmit the ADC output bits from the AIC to the SMJ320 serial port. This transmission of bits from the AIC to the SMJ320 serial port is synchronized with the SHIFT CLK signal.
DX	12	I	This pin is used to receive the DAC input bits and timing and control information from the SMJ320. This serial transmission from the SMJ320 serial port to the AIC is synchronized with the SHIFT CLK signal.
$\overline{\text{EODR}}$	3	O	End of data receive. (See the WORD/$\overline{\text{BYTE}}$ pin description and the Serial Port Timing Diagram.) During the word-mode timing, this signal is a low-going pulse that occurs immediately after the 16 bits of A/D information have been transmitted from the AIC to the SMJ320 serial port. This signal can be used to interrupt a microprocessor upon completion of serial communications. Also, this signal can be used to strobe and enable external serial-to-parallel shift registers, latches, or external FIFO RAM, and to facilitate parallel data bus communications between the AIC and the serial-to-parallel shift registers. During the byte-mode timing, this signal goes low after the first byte has been transmitted from the AIC to the SMJ320 serial port and is kept low until the second byte has been transmitted. The DSP can use this low-going signal to differentiate between the two bytes as to which is first and which is second. $\overline{\text{EODR}}$ does not occur after secondary communication.

PIN NAME	PIN NO.	I/O	DESCRIPTION
$\overline{EODX}$	11	O	End of data transmit. (See the WORD/$\overline{BYTE}$ pin description and the Serial Port Timing Diagram.) During the word-mode timing, this signal is a low-going pulse that occurs immediately after the 16 bits of D/A converter and control or register information have been transmitted from the SMJ320 serial port to the AIC. This signal can be used to interrupt a microprocessor upon the completion of serial communications. Also, this signal can be used to strobe and enable external serial-to-parallel shift registers, latches, or an external FIFO RAM, and to facilitate parallel data-bus communications between the AIC and the serial-to-parallel shift registers. During the byte-mode timing, this signal goes low after the first byte has been transmitted from the SMJ320 serial port to the AIC and is kept low until the second byte has been transmitted. The DSP can use this low-going signal to differentiate between the two bytes as to which is first and which is second.
$\overline{FSR}$	4	O	Frame sync receive. In the serial transmission modes, which are described in the WORD/$\overline{BYTE}$ pin description, the $\overline{FSR}$ pin is held low during bit transmission. When the $\overline{FSR}$ pin goes low, the SMJ320 serial port will begin receiving bits from the AIC via the DR pin of the AIC. The most significant DR bit will be present on the DR pin before $\overline{FSR}$ goes low. (See Serial Port Timing and Internal Timing Configuration Diagrams.) $\overline{FSR}$ does not occur after secondary communications.
$\overline{FSX}$	14	O	Frame syn transmit. When this pin goes low, the SMJ320 serial port will begin transmitting bits to the AIC via the DX pin of the AIC. In all serial transmission modes, which are described in the WORD/$\overline{BYTE}$ pin description, the $\overline{FSX}$ pin is held low during bit transmission (see Serial Port Timing and Internal Timing Configuration Diagrams).
IN+	26	I	Noninverting input to analog input amplifier stage
IN−	25	I	Inverting input to analog input amplifier stage
MSTR CLK	6	I	The Master Clock signal is used to derive all the key logic signals of the AIC, such as the Shift Clock, the switched-capacitor filter clocks, and the A/D and D/A timing signals. The Internal Timing Configuration diagram shows how these key signals are derived. The frequencies of these key signals are synchronous submultiples of the Master Clock frequency to eliminate unwanted aliasing when the sampled analog signals are transferred between the switched-capacitor filters and the A/D and D/A converters (see the Internal Timing Configuration).
OUT+	22	O	Noninverting output of analog output power amplifier. Can drive transformer hybrids or high-impedance loads directly in either a differential or a single-ended configuration.
OUT−	21	O	Inverting output of analog output power amplifier. Functionally identical with and complementary to OUT+.
REF	8	I/O	The internal voltage reference is brought out on this pin. An external voltage reference can also be applied to this pin.
$\overline{RESET}$	2	I	A reset function is provided to initialize the TA, TA′, TB, RA, RA′, RB, and control registers. This reset function initiates serial communications between the AIC and DSP. The reset function will initialize all AIC registers including the control register. After a negative-going pulse on the $\overline{RESET}$pin, the AIC registers will be initialized to provide an 8-kHz data conversion rate for a 5.184-MHz master clock input signal. The conversion rate adjust registers, TA′ and RA′, will be reset to 1. The CONTROL register bits will be reset as follows (see AIC DX Data Word Format section). d9 = 1, d7 = 1, d6 = 1, d5 = 1, d4 = 0, d3 = 0, d2 = 1 This initialization allows normal serial-port communication to occur between AIC and DSP.
SHIFT CLK	10	O	The Shift Clock signal is obtained by dividing the Master Clock signal frequency by four. This signal is used to clock the serial data transfers of the AIC, described in the WORD/$\overline{BYTE}$ pin description below (see the Serial Port Timing and Internal Timing Configuration diagram).
V_{DD}	7		Digital supply voltage, 5 V ±5%
V_{CC+}	20		Positive analog supply voltage, 5 V ±5%
V_{CC-}	19		Negative analog supply voltage, −5 V ±5%

PIN NAME	NO.	I/O	DESCRIPTION
WORD/$\overline{\text{BYTE}}$	13	I	This pin, in conjunction with a bit in the CONTROL register, is used to establish one of four serial modes. These four serial modes are described below. *AIC transmit and receive sections are operated asynchronously.* The following description applies when the AIC is configured to have asynchronous transmit and receive sections. If the appropriate data bit in the Control register is a 0 (see the AIC DX Data Word Format), the transmit and receive sections will be asynchronous. L Serial port directly interfaces with the serial port of the DSP and communicates in two 8-bit bytes. The operation sequence is as follows (see Serial Port Timing diagrams). 1. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought low. 2. One 8-bit byte is transmitted or one 8-bit byte is received. 3. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pin is brought low. 4. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin emits a positive frame-sync pulse that is four Shift Clock cycles wide. 5. One 8-bit byte is transmitted or one 8-bit byte is received. 6. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pin is brought high. 7. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought high. H Serial port directly interfaces with the serial ports of the SMJ32020, SMJ320C25, and SMJ320C30, and communicates in one 16-bit word. The operation sequence is as follows (see Serial Port Timing diagrams): 1. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought low. 2. One 16-bit word is transmitted or one 16-bit word is received. 3. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought high. 4. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pin emits a low-going pulse. *AIC transmit and receive sections are operated synchronously.* If the appropriate data bit in the Control register is a 1, the transmit and receive sections will be configured to be synchronous. In this case, the bandpass switched-capacitor filter and the A/D conversion timing will be derived from the TX Counter A, TX Counter B, and TA, TA′, and TB registers, rather than the RX Counter A, RX Counter B, and RA, RA′, and RB registers. In this case, the AIC $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ timing will be identical during primary data communication; however, $\overline{\text{FSR}}$ will not be asserted during secondary data communication since there is no new A/D conversion result. The synchronous operation sequences are as follows (see Serial Port Timing diagrams). L Serial port directly interfaces with the serial port of the DSP and communicates in two 8-bit bytes. The operation sequence is as follows (see Serial Port Timing diagrams): 1. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought low. 2. One 8-bit byte is transmitted and one 8-bit byte is received. 3. The $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ pins are brought low. 4. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins emit positive frame-sync pulses that are four Shift Clock cycles wide. 5. One 8-bit byte is transmitted and one 8-bit byte is received. 6. The $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ pins are brought high. 7. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought high. H Serial port directly interfaces with the serial ports of the SMJ32020, SMJ320C25, and SMJ320C30, and communicates in one 16-bit word. The operation sequence is as follows (see Serial Port Timing diagrams): 1. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought low. 2. One 16-bit word is transmitted and one 16-bit word is received. 3. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought high. 4. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pins emit low-going pulses. Since the transmit and receive sections of the AIC are now synchronous, the AIC serial port, with additional NOR and AND gates, will interface to two SN54299 serial-to-parallel shift registers. Interfacing the AIC to the SN54299 shift register allows the AIC to interface to an external FIFO RAM and facilitates parallel, data bus communications between the AIC and the digital signal processor. The operation sequence is the same as the above sequence (see Serial Port Timing diagrams).

INTERNAL TIMING CONFIGURATION



NOTE: Frequency 1, 20.736 MHz, is used to show how 153.6 kHz (for a commercially available modem split-band filter clock), popular speech and modem sampling signal frequencies, and an internal 288-kHz switched-capacitor filter clock can be derived synchronously and as submultiples of the crystal oscillator frequency. Since these derived frequencies are synchronous submultiples of the crystal frequency, aliasing does not occur as the sampled analog signal passes between the analog converter and switched-capacitor filter stages. Frequency 2, 41.472 MHz, is used to show that the AIC can work with high-frequency signals, which are used by high-speed digital signal processors.

†Split-band filtering can alternatively be performed after the analog input function via software in the SMJ320.

‡These control bits are described in the AIC DX Data Word Format section.

explanation of internal timing configuration

All of the internal timing of the AIC is derived from the high-frequency clock signal that drives the Master Clock input pin. The Shift Clock signal, which strobes the serial port data between the AIC and DSP, is derived by dividing the Master Clock input signal frequency by four.

Low-pass:

$$\text{SCF Clock Frequency (D/A or A/D Path)} = \frac{\text{Master Clock Frequency}}{2 \times \text{Contents of Counter A}}$$

$$\text{Conversion Frequency} = \frac{\text{SCF Clock Frequency (D/A or A/D Path)}}{\text{Contents of Counter B}}$$

High-pass:

$$\text{SCF Clock Frequency (A/D Path)} = \text{A/D Conversion Frequency}$$

$$\text{Shift Clock Frequency} = \frac{\text{Master Clock Frequency}}{4}$$

TX Counter A and TX Counter B, which are driven by the Master Clock signal, determine the D/A conversion timing. Similarly, RX Counter A and RX Counter B determine the A/D conversion timing. In order for the low-pass switched-capacitor filter in the D/A path to meet its transfer function specifications, the frequency of its clock input must be 288 kHz. If the clock frequency is not 288 kHz, the filter transfer function frequencies are frequency-scaled by the ratios of the clock frequency to 288 kHz. Thus, to obtain the specified filter response, the combination of Master Clock frequency and TX Counter A and RX Counter A values must yield a 288-kHz switched-capacitor clock signal. This 288-kHz clock signal can then be divided by the TX Counter B to establish the D/A conversion timing.

The transfer function of the bandpass switched-capacitor filter in the A/D path is a composite of its high-pass and low-pass section transfer functions. The high-frequency roll-off of the low-pass section will meet the bandpass filter transfer function specification when the low-pass section SCF is 288 kHz. Otherwise, the high-frequency roll-off will be frequency-scaled by the ratio of the high-pass section's SCF clock to 288 kHz. The low-frequency roll-off of the high-pass section will meet the bandpass filter transfer function specification when the A/D conversion rate is 8 kHz. Otherwise, the low-frequency roll-off of the high-pass section will be frequency-scaled by the ratio of the A/D conversion rate to 8 kHz.

TX Counter A and TX Counter B are reloaded every D/A conversion period, while RX Counter A and RX Counter B are reloaded every A/D conversion period. The TX Counter B and RX Counter B are loaded with the values in the TB and RB Registers, respectively. Via software control, the TX Counter A can be loaded with either the TA Register, the TA Register less the TA' Register, or the TA Register plus the TA' Register. By selecting the TA Register less the TA' Register option, the upcoming conversion timing will occur earlier by an amount of time that equals TA' times the signal period of the Master Clock. By selecting the TA Register plus the TA' Register option, the upcoming conversion timing will occur later by an amount of time that equals TA' times the signal period of the Master Clock. Thus, the D/A conversion timing can be advanced or retarded. An identical ability to alter the A/D conversion timing is provided. In this case, however, the RX Counter A can be programmed via software control with the RA Register, the RA Register less the RA' Register, or the RA Register plus the RA' Register.

The ability to advance or retard conversion timing is particularly useful for modem applications. This feature allows controlled changes in the A/D and D/A conversion timing. This feature can be used to enhance signal-to-noise performance, to perform frequency-tracking functions, and to generate nonstandard modem frequencies.

If the transmit and receive sections are configured to be synchronous (see WORD/$\overline{\text{BYTE}}$ pin description), then both the low-pass and bandpass switched-capacitor filter clocks are derived from TX Counter A. Also, both the D/A and A/D conversion timing are derived from the TX Counter A and TX Counter B. When the transmit and receive sections are configured to be synchronous, the RX Counter A, RX Counter B, RA Register, RA′ Register, and RB Registers are not used.

AIC DR or DX word bit pattern

A/D or D/A MSB, 1st bit sent — 1st bit sent of 2nd byte — A/D or D/A LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

AIC DX data word format section

d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	COMMENTS
primary DX serial communication protocol																
← d15 (MSB) through d2 go to the D/A converter register →														0	0	The TX and RX Counter A's are loaded with the TA and RA register values. The TX and RX Counter B's are loaded with TB and RB register values.
← d15 (MSB) through d2 go to the D/A converter register →														0	1	The TX and RX Counter A's are loaded with the TA + TA′ and RA + RA′ register values. The TX and RX Counter B's are loaded with the TB and RB register values. NOTE: d1 = 0, d0 = 1 will cause the next D/A and A/D conversion periods to be changed by the addition of TA′ and RA′ Master Clock cycles, in which TA′ and RA′ can be positive or negative or zero. Please refer to Table 1. AIC Responses to Improper Conditions.
← d15 (MSB) through d2 go to the D/A converter register →														1	0	The TX and RX Counter A's are loaded with the TA − TA′ and RA − RA′ register values. The TX and RX Counter B's are loaded with the TB and RB register values. NOTE: d1 = 1, d0 = 0 will cause the next D/A and A/D conversion periods to be changed by the subtraction of TA′ and RA′ Master Clock cycles, in which TA′ and RA′ can be positive or negative or zero. Please refer to Table 1. AIC Responses to Improper Conditions.
← d15 (MSB) through d2 go to the D/A converter register →														1	1	The TX and RX Counter A's are loaded with the TA and RA register converter register values. The TX and RX Counter B's are loaded with the TB and RB register values. After a delay of four Shift Clock cycles, a secondary transmission will immediately follow to program the AIC to operate in the desired configuration.

NOTE: Setting the two least significant bits to 1 in the normal transmission of DAC information (Primary Communications) to the AIC will initiate Secondary Communications upon completion of the Primary Communications.

Upon completion of the Primary Communication, $\overline{\text{FSX}}$ will remain high for four SHIFT CLOCK cycles and will then go low and initiate the Secondary Communication. The timing specifications for the Primary and Secondary Communications are identical. In this manner, the Secondary Communication, if initiated, is interleaved between successive Primary Communications. This interleaving prevents the Secondary Communication from interfering with the Primary Communications and DAC timing, thus preventing the AIC from skipping a DAC output. It is important to note that in the synchronous mode, $\overline{\text{FSR}}$ will not be asserted during Secondary Communications.

secondary DX serial communication protocol

x x | ← to TA register → | x x | ← to RA register → | 0 0	d13 and d6 are MSBs (unsigned binary)
x | ← to TA′ register → | x | ← to RA′ register → | 0 1	d14 and d7 are 2's complement sign bits
x | ← to TB register → | x | ← to RB register → | 1 0	d14 and d7 are MSBs (unsigned binary)
x x x x x x d9 x d7 d6 d5 d4 d3 d2 1 1 CONTROL REGISTER	d2 = 0/1 deletes/inserts the A/D high-pass filter d3 = 0/1 disables/enables the loopback function d4 = 0/1 disables/enables the AUX IN+ and AUX IN− pins d5 = 0/1 asynchronous/synchronous transmit and receive sections d6 = 0/1 gain control bits (see Gain Control Section) d7 = 0/1 gain control bits (see Gain Control Section) d9 = 0/1 delete/insert on-board second-order (sin x)/x correction filter

reset function

A reset function is provided to initiate serial communications between the AIC and DSP. The reset function will initialize all AIC registers, including the control register. After power has been applied to the AIC, a negative-going pulse on the $\overline{\text{RESET}}$ pin will initialize the AIC registers to provide an 8-kHz A/D and D/A conversion rate for a 5.184 MHz master clock input signal. The AIC, excepting the CONTROL register, will be initialized as follows (see AIC DX Data Word Format section):

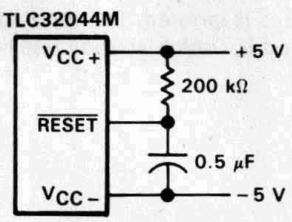
REGISTER	INITIALIZED REGISTER VALUE (HEX)
TA	9
TA′	1
TB	24
RA	9
RA′	1
RB	24

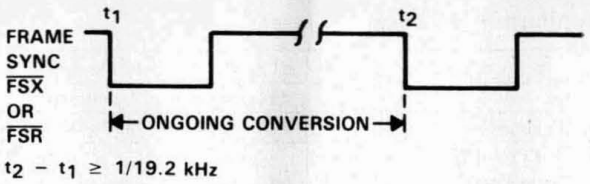
The CONTROL register bits will be reset as follows (see AIC DX Data Word Format section):

d9 = 1, d7 = 1, d6 = 1, d5 = 1, d4 = 0, d3 = 0, d2 = 1

This initialization allows normal serial port communications to occur between AIC and DSP. If the transmit and receive sections are configured to operate synchronously and the user wishes to program different conversion rates, only the TA, TA′, and TB register need to be programmed, since both transmit and receive timing are synchronously derived from these registers (see the Pin Descriptions and AIC DX Word Format sections).

The circuit shown below will provide a reset on power-up when power is applied in the sequence given under Power-Up Sequence. The circuit depends on the power supplies' reaching their recommended values a minimum of 800 ns before the capacitor charges to 0.8 V above DGTL GND.

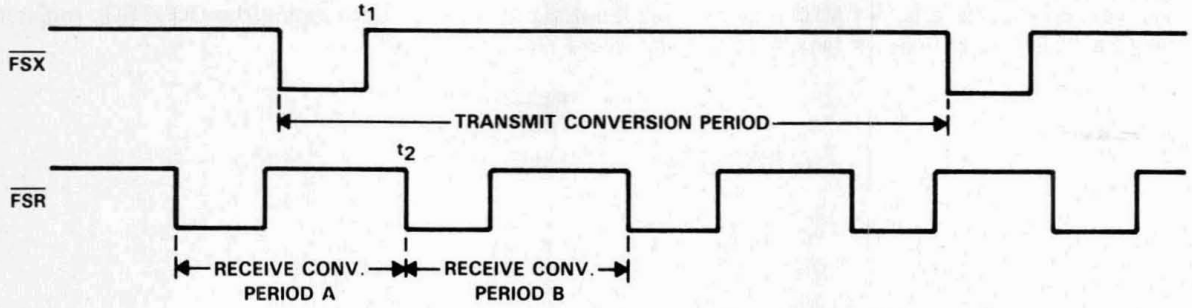




$t_2 - t_1 \geq 1/19.2$ kHz

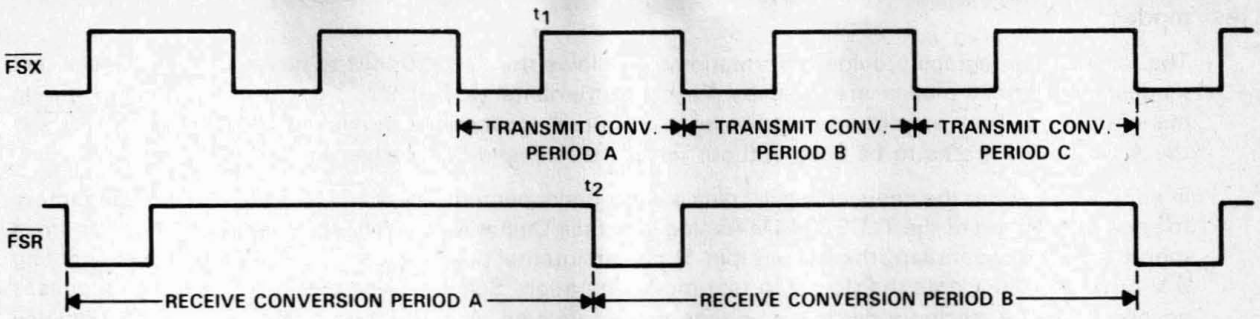
asynchronous operation — more than one receive frame sync occurring between two transmit frame syncs

When incrementally adjusting the conversion period via the A + A′ or A − A′ register options, a specific protocol is followed. The command to use the incremental conversion period adjust option is sent to the AIC during a $\overline{FSX}$ frame sync. The ongoing conversion period is then adjusted. However, either Receive Conversion Period A or B may be adjusted. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. Therefore, if there is sufficient time between t1 and t2, the receive conversion period adjustment will be performed during Receive Conversion Period A. Otherwise, the adjustment will be performed during Receive Conversion Period B. The adjustment command only adjusts one transmit conversion period and one receive conversion period. To adjust another pair of transmit and receive conversion periods, another command must be issued during a subsequent $\overline{FSX}$ frame (see figure below).



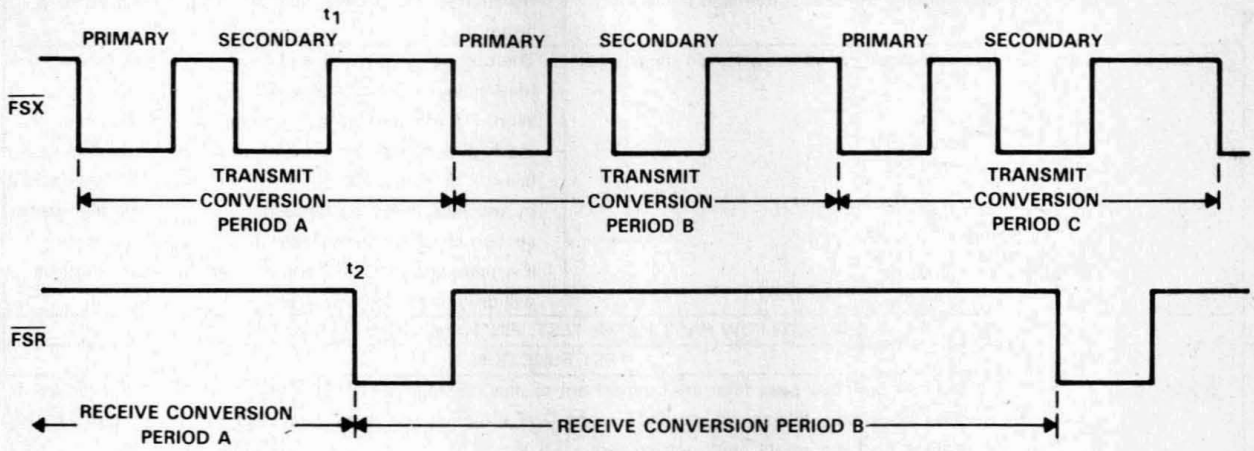
asynchronous operation — more than one transmit frame sync occurring between two receive frame syncs

When incrementally adjusting the conversion period via the A + A′ or A − A′ register options, a specific protocol is followed. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. The command to use the incremental conversion period adjust options is sent to the AIC during a $\overline{FSX}$ frame sync. The ongoing transmit conversion period is then adjusted. However, three possibilities exist for the receive conversion period adjustment in the diagram as shown in the following figure. If the adjustment command is issued during Transmit Conversion Period A, Receive Conversion Period A will be adjusted if there is sufficient time between t1 and t2. Or, if there is not sufficient time between t1 and t2, Receive Conversion Period B will be adjusted. Or, the receive portion of an adjustment command may be ignored if the adjustment command is sent during a receive conversion period, which is already being or will be adjusted due to a prior adjustment command. For example, if adjustment commands are issued during Transmit Conversion Periods A, B, and C, the first two commands may cause Receive Conversion Periods A and B to be adjusted, while the third receive adjustment command is ignored. The third adjustment command is ignored since it was issued during Receive Conversion Period B, which already will be adjusted via the Transmit Conversion Period B adjustment command.



asynchronous operation — more than one set of primary and secondary DX serial communication occurring between two receive frame sync (see AIC DX Data Word Format section)

The TA, TA′, TB, and control register information that is transmitted in the secondary communications is always accepted and is applied during the ongoing transmit conversion period. If there is sufficient time between t1 and t2, the TA, RA′, and RB register information, which is sent during Transmit Conversion Period A, will be applied to Receive Conversion Period A. Otherwise, this information will be applied during Receive Conversion Period B. If RA, RA′, and RB register information has already been received and is being applied during an ongoing conversion period, any subsequent RA, RA′, or RB information that is received during this receive conversion period will be disregarded (see diagram below).



test modes†

The following paragraph provides information that allows the TLC32044M to be operated in special test modes. These test modes are used by Texas Instruments to facilitate testing of the device during manufacturing. They are not intended to be used in real applications, however, they allow the filters in the A/D and D/A paths to be used without using the A/D and D/A converters.

In normal operation, the nonusable (NU) pins are left unconnected. These NU pins are used by the factory to speed up testing of the TLC32044M Analog Interface Circuit (AIC). When the device is used in normal (non-test-mode) operation, the NU pin (pin 1) has an internal pull-down to −5 V. Externally connecting 0 V or 5 V to pin 1 puts the device in test-mode operation. Selecting one of the possible test modes is accomplished by placing a particular voltage on certain pins. A description of these modes is provided in Table 2 and Figures 1 and 2.

TABLE 2. LIST OF TEST MODES

TEST PINS	D/A PATH TEST (PIN 1 to 5 V)	A/D PATH TEST (PIN 1 to 0)
	TEST FUNCTION	TEST FUNCTION
5	The low-pass switched-capacitor filter clock is brought out to pin 5. This clock signal is normally internal.	The bandpass switched-capacitor filter clock is brought out to pin 5. This clock signal is normally internal.
11	No change from normal operation. The $\overline{\text{EODX}}$ signal is brought out to pin 11.	The pulse that initiates the A/D conversion is brought out here. This signal is normally internal.
3	The pulse that initiates the D/A conversion is brought out here.	No change from normal operation. The EODR signal is brought out.
27 and 28	There are no test output signals provided on these pins.	The outputs of the A/D path low-pass or bandpass filter (depending upon control bit d2 — see AIC DX Data Word Format section) are brought out to these pins. If the high-pass section is inserted, the output will have a (sinx)/x droop. The slope of the droop will be determined by the ADC sampling frequency, which is the high-pass section clock frequency (see diagram of bandpass or low-pass filter test for receive section). These outputs will drive small (30-pF) loads.
	D/A PATH LOW-PASS FILTER TEST; PIN 13 (WORD/$\overline{\text{BYTE}}$) to −5 V	
	TEST FUNCTION	
15 and 16	The inputs of the D/A path low-pass filter are brought out to pins 15 and 16. The D/A input to this filter is removed. If the (sin x)/x correction filter is inserted, the OUT+ and OUT− signals will have a flat response (see Figure 2). The common-mode range of these inputs must not exceed ±0.5 V.	

† In the test mode, the AIC responds to the setting of Pin 13 to −5 V, as if Pin 13 were set to 0 V. Thus, the byte mode is selected for communicating between DSP and AIC. Either of the path tests (D/A or A/D) can be performed simultaneously with the D/A low-pass filter test. In this situation, Pin 13 must be connected to −5 V, which initiates byte-mode communications.

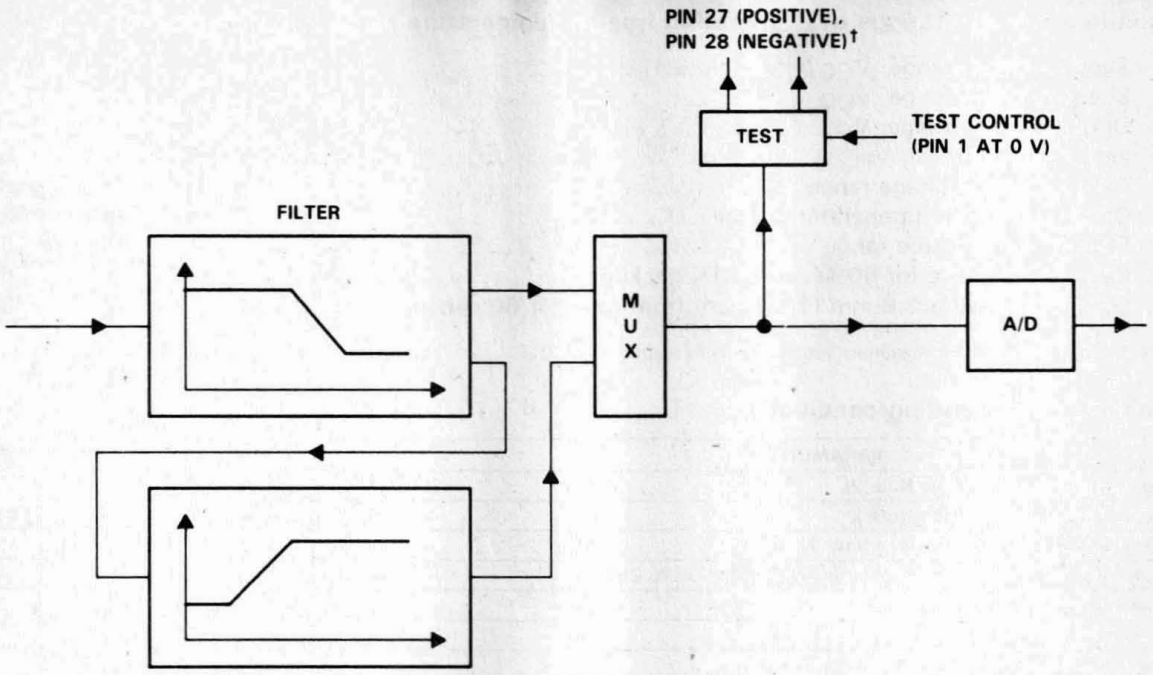


FIGURE 1. BANDPASS OR LOW-PASS FILTER TEST FOR RECEIVER SECTION

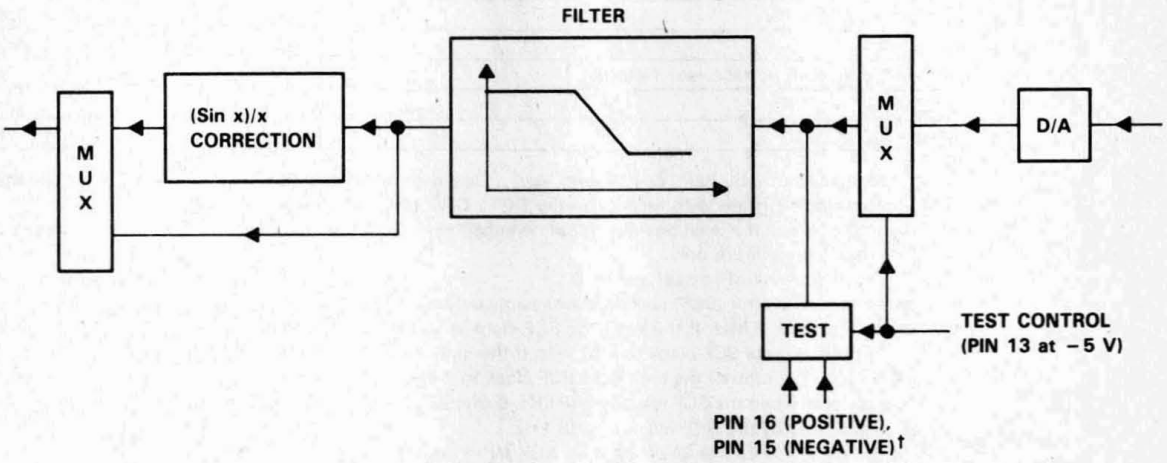


FIGURE 2. LOW-PASS FILTER TEST FOR TRANSMIT SECTION

†All analog signal paths have differential architecture and hence have positive and negative components.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC+} (see Note 1) . . . . . −0.3 V to 15 V
Supply voltage range, V_{DD} . . . . . −0.3 V to 15 V
Output voltage range, V_O . . . . . −0.3 V to 15 V
Input voltage range, V_I . . . . . −0.3 V to 15 V
Digital ground voltage range . . . . . −0.3 V to 15 V
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTE 1: Voltage values for maximum ratings are with respect to VCC−.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} (see Note 2)	4.75	5	5.25	V
Supply voltage, V_{CC-} (see Note 2)	−4.75	−5	−5.25	V
Digital supply voltage, V_{DD} (see Note 2)	4.75	5	5.25	V
Digital ground voltage with respect to ANLG GND, DGTL GND		0		V
Reference input voltage, $V_{ref(ext)}$ (see Note 2)	2		4	V
High-level input voltage, V_{IH}	2		V_{DD}+0.3	V
Low-level input voltage, V_{IL} (see Note 3)	−0.3		0.8	V
Maximum peak output voltage swing across R_L at OUT+ or OUT− (single-ended) (see Note 4)	±3			V
Load resistance at OUT+ and/or OUT−, R_L	300			Ω
Load capacitance at OUT+ and/or OUT−, C_L			100	pF
MSTR CLK frequency (see Note 5)	0.075	5	10.368	MHz
Analog input amplifier common mode input voltage (see Note 6)			±1.5	V
A/D or D/A conversion rate			20	kHz
Operating free-air temperature, T_A	−55		125	°C

NOTES: 2. Voltages at analog inputs and outputs, REF, V_{CC+}, and V_{CC-}, are with respect to the ANLG GND terminal. Voltages at digital inputs and outputs and V_{DD} are with respect to the DGTL GND terminal.
3. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels and temperature only.
4. This applies when $R_L \geq 300\ \Omega$ and offset voltage = 0.
5. The bandpass switched-capacitor filter (SCF) specifications apply only when the low-pass section SCF clock is 288 kHz and the high-pass section SCF clock is 8 kHz. If the low-pass SCF clock is shifted from 288 kHz, the low-pass roll-off frequency will shift by the ratio of the low-pass SCF clock to 288 kHz. If the high-pass SCF clock is shifted from 8 kHz, the high-pass roll-off frequency will shift by the ratio of the high-pass SCF clock to 8 kHz. Similarly, the low-pass switched-capacitor filter (SCF) specifications apply only when the SCF clock is 288 kHz. If the SCF clock is shifted from 288 kHz, the low-pass roll-off frequency will shift by the ratio of the SCF clock to 288 kHz.
6. This range applies when (IN+ − IN−) or (AUX IN+ − AUX IN−) equals ±6 V.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (unless otherwise noted)

total device, MSTR CLK frequency = 5.184 MHz, outputs not loaded

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{DD} = 4.75 V, I_{OH} = −300 μA	2.4			V
V_{OL}	Low-level output voltage	V_{DD} = 4.75 V, I_{OL} = 2 mA			0.4	V
I_{CC+}	Supply current from V_{CC+}				40	mA
I_{CC-}	Supply current from V_{CC-}				−40	mA
I_{DD}	Supply current from V_{DD}	$f_{MSTR\ CLK}$ = 5.184 MHz			8	mA
V_{ref}	Internal reference output voltage		2.9		3.3	V
αV_{ref}	Temperature coefficient of internal reference voltage			200		ppm/°C
r_o	Output resistance at REF			100		kΩ

receive amplifier input

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	A/D converter offset error (filters in)			10	85	mV
CMRR	Common-mode rejection ratio at IN+, IN−, or AUX IN+, AUX IN−	See Note 7	35	55		dB
r_i	Input resistance at IN+, IN− or AUX IN+, AUX IN−, REF			100		kΩ

transmit filter output

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OO}	Output offset voltage at OUT+ or OUT− (single-ended relative to ANLG GND)			15	85	mV
V_{OM}	Maximum peak output voltage swing between OUT+ and OUT− (differential output)	$R_L \geq 300\ \Omega$	±6			V

†All typical values are at T_A = 25°C.
NOTE 7: The test condition is a 0-dBm, 1-kHz input signal with an 8-kHz conversion rate.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (unless otherwise noted)

system distortion specifications, SCF clock frequency = 288 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Attenuation of second harmonic of A/D input signal	single-ended	V_{in} = −0.5 dB to −24 dB referred to V_{ref}, Single-ended tested at 25°C, See Note 8	62	70		dB
	differential		62	70		
Attenuation of third and higher harmonics of A/D input signal	single-ended	V_{in} = −0.5 dB to −24 dB referred to V_{ref}, Single-ended tested at 25°C, See Note 8	57	65		dB
	differential		57	65		
Attenuation of second harmonic of D/A input signal	single-ended	V_{in} = −0 dB to −24 dB referred to V_{ref}, See Note 8		70		dB
	differential		62	70		
Attenuation of third and higher harmonics of D/A input signal	single-ended	V_{in} = −0 dB to −24 dB referred to V_{ref}, See Note 8		65		dB
	differential		57	65		

A/D channel signal-to-distortion ratio

PARAMETER	TEST CONDITIONS (see Note 8)	A_v = 1‡		A_v = 2‡		A_v = 4‡		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
A/D channel signal-to-distortion ratio	V_{in} = −6 dB to −0.5 dB	58		>58§		>58§		dB
	V_{in} = −12 dB to −6 dB	58		58		>58§		
	V_{in} = −18 dB to −12 dB	56		58		58		
	V_{in} = −24 dB to −18 dB	50		56		58		
	V_{in} = −30 dB to −24 dB	44		50		56		
	V_{in} = −36 dB to −30 dB	38		44		50		
	V_{in} = −42 dB to −36 dB	32		38		44		
	V_{in} = −48 dB to −42 dB	26		32		38		
	V_{in} = −54 dB to −48 dB	20		26		32		

†All typical values are at T_A = 25°C.
‡A_v is the programmable gain of the input amplifier.
§A value >58 is over range and signal clipping occurs.

D/A channel signal-to-distortion ratio

PARAMETER	TEST CONDITIONS (see Note 8)	MIN	MAX	UNIT
D/A channel signal-to-distortion ratio	V_{in} = −6 dB to 0 dB	58		dB
	V_{in} = −12 dB to −6 dB	58		
	V_{in} = −18 dB to −12 dB	56		
	V_{in} = −24 dB to −18 dB	50		
	V_{in} = −30 dB to −24 dB	44		
	V_{in} = −36 dB to −30 dB	38		
	V_{in} = −42 dB to −36 dB	32		
	V_{in} = −48 dB to −42 dB	26		
	V_{in} = −54 dB to −48 dB	20		

NOTE 8: The test condition is a 1-kHz input signal with an 8-kHz conversion rate (0 dB relative to V_{ref}). The load impedance for the DAC is 300 Ω.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (unless otherwise noted) (continued)

gain and dynamic range

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Absolute transmit gain tracking error while transmitting into 300 Ω	−48 dB to 0 dB signal range, See Note 9		±0.05	±0.15	dB
Absolute receive gain tracking error	−48 dB to 0 dB signal range, See Note 9		±0.05	±0.15	dB
Absolute gain of the A/D channel	Signal input is a −0.5-dB, 1-kHz sinewave		0.2		dB
Absolute gain of the D/A channel	Signal input is a 0-dB, 1-kHz sinewave		−0.3		dB

power supply rejection and crosstalk attenuation

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{CC+} or V_{CC-} supply voltage rejection ratio, receive channel	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at DR (ADC output)		30		dB
	f = 30 kHz to 50 kHz			45		
V_{CC+} or V_{CC-} supply voltage rejection ratio, transmit channel (single-ended)	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at OUT+		30		dB
	f = 30 kHz to 50 kHz			45		
Crosstalk attenuation (differential)	Transmit-to-receive	DX = 00000000000000	65	80		dB
	Receive-to-transmit	Inputs grounded	65	80		

†All typical values are at T_A = 25°C.
NOTE 9: Gain tracking is relative to the absolute gain at 1 kHz and 0 dB (0 db relative to V_{ref}).

delay distortion

bandpass filter transfer function, SCF f_{clock} = 288 kHz IN+ − IN− is a ±3 V sinewave† (see Note 10)

PARAMETER	TEST CONDITION	FREQUENCEY RANGE	ADJUSTMENT ADDEND‡	MIN	TYP§	MAX	UNIT
Filter gain	Input signal reference to 0 dB	f ≤ 50 Hz	K1 × 0 dB	−33	−29	−25	dB
		f = 100 Hz	K1 × − 0.26 dB	−4	−2	−1	
		f = 150 Hz to 3100 Hz	K1 × 0 dB	−0.25	0	0.25	
		f = 3100 Hz to 3300 Hz	K1 × 0 dB	−0.3	0	0.3	
		f = 3300 Hz to 3600 Hz	K1 × 0 dB	−0.5	0	0.5	
		f = 3800 Hz	K1 × 2.3 dB	−3		−0.5	
		f = 4000 Hz	K1 × 2.7 dB	−20	−17	−16	
		f ≥ 4400 Hz	K1 × 3.2 dB			−40	
		f ≥ 5000 Hz	K1 × 0 dB			−65	

low-pass filter transfer function (see curves), SCF f_{clock} = 288 kHz (see Note 10)

PARAMETER	TEST CONDITION	FREQUENCY RANGE	ADJUSTMENT ADDEND‡	MIN	TYP§	MAX	UNIT
Filter gain	Input signal reference is 0 dB	f = 0 Hz to 3100 Hz	K1 × 0 dB	−0.25	0	0.25	dB
		f = 3100 Hz to 3300 Hz	K1 × 0 dB	−0.3	0	0.3	
		f = 3300 Hz to 3600 Hz	K1 × 0 dB	−0.5	0	0.5	
		f = 3800 Hz	K1 × 2.3 dB	−3		−0.5	
		f = 4000 Hz	K1 × 2.7 dB	−20	−17	−16	
		f ≥ 4400 Hz	K1 × 3.2 dB			−40	
		f ≥ 5000 Hz	K1 × 0 dB			−65	

serial port

PARAMETER		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −300 μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4	V
I_I	Input current				±10	μA
C_i	Input capacitance			15		pF
C_o	Output capacitance			15		pF

† See filter curves in typical characteristics.

‡ The MIN, TYP, and MAX specifications are given for a 288-kHz SCF clock frequency. A slight error in the 288-kHz SCF may result from inaccuracies in the MSTR CLK frequency, resulting from crystal frequency tolerances. If this frequency error is less than 0.25%, the ADJUSTMENT ADDEND should be added to the MIN, TYP, and MAX specifications, where K1 = 100 • [(SCF frequency − 288 kHz)/ 288 kHz]. For errors greater than 0.25%, see Note 10.

§ All typical values are at T_A = 25°C.

NOTE 10: The filter gain outside of the passband is measured with respect to the gain at 1 kHz. The filter gain within the passband is measured with respect to the average gain within the passband. The passbands are 150 to 3600 Hz and 0 to 3600 Hz for the bandpass and low-pass filters respectively. For switched-capacitor filter clocks at frequencies other than 288 kHz, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 288 kHz.

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V

noise (measurement includes low-pass and bandpass switched-capacitor filters)

PARAMETER		TEST CONDITIONS	TYP†	MAX	UNIT
Transmit noise	with (sin x)/x	DX input = 00000000000000, constant input code		575	μV rms
	without (sin x)/x		325	450	μV rms
			18		dBrnc0
Receive noise (see Note 11)		Inputs grounded, gain = 1	300	500	μV rms
			18		dBrnc0

timing requirements

serial port recommended input signals

PARAMETER		MIN	MAX	UNIT
$t_{c(MCLK)}$	Master clock cycle time	100	192	ns
$t_{r(MCLK)}$	Master clock rise time		10	ns
$t_{f(MCLK)}$	Master clock fall time		10	ns
	Master clock duty cycle	25%	75%	
	$\overline{RESET}$ pulse duration (see Note 12)	800		ns
$t_{su(DX)}$	DX setup time before SCLK↓	28		ns
$t_{h(DX)}$	DX hold time after SCLK↓	$t_{c(SCLK)}/4$		ns

NOTES: 11. The noise is computed by statistically evaluating the digital output of the A/D converter.
12. $\overline{RESET}$ pulse duration is the amount of time that the reset pin is held below 0.8 V after the power supplies have reached their recommended values.

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (continued)

serial port — AIC output signals

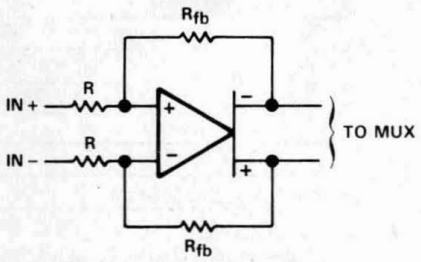
PARAMETER		MIN	TYP†	MAX	UNIT
$t_{c(SCLK)}$	Shift clock (SCLK) cycle time	400			ns
$t_{f(SCLK)}$	Shift clock (SCLK) fall time		50		ns
$t_{r(SCLK)}$	Shift clock (SCLK) rise time		50		ns
	Shift clock (SCLK) duty cycle		50		%
$t_{d(CH-FL)}$	Delay from SCLK↑ to $\overline{FSR}/\overline{FSX}$↓			260	ns
$t_{d(CH-FH)}$	Delay from SCLK↑ to $\overline{FSR}/\overline{FSX}$↑			260	ns
$t_{d(CH-DR)}$	DR valid after SCLK↑			316	ns
$t_{dw(CH-EL)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↓ in word mode			280	ns
$t_{dw(CH-EH)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↑ in word mode			280	ns
$t_{f(EODX)}$	$\overline{EODX}$ fall time		15		ns
$t_{f(EODR)}$	$\overline{EODR}$ fall time		15		ns
$t_{db(CH-EL)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↓ in byte mode		100		ns
$t_{db(CH-EH)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↑ in byte mode		100		ns
$t_{d(MH-SL)}$	Delay from MSTR CLK↑ to SCLK↓		65	105	ns
$t_{d(MH-SH)}$	Delay from MSTR CLK↑ to SCLK↑		65		ns

†All typical values are at T_A = 25°C.

**TABLE 3. GAIN CONTROL TABLE
(ANALOG INPUT SIGNAL REQUIRED FOR FULL-SCALE A/D CONVERSION)**

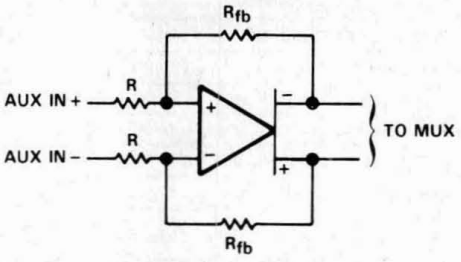
INPUT CONFIGURATIONS	CONTROL REGISTER BITS		ANALOG INPUT†	A/D CONVERSION RESULT
	d6	d7		
Differential configuration Analog input = IN+ − IN− = AUX IN+ − AUX IN−	1	1	±6 V	full-scale
	0	0		
	1	0	±3 V	full-scale
	0	1	±1.5 V	full-scale
Single-ended configuration Analog input = IN+ − ANLG GND = AUX IN+ − ANLG GND	1	1	±3 V	half-scale
	0	0		
	1	0	±3 V	full-scale
	0	1	±1.5 V	full-scale

†In this example, V_{ref} is assumed to be 3 V. In order to minimize distortion, it is recommended that the analog input not exceed 0.1 dB below full scale.



R_{fb} = R for d6 = 1, d7 = 1
d6 = 0, d7 = 0
R_{fb} = 2R for d6 = 1, d7 = 0
R_{fb} = 4R for d6 = 0, d7 = 1

FIGURE 3. IN+ AND IN− GAIN CONTROL CIRCUITRY



R_{fb} = R for d6 = 1, d7 = 1
d6 = 0, d7 = 0
R_{fb} = 2R for d6 = 1, d7 = 0
R_{fb} = 4R for d6 = 0, d7 = 1

FIGURE 4. AUX IN+ AND AUX IN− GAIN CONTROL CIRCUITRY

(sin x)/x correction section

If the designer does not wish to use the on-board second-order (sin x)/x correction filter, correction can be accomplished in digital signal processor (DSP) software. (Sin x)/x correction can be accomplished easily and efficiently in digital signal processor (DSP) software. Excellent correction accuracy can be achieved to a band edge of 3000 Hz by using a first-order digital correction filter. The results, which are shown below, are typical of the numerical correction accuracy that can be achieved for sample rates of interest. The filter requires only seven instruction cycles per sample on the SMJ320 DSPs. With a 200-ns instruction cycle, nine instructions per sample represents an overhead factor of 1.4% and 1.7% for sampling rates of 8000 Hz and 9600 Hz, respectively. This correction will add a slight amount of group delay at the upper edge of the 300−3000-Hz band.

(sin x)/x roll-off for a zero-order hold function

The (sin x)/x roll-off for the AIC DAC zero-order hold function at a band-edge frequency of 3000 Hz for the various sampling rates is shown in the table below.

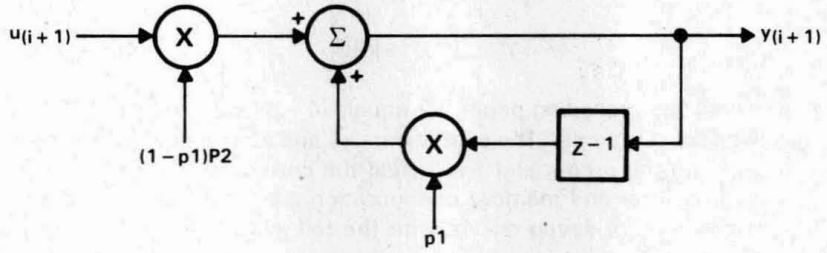
TABLE 4. (sin x)/x ROLL-OFF

f_s (Hz)	$20 \log \frac{\sin \pi f/f_s}{\pi f/f_s}$ (f = 3000 Hz) (dB)
7200	−2.64
8000	−2.11
9600	−1.44
14400	−0.63
19200	−0.35

Note that the actual AIC (sin x)/x roll-off will be slightly less than the above figures, because the AIC has less than a 100% duty cycle hold interval.

correction filter

To compensate for the (sin x)/x roll-off of the AIC, a first-order correction filter shown below, is recommended.



The difference equation for this correction filter is:

$$y_{i+1} = p2(1-p1)\,(u_{i+1}) + p1\,y_i$$

where the constant p1 determines the pole locations.

The resulting squared magnitude transfer function is:

$$|H(f)|^2 = \frac{p2^2\,(1-p1)^2}{1 - 2p1\cos(2\,\pi\,f/f_S) + p1^2}$$

correction results

Table 5 below shows the optimum p values and the corresponding correction results for 8000-Hz and 9600-Hz sampling rates.

TABLE 5

f (Hz)	ERROR (dB) f_S = 8000 Hz p1 = −0.14813 p2 = 0.9888	ERROR (dB) f_S = 9600 Hz p1 = −0.1307 p2 = 0.9951
300	−0.099	−0.043
600	−0.089	−0.043
900	−0.054	0
1200	−0.002	0
1500	0.041	0
1800	0.079	0.043
2100	0.100	0.043
2400	0.091	0.043
2700	−0.043	0
3000	−0.102	−0.043

SMJ320 software requirements

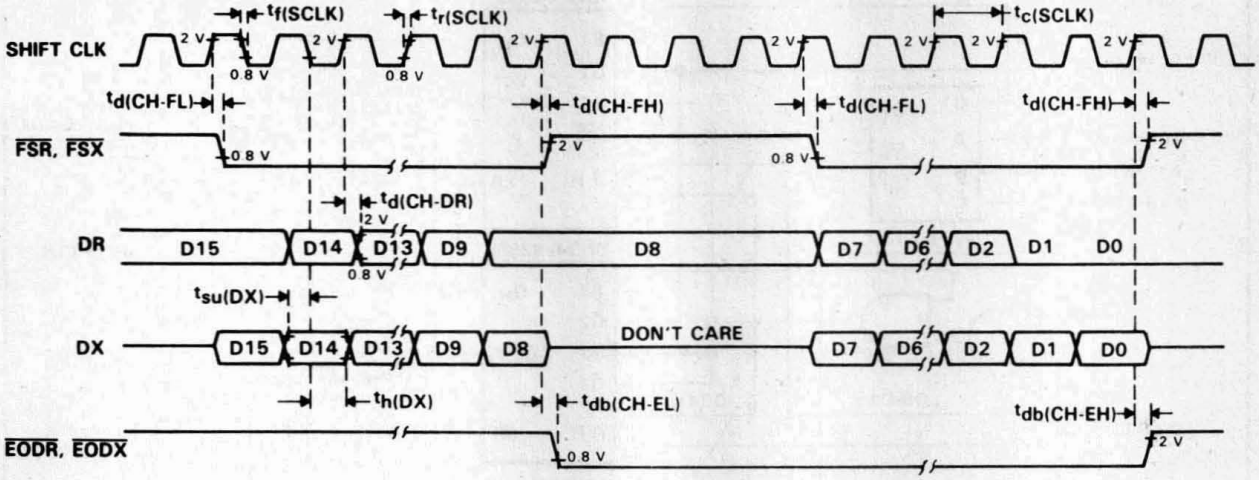
The digital correction filter equation can be written in state variable form as follows:

$$Y = k1Y + k2U$$

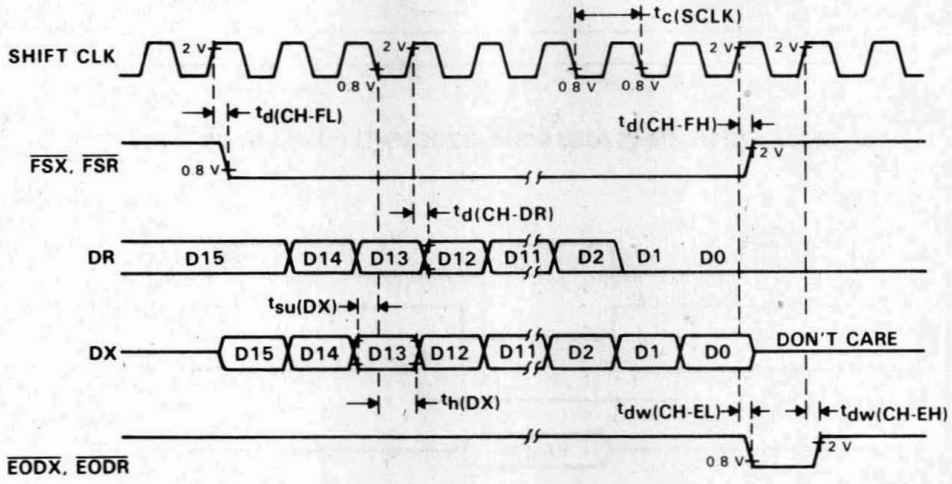
where k1 equals p1 (from the preceding page), k2 equals (1 − p1)p2 (from the preceding page), Y is the filter state, and U is the next I/O sample. The coefficients k1 and k2 must be represented as 16-bit integers. The SACH instruction (with the proper shift) will yield the correct result. With the assumption that the SMJ320 processor page pointer and memory configuration are properly initialized, the equation can be executed in seven instructions or seven cycles with the following program:

```
ZAC
LT K2
MPY U
LTA K1
MPY Y
APAC
SACH (dma), (shift)
```

byte-mode timing



word-mode timing



shift-clock timing

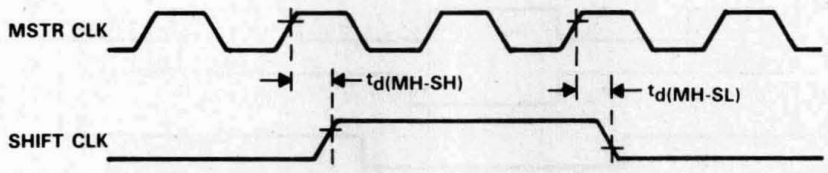


FIGURE 5. SERIAL PORT TIMING

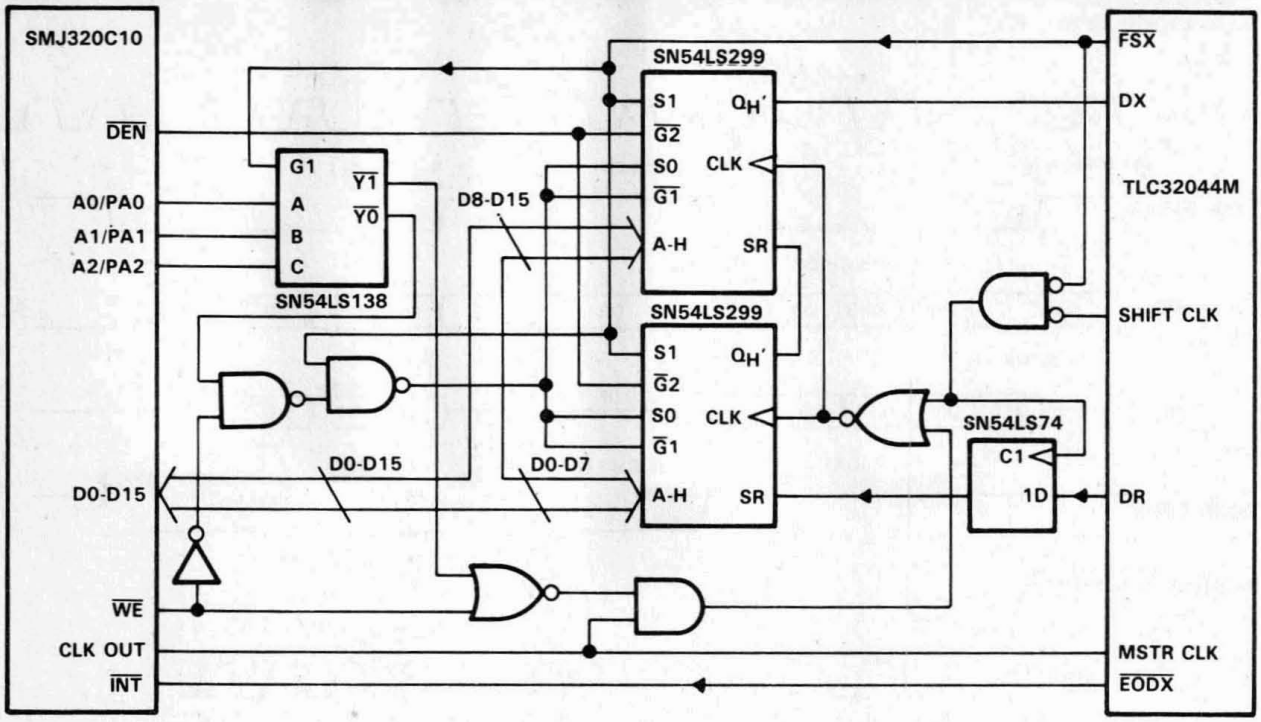
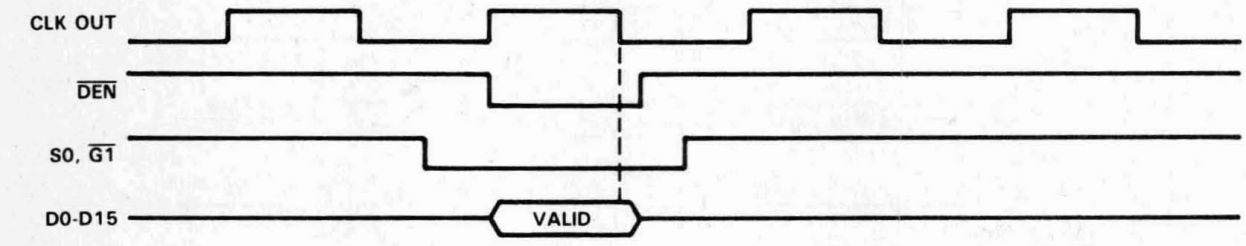


FIGURE 6. SMJ320C10/SMJ320C15/SMJ320E15-TLC32044M INTERFACE CIRCUIT

in instruction timing



out instruction timing

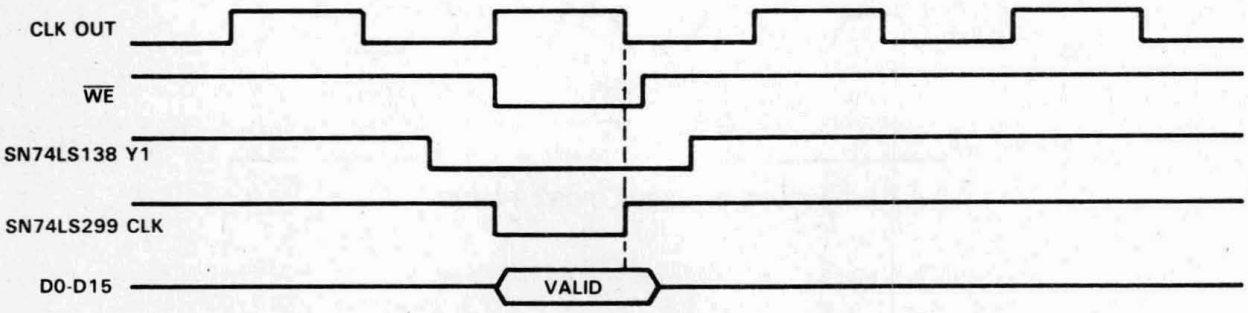


FIGURE 7. SMJ320C10/SMJ320C15/SMJ320E15-TLC32044M INTERFACE TIMING

TYPICAL CHARACTERISTICS

AIC TRANSMIT AND RECEIVE LOW-PASS FILTER

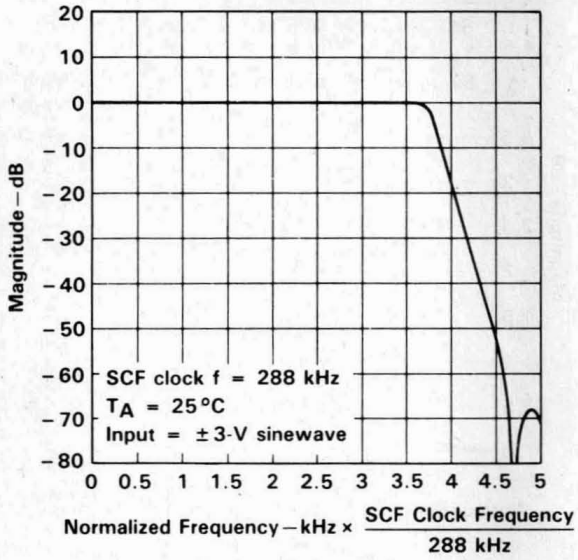


FIGURE 8

AIC TRANSMIT AND RECEIVE LOW-PASS FILTER

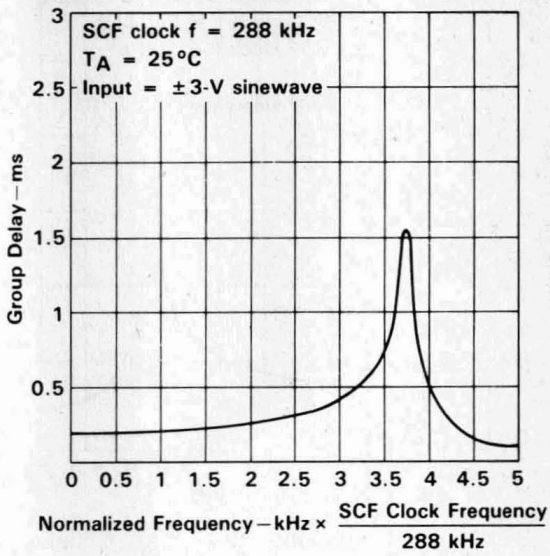


FIGURE 9

AIC RECEIVE-CHANNEL BANDPASS FILTER

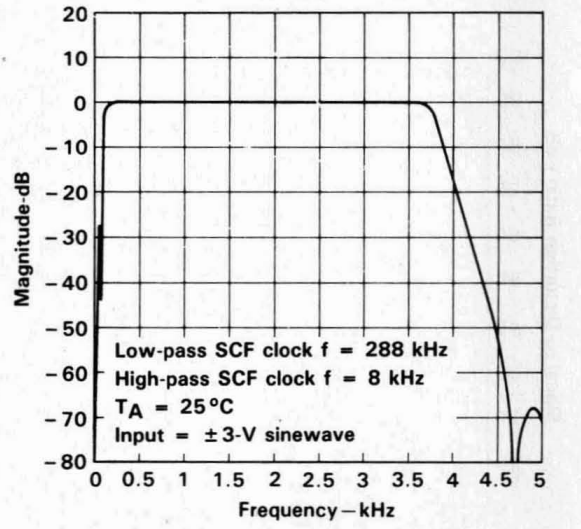


FIGURE 10

AIC RECEIVE-CHANNEL HIGH-PASS FILTER

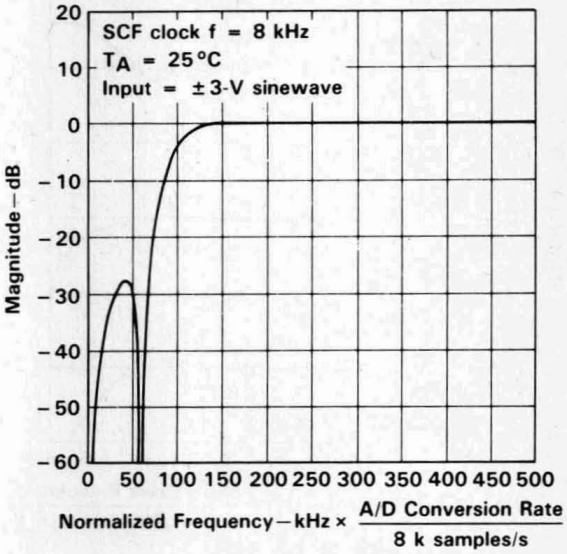


FIGURE 11

TYPICAL CHARACTERISTICS

AIC RECEIVE CHANNEL BANDPASS FILTER

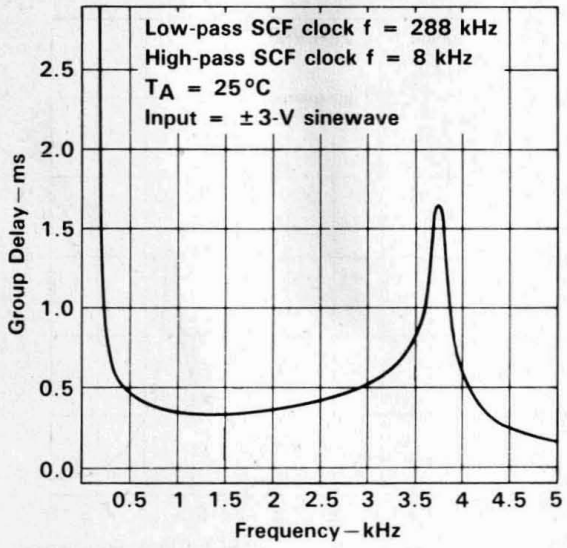


FIGURE 12

AIC (SIN X)/X CORRECTION FILTER

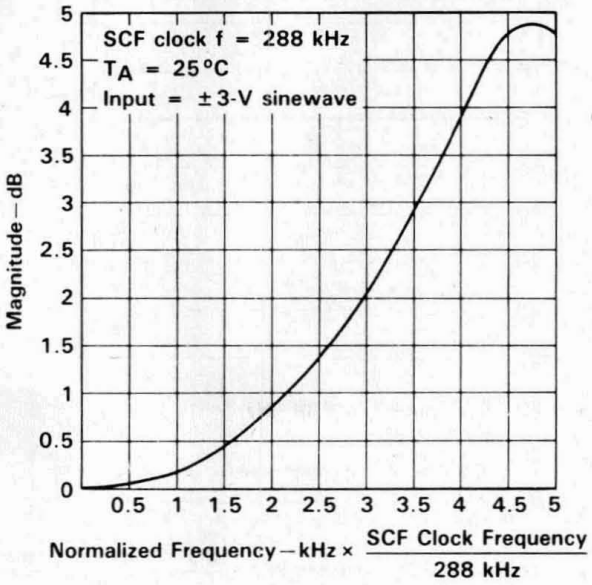


FIGURE 13

(SIN X)/X CORRECTION FILTER

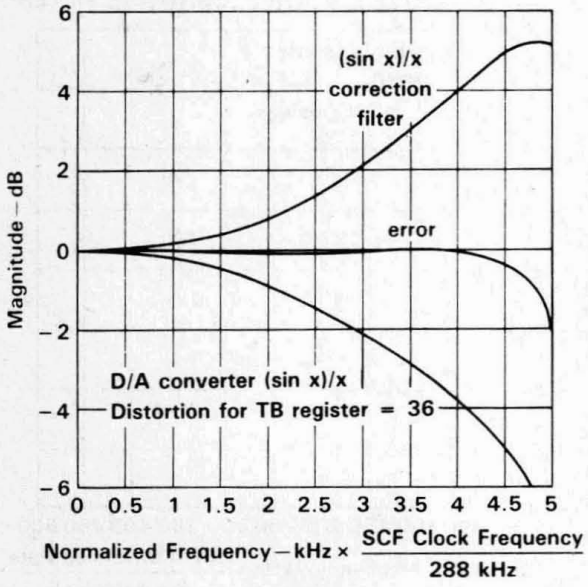


FIGURE 14

A/D SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL

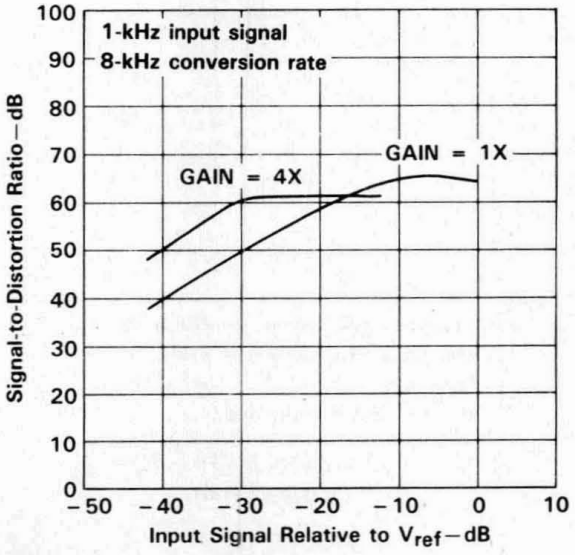


FIGURE 15

TYPICAL CHARACTERISTICS

A/D GAIN TRACKING
(GAIN RELATIVE TO GAIN AT 0 dB INPUT SIGNAL)

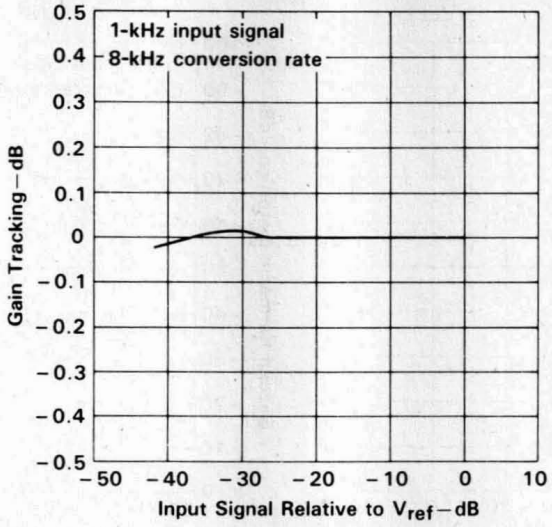


FIGURE 16

D/A CONVERTER SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL LEVEL

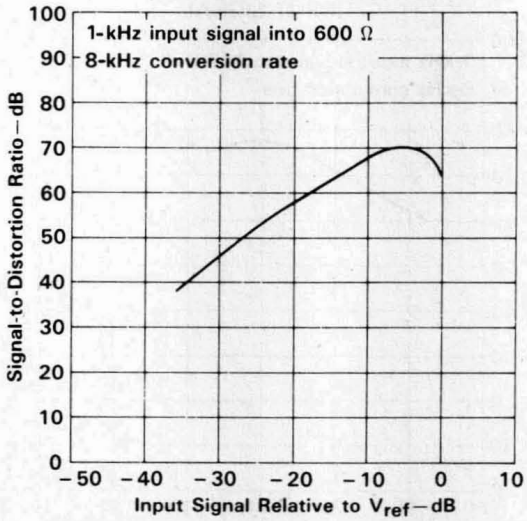


FIGURE 17

TYPICAL CHARACTERISTICS

D/A GAIN TRACKING
(GAIN RELATIVE TO GAIN
AT 0 dB INPUT SIGNAL LEVEL)

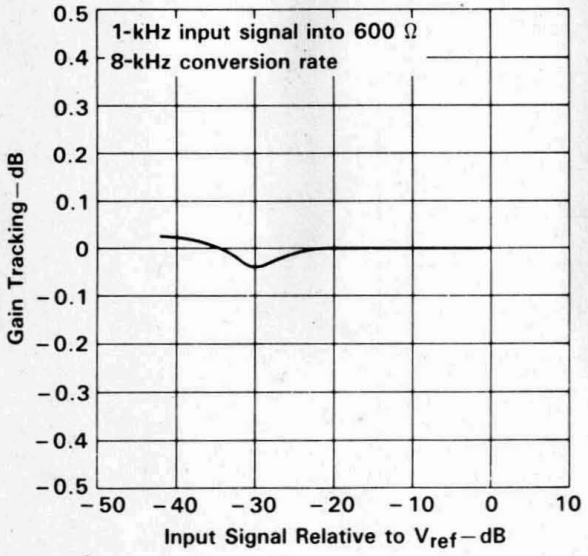


FIGURE 18

A/D SECOND HARMONIC DISTORTION
vs
INPUT SIGNAL

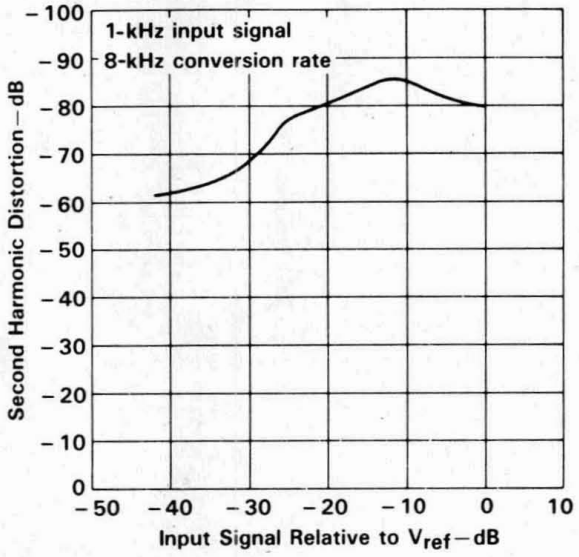


FIGURE 19

D/A SECOND HARMONIC DISTORTION
vs
INPUT SIGNAL

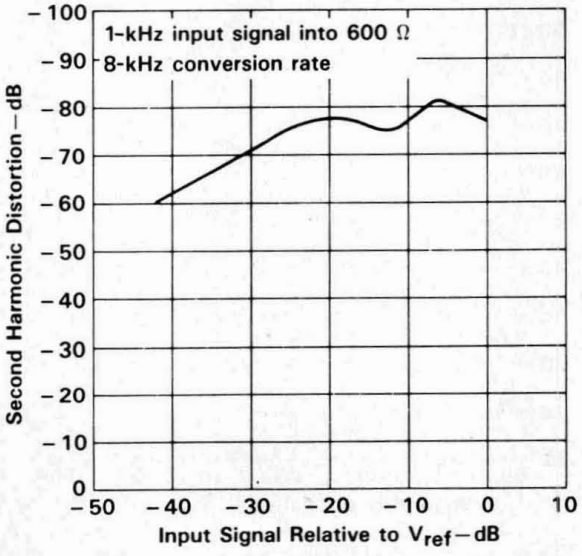


FIGURE 20

TYPICAL CHARACTERISTICS

A/D THIRD HARMONIC DISTORTION
vs
INPUT SIGNAL

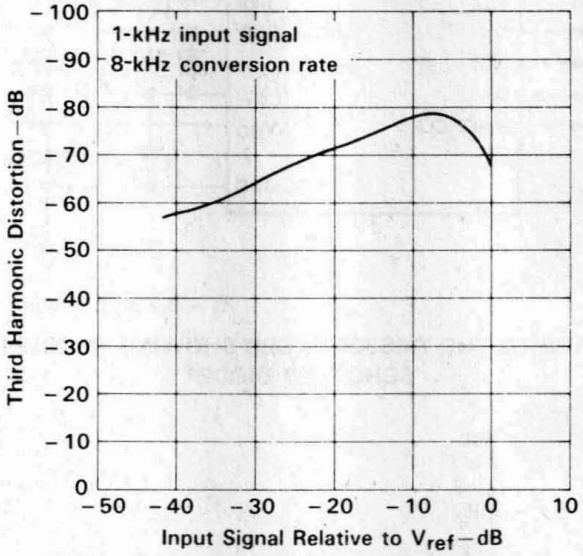


FIGURE 21

D/A THIRD HARMONIC DISTORTION
vs
INPUT SIGNAL

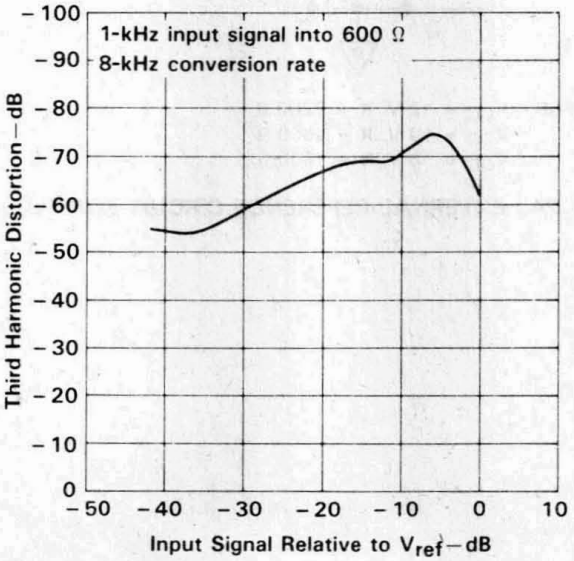
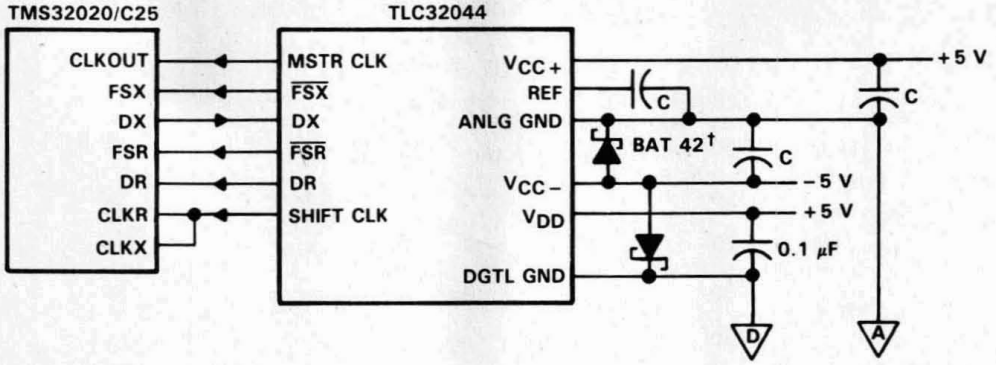


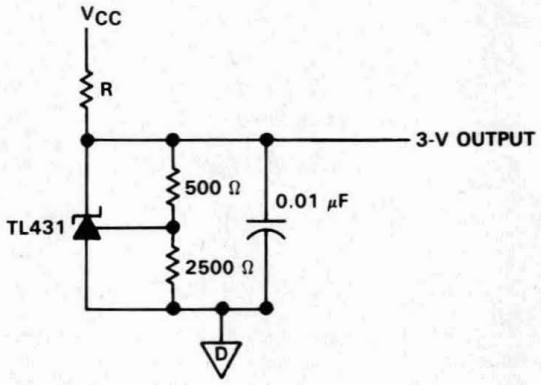
FIGURE 22

TYPICAL APPLICATION INFORMATION



C = 0.2 μF, CERAMIC

FIGURE 23. AIC INTERFACE TO THE TMS32020/C25 SHOWING DECOUPLING CAPACITORS AND SCHOTTKY DIODE†



FOR: V_{CC} = 12 V, R = 7200 Ω
V_{CC} = 10 V, R = 5600 Ω
V_{CC} = 5 V, R = 1600 Ω

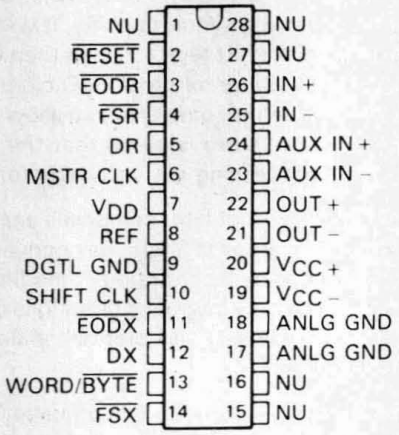
FIGURE 24. EXTERNAL REFERENCE CIRCUIT FOR TLC32044

†Thomson Semiconductors

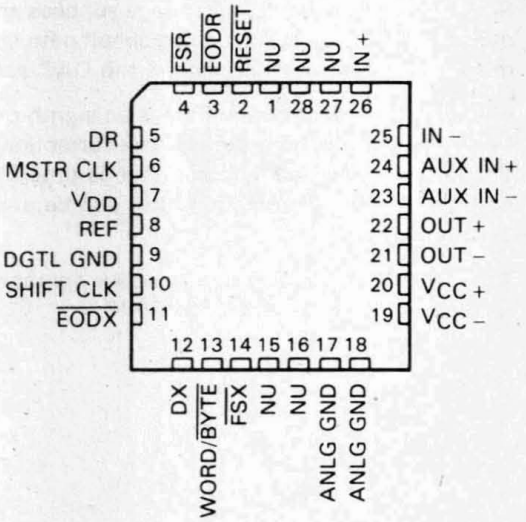
D3188, DECEMBER 1988—REVISED MAY 1991

- **Advanced LinCMOS™ Silicon-Gate Process Technology**
- **14-Bit Dynamic Range ADC and DAC**
- **16-Bit Dynamic Range Input with Programmable Gain**
- **Variable ADC and DAC Sampling Rate Up to 19,200 Samples per Second**
- **Switched-Capacitor Antialiasing Input Filter and Output-Reconstruction Filter**
- **Serial Port for Direct Interface to TMS320C17, TMS32020, TMS320C25, and TMS320C30 Digital Processors**
- **Synchronous or Asynchronous ADC and DAC Conversion Rates with Programmable Incremental ADC and DAC Conversion Timing Adjustments**
- **Serial Port Interface to SN74299 Serial-to-Parallel Shift Register for Parallel Interface to TMS32010, TMS320C15, or Other Digital Processors**
- **Internal Reference for Normal Operation and External Purposes, or Can Be Overridden by External Reference**
- **600-mil Wide N package (C_L to C_L)**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NU—Nonusable; no external connection should be made to these pins. See Table 2.

description

The TLC32045 is a complete analog-to-digital and digital-to-analog input/output system on a single monolithic CMOS chip. This device integrates a bandpass switched-capacitor antialiasing input filter, a 14-bit-resolution A/D converter, four microprocessor-compatible serial port modes, a 14-bit-resolution D/A converter, and a low-pass switched-capacitor output-reconstruction filter. The device offers numerous combinations of Master Clock input frequencies and conversion/sampling rates, which can be changed via digital processor control.

Typical applications for this IC include speech encryption for digital transmission, speech recognition/storage systems, speech synthesis, modems (7.2-, 8-, 9.6-, 14.4-, and 19.2-kHz sampling rate), analog interface for digital signal processors (DSPs), industrial process control, biomedical instrumentation, acoustical signal processing, spectral analysis, data acquisition, and instrumentation recorders. Four serial modes, which allow direct interface to the TMS320C17, TMS32020, TMS320C25, and TMS320C30 digital signal

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description (continued)

processors, are provided. Also, when the transmit and receive sections of the Analog Interface Circuit (AIC) are operating synchronously, it will interface to two SN74299 serial-to-parallel shift registers. These serial-to-parallel shift registers can then interface in parallel to the TMS32010, TMS320C15, other digital signal processors, or external FIFO circuitry. Output data pulses are emitted to inform the processor that data transmission is complete or to allow the DSP to differentiate between two transmitted bytes. A flexible control scheme is provided so that the functions of the IC can be selected and adjusted coincidentally with signal processing via software control.

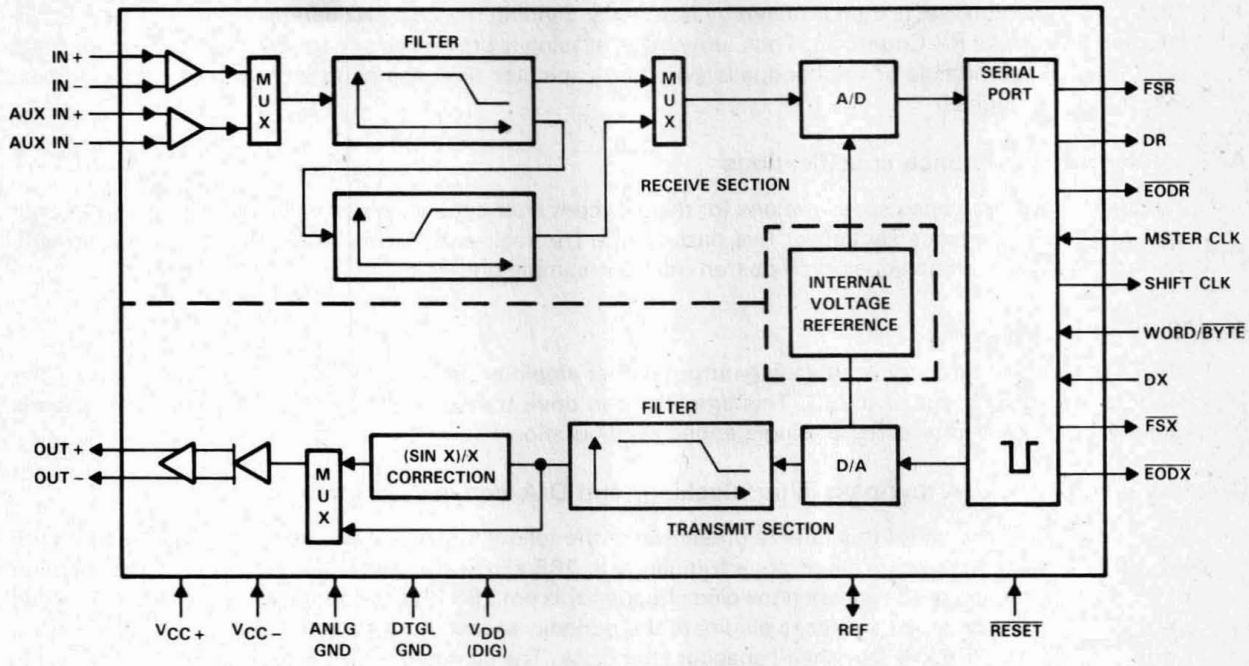
The antialiasing input filter comprises eighth-order and fourth-order CC-type (Chebyshev/elliptic transitional) low-pass and high-pass filters, respectively. The input filter is implemented in switched-capacitor technology and is preceded by a continuous time filter to eliminate any possibility of aliasing caused by sampled data filtering. When only low-pass filtering is desired, the high-pass filter can be switched out of the signal path. A selectable, auxiliary, differential analog input is provided for applications where more than one analog input is required.

The A/D and D/A converters each have 14 bits of resolution with 9 bits of integral linearity specified over any 9-bit range. The A/D and D/A architectures ensure no missing codes and monotonic operation. An internal voltage reference is provided to ease the design task and to provide complete control over the performance of the IC. The internal voltage reference is brought out to a pin and is available to the designer. Separate analog and digital voltage supplies and grounds are provided to minimize noise and ensure a wide dynamic range. Also, the analog circuit path contains only differential circuitry to keep noise to an absolute minimum. The only exception is the DAC sample-and-hold, which utilizes pseudo-differential circuitry.

The output-reconstruction filter is an eighth-order CC-type (Chebyshev/elliptic transitional low-pass filter) followed by a second-order (sin x)/x correction filter) and is implemented in switched-capacitor technology. This filter is followed by a continuous-time filter to eliminate images of the digitally encoded signal. The on-board (sin x)/x correction filter can be switched out of the signal path using digital signal processor control, if desired.

The TLC32045C is characterized for operation from 0°C to 70°C and the TLC32045I is characterized for operation from −40°C to 85°C.

functional block diagram



PRINCIPLES OF OPERATION

analog input

Two sets of analog inputs are provided. Normally, the IN+ and IN− input set is used; however, the auxiliary input set, AUX IN+ and AUX IN−, can be used if a second input is required. Each input set can be operated in either differential or single-ended modes, since sufficient common-mode range and rejection are provided. The gain for the IN+, IN−, AUX IN+, and AUX IN− inputs can be programmed to be either 1, 2, or 4 (see Table 2). Either input circuit can be selected via software control. It is important to note that a wide dynamic range is assured by the differential internal analog architecture and by the separate analog and digital voltage supplies and grounds.

A/D bandpass filter, A/D bandpass filter clocking, and A/D conversion timing

The A/D high-pass filter can be selected or bypassed via software control. The frequency response of this filter is presented in the following pages. This response results when the switched-capacitor filter clock frequency is 288 kHz and the A/D sample rate is 8 kHz. Several possible options can be used to attain a 288-kHz switched-capacitor filter clock. When the filter clock frequency is not 288 kHz, the low-pass filter transfer function is frequency-scaled by the ratio of the actual clock frequency to 288 kHz. The ripple bandwidth and 3-dB low-frequency roll-off points of the high-pass section are 150 and 100 Hz, respectively. However, the high-pass section low-frequency roll-off is frequency-scaled by the ratio of the A/D sample rate to 8 kHz.

The Internal Timing Configuration and AIC DX Data Word Format sections of this data sheet indicate the many options for attaining a 288-kHz bandpass switched-capacitor filter clock. These sections indicate that the RX Counter A can be programmed to give a 288-kHz bandpass switched-capacitor filter clock for several Master Clock input frequencies.

PRINCIPLES OF OPERATION (continued)

The A/D conversion rate is then attained by frequency-dividing the 288-kHz bandpass switched-capacitor filter clock with the RX Counter B. Thus, unwanted aliasing is prevented because the A/D conversion rate is an integral submultiple of the bandpass switched-capacitor filter sampling rate, and the two rates are synchronously locked.

A/D converter performance specifications

Fundamental performance specifications for the A/D converter circuitry are presented in the A/D converter operating characteristics section of this data sheet. The realization of the A/D converter circuitry with switched-capacitor techniques provides an inherent sample-and-hold.

analog output

The analog output circuitry is an analog output power amplifier. Both noninverting and inverting amplifier outputs are brought out of the IC. This amplifier can drive transformer hybrids or low-impedance loads directly in either a differential or single-ended configuration.

D/A low-pass filter, D/A low-pass filter clocking, and D/A conversion timing

The frequency response of this filter is presented in the following pages. This response results when the low-pass switched-capacitor filter clock frequency is 288 kHz. Like the A/D filter, the transfer function of this filter is frequency-scaled when the clock frequency is not 288 kHz. A continuous-time filter is provided on the output of the (sin x)/x filter to eliminate the periodic sample data signal information, which occurs at multiples of the 288-kHz switched-capacitor filter clock. The continuous time filter also greatly attenuates any switched-capacitor clock feedthrough.

The D/A conversion rate is attained by frequency-dividing the 288-kHz switched-capacitor filter clock with TX Counter B. Thus, unwanted aliasing is prevented because the D/A conversion rate is an integral submultiple of the switched-capacitor low-pass filter sampling rate, and the two rates are synchronously locked.

asynchronous versus synchronous operation

If the transmit section of the AIC (low-pass filter and DAC) and receive section (bandpass filter and ADC) are operated asynchronously, the low-pass and bandpass filter clocks are independently generated from the Master Clock signal. Also, the D/A and A/D conversion rates are independently determined. If the transmit and receive sections are operated synchronously, the low-pass filter clock drives both low-pass and bandpass filters. In synchronous operation, the A/D conversion timing is derived from, and is equal to, the D/A conversion timing. (See description of the WORD/$\overline{\text{BYTE}}$ pin in the Pin Functional Description Section.)

D/A converter performance specifications

Fundamental performance specifications for the D/A converter circuitry are presented in the D/A converter operating characteristics section of the data sheet. The D/A converter has a sample-and-hold that is realized with a switched-capacitor ladder.

system frequency response correction

(Sin x)/x correction for the D/A converter's zero-order sample-and-hold output can be provided by an on-board second-order (sin x)/x correction filter. This (sin x)/x correction filter can be inserted into or deleted from the signal path by digital signal processor control. When inserted, the (sin x)/x correction filter follows the switched-capacitor low-pass filter. When the TB register (see Internal Timing Configuration section) equals 36, the correction results of Figures 11 and 12 will be obtained.

PRINCIPLES OF OPERATION (continued)

(Sin x)/x correction can also be accomplished by deleting the on-board second-order correction filter and performing the (sin x)/x correction in digital signal processor software. The system frequency response can be corrected via DSP software to ±0.1 dB accuracy to a band-edge of 3000 Hz for all sampling rates. This correction is accomplished with a first-order digital correction filter, which requires only seven TMS320 instruction cycles. With a 200-ns instruction cycle, seven instructions represent an overhead factor of only 1.1% and 1.3% for sampling rates of 8 and 9.6 kHz, respectively (see the (sin x)/x Correction Section for more details).

serial port

The serial port has four possible modes that are described in detail in the Functional Pin Description Section. These modes are briefly described below and in the Functional Description for Pin 13, WORD/$\overline{\text{BYTE}}$.

1. The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS320C17.
2. The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS32020, TMS320C25, and the TMS320C30.
3. The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS320C17.
4. The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS32020, TMS320C25, TMS320C30, or two SN74299 serial-to-parallel shift registers, which can then interface in parallel to the TMS32010, TMS320C15, to any other digital signal processor, or to external FIFO circuitry.

operation of TLC32045 with internal voltage reference

The internal reference of the TLC32045 eliminates the need for an external voltage reference and provides overall circuit cost reduction. Thus, the internal reference eases the design task and provides complete control over the performance of the IC. The internal reference is brought out to a pin and is available to the designer. To keep the amount of noise on the reference signal to a minimum, an external capacitor may be connected between REF and ANLG GND.

operation of TLC32045 with external voltage reference

The REF pin may be driven from an external reference circuit if so desired. This external circuit must be capable of supplying 250 μA and must be adequately protected from noise such as crosstalk from the analog input.

reset

A reset function is provided to initiate serial communications between the AIC and DSP and to allow fast, cost-effective testing during manufacturing. The reset function will initialize all AIC registers, including the control register. After a negative-going pulse on the $\overline{\text{RESET}}$ pin, the AIC will be initialized. This initialization allows normal serial port communications activity to occur between AIC and DSP (see AIC DX Data Word Format section).

PRINCIPLES OF OPERATION (continued)

loopback

This feature allows the user to test the circuit remotely. In loopback, the OUT + and OUT − pins are internally connected to the IN + and IN − pins. Thus, the DAC bits (d15 to d2), which are transmitted to the DX pin, can be compared with the ADC bits (d15 to d2), which are received from the DR pin. An ideal comparison would be that the bits on the DR pin equal the bits on the DX pin. However, in practice there will be some difference in these bits due to the ADC and DAC output offsets.

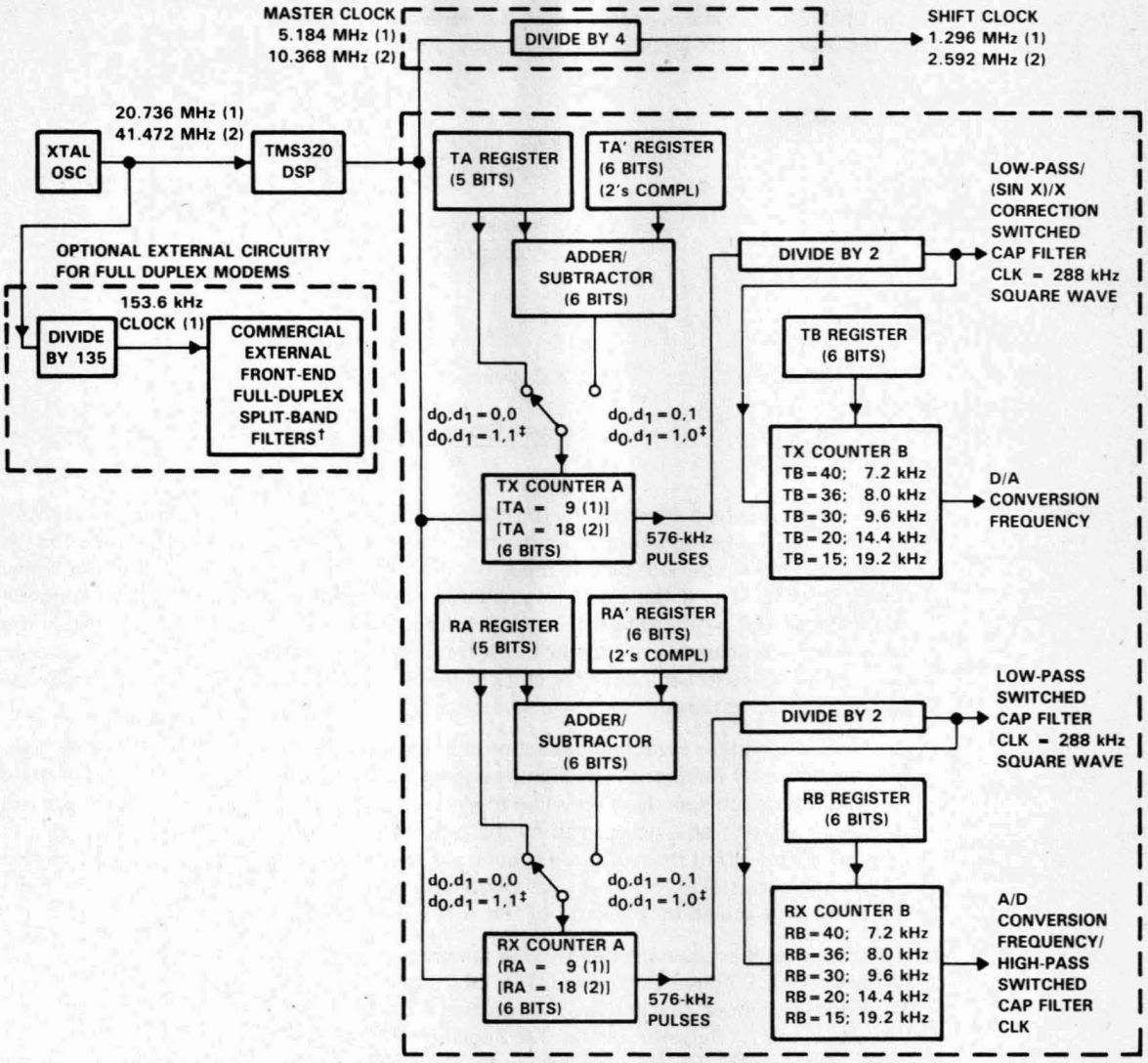
The loopback feature is implemented with digital signal processor control by transmitting the appropriate serial port bit to the control register (see AIC Data Word Format section).

PIN NAME	PIN NO.	I/O	DESCRIPTION
ANLG GND	17,18		Analog ground return for all internal analog circuits. Not internally connected to DGTL GND.
AUX IN+	24	I	Noninverting auxiliary analog input stage. This input can be switched into the bandpass filter and A/D converter path via software control. If the appropriate bit in the Control register is a 1, the auxiliary inputs will replace the IN + and IN − inputs. If the bit is a 0, the IN + and IN − inputs will be used (see the AIC DX Data Word Format section).
AUX IN−	23	I	Inverting auxiliary analog input (see the above AUX IN + pin description).
DGTL GND	9		Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
DR	5	O	This pin is used to transmit the ADC output bits from the AIC to the TMS320 serial port. This transmission of bits from the AIC to the TMS320 serial port is synchronized with the SHIFT CLK signal.
DX	12	I	This pin is used to receive the DAC input bits and timing and control information from the TMS320. This serial transmission from the TMS320 serial port to the AIC is synchronized with the SHIFT CLK signal.
$\overline{\text{EODR}}$	3	O	End of Data Receive. See the WORD/BYTE pin description and Figure 5. During the word-mode timing, this signal is a low-going pulse that occurs immediately after the 16 bits of A/D information have been transmitted from the AIC to the TMS320 serial port. This signal can be used to interrupt a microprocessor upon completion of serial communications. Also, this signal can be used to strobe and enable external serial-to-parallel shift registers, latches, or external FIFO RAM, and to facilitate parallel data bus communications between the AIC and the serial-to-parallel shift registers. During the byte-mode timing, this signal goes low after the first byte has been transmitted from the AIC to the TMS320 serial port and is kept low until the second byte has been transmitted. The TMS320C17 can use this low-going signal to differentiate between the two bytes as to which is first and which is second. $\overline{\text{EODR}}$ does not occur after secondary communication.

PIN NAME	PIN NO.	I/O	DESCRIPTION
$\overline{EODX}$	11	O	End of Data Transmit. See the WORD/$\overline{BYTE}$ pin description and Figure 5. During the word-mode timing, this signal is a low-going pulse that occurs immediately after the 16 bits of D/A converter and control or register information have been transmitted from the TMS320 serial port to the AIC. This signal can be used to interrupt a microprocessor upon the completion of serial communications. Also, this signal can be used to strobe and enable external serial-to-parallel shift registers, latches, or an external FIFO RAM, and to facilitate parallel data-bus communications between the AIC and the serial-to-parallel shift registers. During the byte-mode timing, this signal goes low after the first byte has been transmitted from the TMS320 serial port to the AIC and is kept low until the second byte has been transmitted. The TMS320C17 can use this low-going signal to differentiate between the two bytes as to which is first and which is second.
$\overline{FSR}$	4	O	Frame Sync Receive. In the serial transmission modes, which are described in the WORD/$\overline{BYTE}$ pin description, the $\overline{FSR}$ pin is held low during bit transmission. When the $\overline{FSR}$ pin goes low, the TMS320 serial port will begin receiving bits from the AIC via the DR pin of the AIC. The most significant DR bit will be present on the DR pin before $\overline{FSR}$ goes low. See Internal Timing Configuration diagram and Figure 5. $\overline{FSR}$ does not occur after secondary communication.
$\overline{FSX}$	14	O	Frame Sync Transmit. When this pin goes low, the TMS320 serial port will begin transmitting bits to the AIC via the DX pin of the AIC. In all serial transmission modes, which are described in the WORD/$\overline{BYTE}$ pin description, the $\overline{FSX}$ pin is held low during bit transmission. See Internal Timing Configuration diagram and Figure 5.
IN+	26	I	Noninverting input to analog input amplifier stage
IN−	25	I	Inverting input to analog input amplifier stage
MSTR CLK	6	I	The Master Clock signal is used to derive all the key logic signals of the AIC, such as the Shift Clock, the switched-capacitor filter clocks, and the A/D and D/A timing signals. The Internal Timing Configuration diagram shows how these key signals are derived. The frequencies of these key signals are synchronous submultiples of the Master Clock frequency to eliminate unwanted aliasing when the sampled analog signals are transferred between the switched-capacitor filters and the A/D and D/A converters. See Internal Timing Configuration diagram.
OUT+	22	O	Noninverting output of analog output power amplifier. Can drive transformer hybrids or high-impedance loads directly in either a differential or a single-ended configuration.
OUT−	21	O	Inverting output of analog output power amplifier. Functionally identical with and complementary to OUT+.
REF	8	I/O	The internal voltage reference is brought out on this pin. An external voltage reference can also be applied to this pin.
$\overline{RESET}$	2	I	A reset function is provided to initialize the TA, TA′, TB, RA, RA′, RB, and control registers. This reset function initiates serial communications between the AIC and DSP. The reset function will initialize all AIC registers including the control register. After a negative-going pulse on the $\overline{RESET}$ pin, the AIC registers will be initialized to provide an 8-kHz data conversion rate for a 5.184-MHz master clock input signal. The conversion rate adjust registers, TA′ and RA′, will be reset to 1. The CONTROL register bits will be reset as follows (see AIC DX Data Word Format section). d9 = 1, d7 = 1, d6 = 1, d5 = 1, d4 = 0, d3 = 0, d2 = 1 This initialization allows normal serial-port communication to occur between AIC and DSP.
SHIFT CLK	10	O	The Shift Clock signal is obtained by dividing the Master Clock signal frequency by four. This signal is used to clock the serial data transfers of the AIC, described in the WORD/$\overline{BYTE}$ pin description. See Internal Timing Configuration diagram and Figure 5.
V_{DD}	7		Digital supply voltage, 5 V ±5%
V_{CC+}	20		Positive analog supply voltage, 5 V ±5%
V_{CC-}	19		Negative analog supply voltage −5 V ±5%

PIN NAME	NO.	I/O	DESCRIPTION
WORD/$\overline{\text{BYTE}}$	13	I	This pin, in conjunction with a bit in the CONTROL register, is used to establish one of four serial modes. These four serial modes are described below. *AIC transmit and receive sections are operated asynchronously.* The following description applies when the AIC is configured to have asynchronous transmit and receive sections. If the appropriate data bit in the Control register is a 0 (see the AIC DX Data Word Format), the transmit and receive sections will be asynchronous. L Serial port directly interfaces with the serial port of the TMS320C17 and communicates in two 8-bit bytes. The operation sequence is as follows (see Figure 5). 1. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought low. 2. One 8-bit byte is transmitted or one 8-bit byte is received. 3. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pin is brought low. 4. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin emits a positive frame-sync pulse that is four Shift Clock cycles wide. 5. One 8-bit byte is transmitted or one 8-bit byte is received. 6. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pin is brought high. 7. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought high. H Serial port directly interfaces with the serial ports of the TMS32020, TMS320C25, and TMS320C30, and communicates in one 16-bit word. The operation sequence is as follows (see Figure 5): 1. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought low. 2. One 16-bit word is transmitted or one 16-bit word is received. 3. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought high. 4. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pin emits a low-going pulse. *AIC transmit and receive sections are operated synchronously.* If the appropriate data bit in the Control register is a 1, the transmit and receive sections will be configured to be synchronous. In this case, the bandpass switched-capacitor filter and the A/D conversion timing will be derived from the TX Counter A, TX Counter B, and TA, TA′, and TB registers, rather than the RX Counter A, RX Counter B, and RA, RA′, and RB registers. In this case, the AIC $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ timing will be identical during primary data communication; however, $\overline{\text{FSR}}$ will not be asserted during secondary data communication since there is no new A/D conversion result. The synchronous operation sequences are as follows (see Figure 5). L Serial port directly interfaces with the serial port of the TMS320C17 and communicates in two 8-bit bytes. The operation sequence is as follows (see Figure 5): 1. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought low. 2. One 8-bit byte is transmitted and one 8-bit byte is received. 3. The $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ pins are brought low. 4. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins emit positive frame-sync pulses that are four Shift Clock cycles wide. 5. One 8-bit byte is transmitted and one 8-bit byte is received. 6. The $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ pins are brought high. 7. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought high. H Serial port directly interfaces with the serial ports of the TMS32020, TMS320C25, and TMS320C30, and communicates in one 16-bit word. The operation sequence is as follows (see Figure 5): 1. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought low. 2. One 16-bit word is transmitted and one 16-bit word is received. 3. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought high. 4. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pins emit low-going pulses. Since the transmit and receive sections of the AIC are now synchronous, the AIC serial port, with additional NOR and AND gates, will interface to two SN74299 serial-to-parallel shift registers. Interfacing the AIC to the SN74299 shift register allows the AIC to interface to an external FIFO RAM and facilitates parallel, data bus communications between the AIC and the digital signal processor. The operation sequence is the same as the above sequence (see Figure 5).

INTERNAL TIMING CONFIGURATION



NOTE: Frequency 1, 20.736 MHz, is used to show how 153.6 kHz (for a commercially available modem split-band filter clock), popular speech and modem sampling signal frequencies, and an internal 288-kHz switched-capacitor filter clock can be derived synchronously and as submultiples of the crystal oscillator frequency. Since these derived frequencies are synchronous submultiples of the crystal frequency, aliasing does not occur as the sampled analog signal passes between the analog converter and switched-capacitor filter stages. Frequency 2, 41.472 MHz, is used to show that the AIC can work with high-frequency signals, which are used by high-speed digital signal processors.

†Split-band filtering can alternatively be performed after the analog input function via software in the TMS320.

‡These control bits are described in the AIC DX Data Word Format section.

explanation of internal timing configuration

All of the internal timing of the AIC is derived from the high-frequency clock signal that drives the Master Clock input pin. The Shift Clock signal, which strobes the serial port data between the AIC and DSP, is derived by dividing the Master Clock input signal frequency by four.

Low-pass:

$$\text{SCF Clock Frequency (D/A or A/D Path)} = \frac{\text{Master Clock Frequency}}{2 \times \text{Contents of Counter A}}$$

$$\text{Conversion Frequency} = \frac{\text{SCF Clock Frequency (D/A or A/D Path)}}{\text{Contents of Counter B}}$$

High-pass:

$$\text{SCF Clock Frequency (A/D Path)} = \text{A/D Conversion Frequency}$$

$$\text{Shift Clock Frequency} = \frac{\text{Master Clock Frequency}}{4}$$

TX Counter A and TX Counter B, which are driven by the Master Clock signal, determine the D/A conversion timing. Similarly, RX Counter A and RX Counter B determine the A/D conversion timing. In order for the low-pass switched-capacitor filter in the D/A path to meet its transfer function specifications, the frequency of its clock input must be 288 kHz. If the clock frequency is not 288 kHz, the filter transfer function frequencies are frequency-scaled by the ratios of the clock frequency to 288 kHz. Thus, to obtain the specified filter response, the combination of Master Clock frequency and TX Counter A and RX Counter A values must yield a 288-kHz switched-capacitor clock signal. This 288-kHz clock signal can then be divided by the TX Counter B to establish the D/A conversion timing.

The transfer function of the bandpass switched-capacitor filter in the A/D path is a composite of its high-pass and low-pass section transfer functions. The high-frequency roll-off of the low-pass section will meet the bandpass filter transfer function specification when the low-pass section SCF is 288 kHz. Otherwise, the high-frequency roll-off will be frequency-scaled by the ratio of the high-pass section's SCF clock to 288 kHz. The low-frequency roll-off of the high-pass section will meet the bandpass filter transfer function specification when the A/D conversion rate is 8 kHz. Otherwise, the low-frequency roll-off of the high-pass section will be frequency-scaled by the ratio of the A/D conversion rate to 8 kHz.

TX Counter A and TX Counter B are reloaded every D/A conversion period, while RX Counter A and RX Counter B are reloaded every A/D conversion period. The TX Counter B and RX Counter B are loaded with the values in the TB and RB Registers, respectively. Via software control, the TX Counter A can be loaded with either the TA Register, the TA Register less the TA' Register, or the TA Register plus the TA' Register. By selecting the TA Register less the TA' Register option, the upcoming conversion timing will occur earlier by an amount of time that equals TA' times the signal period of the Master Clock. By selecting the TA Register plus the TA' Register option, the upcoming conversion timing will occur later by an amount of time that equals TA' times the signal period of the Master Clock. Thus, the D/A conversion timing can be advanced or retarded. An identical ability to alter the A/D conversion timing is provided. In this case, however, the RX Counter A can be programmed via software control with the RA Register, the RA Register less the RA' Register, or the RA Register plus the RA' Register.

The ability to advance or retard conversion timing is particularly useful for modem applications. This feature allows controlled changes in the A/D and D/A conversion timing. This feature can be used to enhance signal-to-noise performance, to perform frequency-tracking functions, and to generate nonstandard modem frequencies.

If the transmit and receive sections are configured to be synchronous (see WORD/$\overline{\text{BYTE}}$ pin description), then both the low-pass and bandpass switched-capacitor filter clocks are derived from TX Counter A. Also, both the D/A and A/D conversion timing are derived from the TX Counter A and TX Counter B. When the transmit and receive sections are configured to be synchronous, the RX Counter A, RX Counter B, RA Register, RA' Register, and RB Registers are not used.

AIC DR or DX word bit pattern

A/D or D/A MSB, 1st bit sent — 1st bit sent of 2nd byte — A/D or D/A LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

AIC DX data word format section

d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	COMMENTS
primary DX serial communication protocol																
← d15 (MSB) through d2 go to the D/A converter register →														0	0	The TX and RX Counter A's are loaded with the TA and RA register values. The TX and RX Counter B's are loaded with TB and RB register values.
← d15 (MSB) through d2 go to the D/A converter register →														0	1	The TX and RX Counter A's are loaded with the TA + TA' and RA + RA' register values. The TX and RX Counter B's are loaded with the TB and RB register values. NOTE: d1 = 0, d0 = 1 will cause the next D/A and A/D conversion periods to be changed by the addition of TA' and RA' Master Clock cycles, in which TA' and RA' can be positive or negative or zero. Please refer to Table 1. AIC Responses to Improper Conditions.
← d15 (MSB) through d2 go to the D/A converter register →														1	0	The TX and RX Counter A's are loaded with the TA − TA' and RA − RA' register values. The TX and RX Counter B's are loaded with the TB and RB register values. NOTE: d1 = 1, d0 = 0 will cause the next D/A and A/D conversion periods to be changed by the subtraction of TA' and RA' Master Clock cycles, in which TA' and RA' can be positive or negative or zero. Please refer to Table 1. AIC Responses to Improper Conditions.
← d15 (MSB) through d2 go to the D/A converter register →														1	1	The TX and RX Counter A's are loaded with the TA and RA register converter register values. The TX and RX Counter B's are loaded with the TB and RB register values. After a delay of four Shift Clock cycles, a secondary transmission will immediately follow to program the AIC to operate in the desired configuration.

NOTE: Setting the two least significant bits to 1 in the normal transmission of DAC information (Primary Communications) to the AIC will initiate Secondary Communications upon completion of the Primary Communications.

Upon completion of the Primary Communication, $\overline{\text{FSX}}$ will remain high for four SHIFT CLOCK cycles and will then go low and initiate the Secondary Communication. The timing specifications for the Primary and Secondary Communications are identical. In this manner, the Secondary Communication, if initiated, is interleaved between successive Primary Communications. This interleaving prevents the Secondary Communication from interfering with the Primary Communications and DAC timing, thus preventing the AIC from skipping a DAC output. It is important to note that in the synchronous mode, $\overline{\text{FSR}}$ will not be asserted during Secondary Communications.

secondary DX serial communication protocol

x x | ← to TA register → | x x | ← to RA register → | 0 0	d13 and d6 are MSBs (unsigned binary)
x | ← to TA′ register → | x | ← to RA′ register → | 0 1	d14 and d7 are 2's complement sign bits
x | ← to TB register → | x | ← to RB register → | 1 0	d14 and d7 are MSBs (unsigned binary)
x x x x x x d9 x d7 d6 d5 d4 d3 d2 1 1 (CONTROL REGISTER)	d2 = 0/1 deletes/inserts the A/D highpass filter d3 = 0/1 disables/enables the loopback function d4 = 0/1 disables/enables the AUX IN+ and AUX IN− pins d5 = 0/1 asynchronous/synchronous transmit and receive sections d6 = 0/1 gain control bits (see Gain Control Section) d7 = 0/1 gain control bits (see Gain Control Section) d9 = 0/1 delete/insert on-board second-order (sin x)/x correction filter

reset function

A reset function is provided to initiate serial communications between the AIC and DSP. The reset function will initialize all AIC registers, including the control register. After power has been applied to the AIC, a negative-going pulse on the $\overline{\text{RESET}}$ pin will initialize the AIC registers to provide an 8-kHz A/D and D/A conversion rate for a 5.184 MHz master clock input signal. The AIC, excepting the CONTROL register, will be initialized as follows (see AIC DX Data Word Format section):

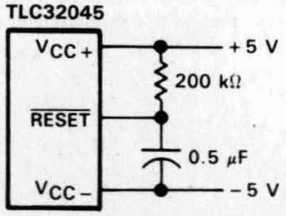
REGISTER	INITIALIZED REGISTER VALUE (HEX)
TA	9
TA′	1
TB	24
RA	9
RA′	1
RB	24

The CONTROL register bits will be reset as follows (see AIC DX Data Word Format section):

d9 = 1, d7 = 1, d6 = 1, d5 = 1, d4 = 0, d3 = 0, d2 = 1

This initialization allows normal serial port communications to occur between AIC and DSP. If the transmit and receive sections are configured to operate synchronously and the user wishes to program different conversion rates, only the TA, TA′, and TB register need to be programmed, since both transmit and receive timing are synchronously derived from these registers (see the Pin Descriptions and AIC DX Word Format sections).

The circuit shown below will provide a reset on power-up when power is applied in the sequence given under Power-Up Sequence. The circuit depends on the power supplies' reaching their recommended values a minimum of 800 ns before the capacitor charges to 0.8 V above DGTL GND.



power-up sequence

To ensure proper operation of the AIC, and as a safeguard against latch-up, it is recommmended that Schottky diodes with forward voltages less than or equal to 0.4 V be connected from V_{CC-} to ANLG GND and from V_{CC-} to DGTL GND (see Figure 21). In the absence of such diodes, power should be applied in the following sequence: ANLG GND and DGTL GND, V_{CC-}, then V_{CC+} and V_{DD}. Also, no input signal should be applied until after power-up.

AIC responses to improper conditions

The AIC has provisions for responding to improper conditions. These improper conditions and the response of the AIC to these conditions are presented in Table 1 below.

AIC register constraints

The following constraints are placed on the contents of the AIC registers:

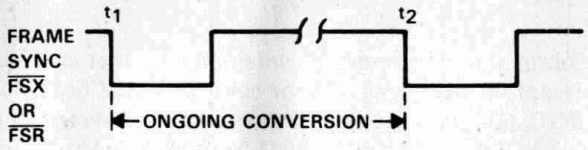
1. TA register must be ≥ 4 in word mode (WORD/$\overline{\text{BYTE}}$ = High).
2. TA register must be ≥ 5 in byte mode (WORD/$\overline{\text{BYTE}}$ = Low).
3. TA′ register can be either positive, negative, or zero.
4. RA register must be ≥ 4 in word mode (WORD/$\overline{\text{BYTE}}$ = High).
5. RA register must be ≥ 5 in byte mode (WORD/$\overline{\text{BYTE}}$ = Low).
6. RA′ register can be either positive, negative, or zero.
7. (TA register ± TA′ register) must be > 1.
8. (RA register ± RA′ register) must be > 1.
9. TB register must be > 1.

TABLE 1. AIC RESPONSES TO IMPROPER CONDITIONS

IMPROPER CONDITION	AIC RESPONSE
TA register + TA′ register = 0 or 1 TA register − TA′ register = 0 or 1	Reprogram TX Counter A with TA register value
TA register + TA′ register < 0	MODULO 64 arithmetic is used to ensure that a positive value is loaded into the TX Counter A, i.e., TA register + TA′ register + 40 HEX is loaded into TX Counter A.
RA register + RA′ register = 0 or 1 RA register − RA′ register = 0 or 1	Reprogram RX Counter A with RA register value
RA register + RA′ register = 0 or 1	MODULO 64 arithmetic is used to ensure that a positive value is loaded into RX Counter A, i.e., RA register + RA′ register + 40 HEX is loaded into RX Counter A.
TA register = 0 or 1 RA register = 0 or 1	AIC is shut down.
TA register < 4 in word mode TA register < 5 in byte mode RA register < 4 in word mode RA register < 5 in byte mode	The AIC serial port no longer operates.
TB register = 0 or 1	Reprogram TB register with 24 HEX
RB register = 0 or 1	Reprogram RB register with 24 HEX
AIC and DSP cannot communicate	Hold last DAC output

improper operation due to conversion times being too close together

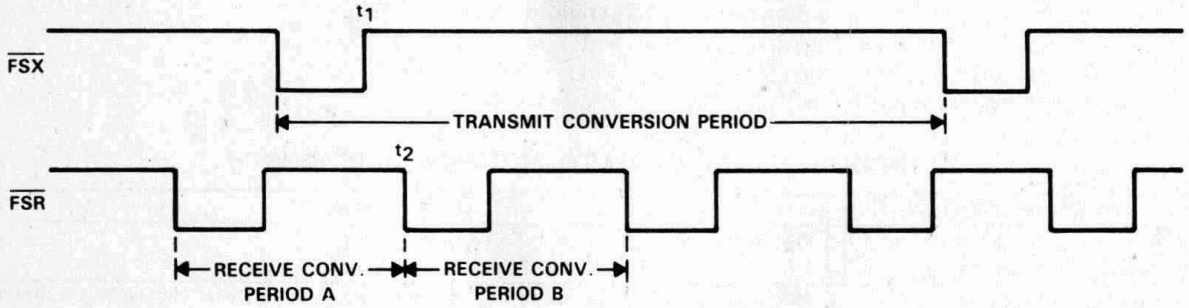
If the difference between two successive D/A conversion frame syncs is less that 1/19.2 kHz, the AIC operates improperly. In this situation, the second D/A conversion frame sync occurs too quickly and there is not enough time for the ongoing conversion to be completed. This situation can occur if the A and B registers are improperly programmed or if the A + A′ register or A − A′ register result is too small. When incrementally adjusting the conversion period via the A + A′ register options, the designer should be very careful not to violate this requirement (see following diagram).



$t_2 - t_1 \geq 1/19.2$ kHz

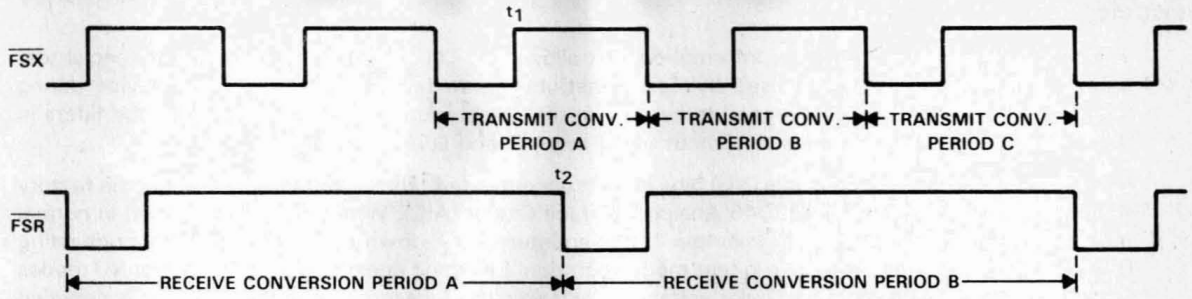
asynchronous operation — more than one receive frame sync occurring between two transmit frame syncs

When incrementally adjusting the conversion period via the A + A′ or A − A′ register options, a specific protocol is followed. The command to use the incremental conversion period adjust option is sent to the AIC during a $\overline{\text{FSX}}$ frame sync. The ongoing conversion period is then adjusted. However, either Receive Conversion Period A or B may be adjusted. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. Therefore, if there is sufficient time between t1 and t2, the receive conversion period adjustment will be performed during Receive Conversion Period A. Otherwise, the adjustment will be performed during Receive Conversion Period B. The adjustment command only adjusts one transmit conversion period and one receive conversion period. To adjust another pair of transmit and receive conversion periods, another command must be issued during a subsequent $\overline{\text{FSX}}$ frame (see figure below).



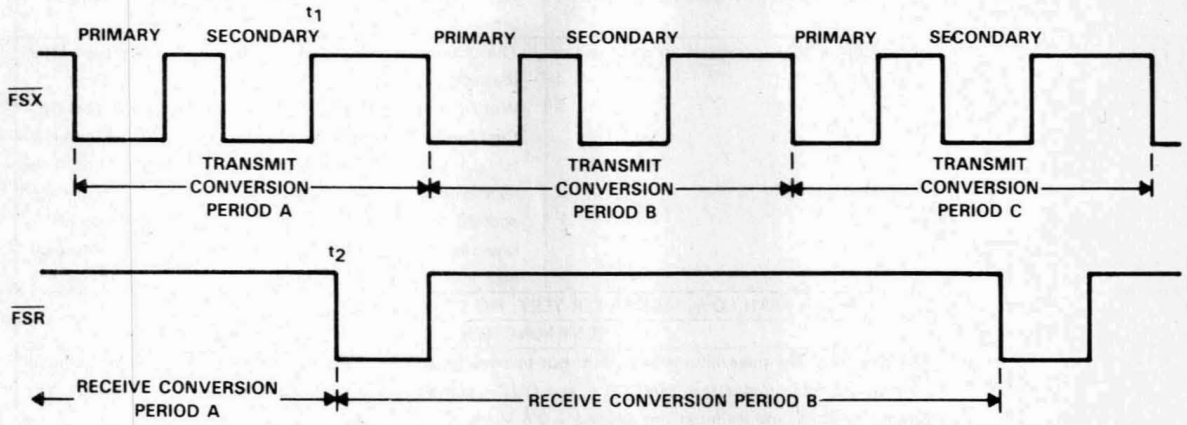
asynchronous operation — more than one transmit frame sync occurring between two receive frame syncs

When incrementally adjusting the conversion period via the A + A′ or A − A′ register options, a specific protocol is followed. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. The command to use the incremental conversion period adjust options is sent to the AIC during a $\overline{\text{FSX}}$ frame sync. The ongoing transmit conversion period is then adjusted. However, three possibilities exist for the receive conversion period adjustment in the diagram as shown in the following figure. If the adjustment command is issued during Transmit Conversion Period A, Receive Conversion Period A will be adjusted if there is sufficient time between t1 and t2. Or, if there is not sufficient time between t1 and t2, Receive Conversion Period B will be adjusted. Or, the receive portion of an adjustment command may be ignored if the adjustment command is sent during a receive conversion period, which is already being or will be adjusted due to a prior adjustment command. For example, if adjustment commands are issued during Transmit Conversion Periods A, B, and C, the first two commands may cause Receive Conversion Periods A and B to be adjusted, while the third receive adjustment command is ignored. The third adjustment command is ignored since it was issued during Receive Conversion Period B, which already will be adjusted via the Transmit Conversion Period B adjustment command.



asynchronous operation — more than one set of primary and secondary DX serial communication occurring between two receive frame sync (see AIC DX Data Word Format section)

The TA, TA′, TB, and control register information that is transmitted in the secondary communications is always accepted and is applied during the ongoing transmit conversion period. If there is sufficient time between t1 and t2, the TA, RA′, and RB register information, which is sent during Transmit Conversion Period A, will be applied to Receive Conversion Period A. Otherwise, this information will be applied during Receive Conversion Period B. If RA, RA′, and RB register information has already been received and is being applied during an ongoing conversion period, any subsequent RA, RA′, or RB information that is received during this receive conversion period will be disregarded (see diagram below).



test modes†

The following paragraph provides information that allows the TLC32045 to be operated in special test modes. These test modes are used by Texas Instruments to facilitate testing of the device during manufacturing. They are not intended to be used in real applications, however, they allow the filters in the A/D and D/A paths to be used without using the A/D and D/A converters.

In normal operation, the nonusable (NU) pins are left unconnected. These NU pins are used by the factory to speed up testing of the TLC32045 Analog Interface Circuit (AIC). When the device is used in normal (non-test mode) operation, the NU pin (pin 1) has an internal pull-down to −5 V. Externally connecting 0 V or 5 V to pin 1 puts the device in test-mode operation. Selecting one of the possible test or NU modes is accomplished by placing a particular voltage on certain pins. A description of these modes is provided in Table 2 and Figures 1 and 2.

TABLE 2. LIST OF TEST MODES

TEST PINS	D/A PATH TEST (PIN 1 to 5 V)	A/D PATH TEST (PIN 1 to 0)
	TEST FUNCTION	TEST FUNCTION
5	The low-pass switched-capacitor filter clock is brought out to pin 5. This clock signal is normally internal.	The bandpass switched-capacitor filter clock is brought out to pin 5. This clock signal is normally internal.
11	No change from normal operation. The $\overline{\text{EODX}}$ signal is brought out to pin 11.	The pulse that initiates the A/D conversion is brought out here. This signal is normally internal.
3	The pulse that initiates the D/A conversion is brought out here.	No change from normal operation. The EODR signal is brought out.
27 and 28	There are no test output signals provided on these pins.	The outputs of the A/D path low-pass or bandpass filter (depending upon control bit d2 — see AIC DX Data Word Format section) are brought out to these pins. If the high-pass section is inserted, the output will have a (sinx)/x droop. The slope of the droop will be determined by the ADC sampling frequency, which is the high-pass section clock frequency (see diagram of bandpass or low-pass filter test for receive section). These outputs will drive small (30-pF) loads.
	D/A PATH LOW-PASS FILTER TEST; PIN 13 (WORD/BYTE) to −5 V	
	TEST FUNCTION	
15 and 16	The inputs of the D/A path low-pass filter are brought out to pins 15 and 16. The D/A input to this filter is removed. If the (sin x)/x correction filter is inserted, the OUT+ and OUT− signals will have a flat response (see Figure 2). The common-mode range of these inputs must not exceed ±0.5 V.	

† In the test mode, the AIC responds to the setting of Pin 13 to −5 V, as if Pin 13 were set to 0 V. Thus, the byte mode is selected for communicating between DSP and AIC. Either of the path tests (D/A or A/D) can be performed simultaneously with the D/A low-pass filter test. In this situation, Pin 13 must be connected to −5 V, which initiates byte-mode communications.

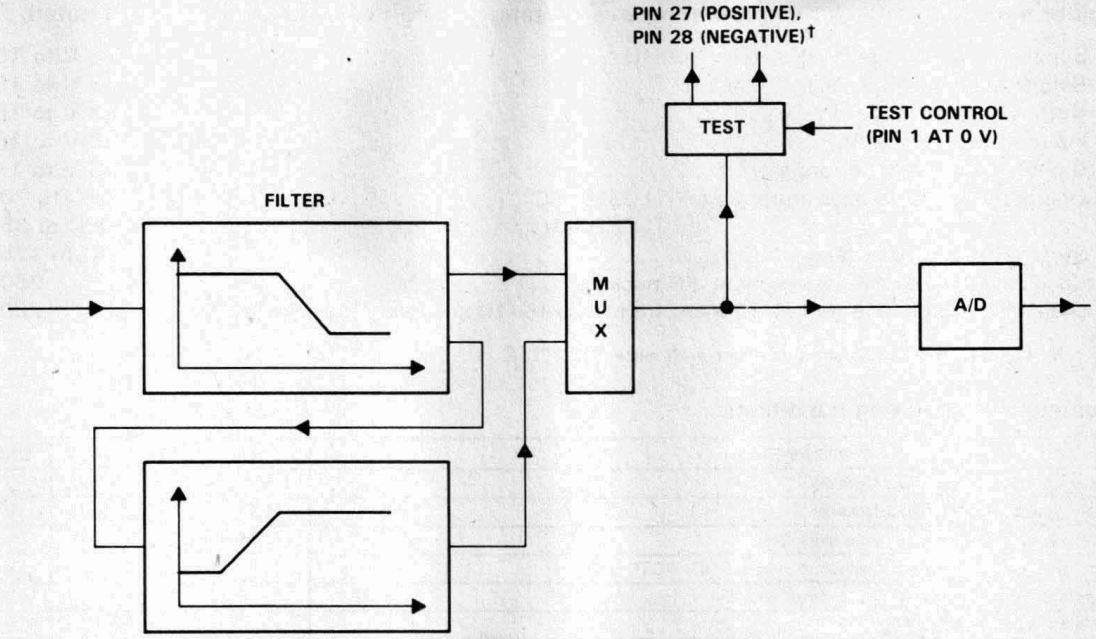


FIGURE 1. BANDPASS OR LOW-PASS FILTER TEST FOR RECEIVER SECTION

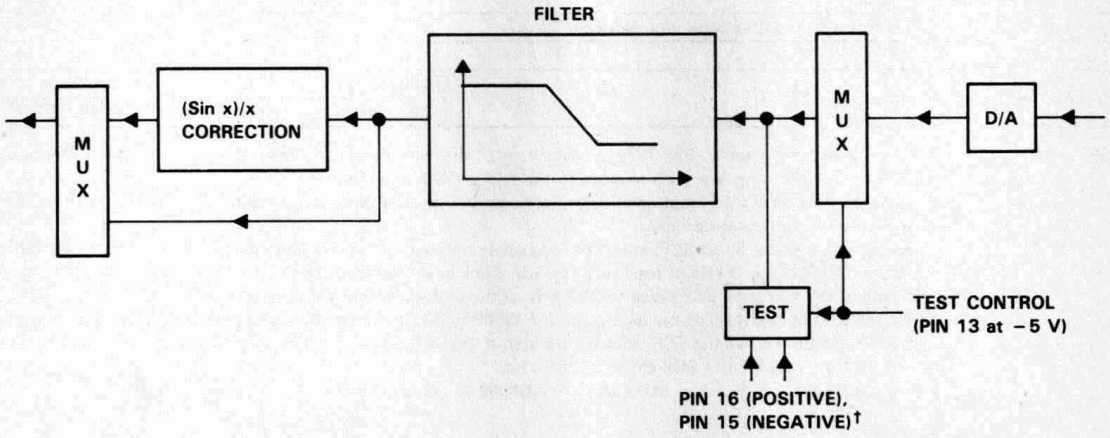


FIGURE 2. LOW-PASS FILTER TEST FOR TRANSMIT SECTION

†All analog signal paths have differential architecture and hence have positive and negative components.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC+} (see Note 1) . . . . . −0.3 V to 15 V
Supply voltage range, V_{DD} . . . . . −0.3 V to 15 V
Output voltage range, V_O . . . . . −0.3 V to 15 V
Input voltage range, V_I . . . . . −0.3 V to 15 V
Digital ground voltage range . . . . . −0.3 V to 15 V
Operating free-air temperature range: TLC32045C . . . . . 0°C to 70°C
TLC32045I . . . . . −40°C to 85°C
Storage temperature range . . . . . −40°C to 125°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTE 1: Voltage values for maximum ratings are with respect to VCC−.

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} (see Note 2)		4.75	5	5.25	V
Supply voltage, V_{CC-} (see Note 2)		−4.75	−5	−5.25	V
Digital supply voltage, V_{DD} (see Note 2)		4.75	5	5.25	V
Digital ground voltage with respect to ANLG GND, DGTL GND			0		V
Reference input voltage, $V_{ref(ext)}$ (see Note 2)		2		4	V
High-level input voltage, V_{IH}		2		V_{DD}+0.3	V
Low-level input voltage, V_{IL} (see Note 3)		−0.3		0.8	V
Load resistance at OUT+ and/or OUT−, R_L		300			Ω
Load capacitance at OUT+ and/or OUT−, C_L				100	pF
MSTR CLK frequency (see Note 4)		0.075	5	10.368	MHz
Analog input amplifier common mode input voltage (see Note 5)				±1.5	V
A/D or D/A conversion rate				20	kHz
Operating free-air temperature, T_A	TLC32045C	0		70	°C
	TLC32045I	−40		85	

NOTES: 2. Voltages at analog inputs and outputs, REF, V_{CC+}, and V_{CC-}, are with respect to the ANLG GND terminal. Voltages at digital inputs and outputs and V_{DD} are with respect to the DGTL GND terminal.
3. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels and temperature only.
4. The bandpass switched-capacitor filter (SCF) specifications apply only when the low-pass section SCF clock is 288 kHz and the high-pass section SCF clock is 8 kHz. If the low-pass SCF clock is shifted from 288 kHz, the low-pass roll-off frequency will shift by the ratio of the low-pass SCF clock to 288 kHz. If the high-pass SCF clock is shifted from 8 kHz, the high-pass roll-off frequency will shift by the ratio of the high-pass SCF clock to 8 kHz. Similarly, the low-pass switched-capacitor filter (SCF) specifications apply only when the SCF clock is 288 kHz. If the SCF clock is shifted from 288 kHz, the low-pass roll-off frequency will shift by the ratio of the SCF clock to 288 kHz.
5. This range applies when (IN+ − IN−) or (AUX IN+ − AUX IN−) equals ±6 V.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (unless otherwise noted)

total device, MSTR CLK frequency = 5.184 MHz, outputs not loaded

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 4.75 V, I_{OH} = −300 μA	2.4			V
V_{OL}	Low-level output voltage		V_{DD} = 4.75 V, I_{OL} = 2 mA			0.4	V
I_{CC+}	Supply current from V_{CC+}	TLC32045C				40	mA
		TLC32045I				45	
I_{CC-}	Supply current from V_{CC-}	TLC32045C				−40	mA
		TLC32045I				−45	
I_{DD}	Supply current from V_{DD}		$f_{MSTR\ CLK}$ = 5.184 MHz			7	mA
V_{ref}	Internal reference output voltage			2.9		3.4	V
αV_{ref}	Temperature coefficient of internal reference voltage				200		ppm/°C
r_o	Output resistance at REF				100		kΩ

receive amplifier input

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	A/D converter offset error (filters in)			10	75	mV
CMRR	Common-mode rejection ratio at IN+, IN−, or AUX IN+, AUX IN−	See Note 6		55		dB
r_I	Input resistance at IN+, IN− or AUX IN+, AUX IN−, REF			100		kΩ

transmit filter output

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OO}	Output offset voltage at OUT+ or OUT− (single-ended relative to ANLG GND)			15	80	mV
V_{OM}	Maximum peak output voltage swing across R_L at OUT+ or OUT− (single-ended)	$R_L \geq 300\ \Omega$, Offset voltage = 0	±3			V
V_{OM}	Maximum peak output voltage swing between OUT+ and OUT− (differential output)	$R_L \geq 600\ \Omega$	±6			V

†All typical values are at T_A = 25°C.

NOTE 6: The test condition is a 0-dBm, 1-kHz input signal with an 8-kHz conversion rate.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (unless otherwise noted)

system distortion specifications, SCF clock frequency = 288 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Attenuation of second harmonic of A/D input signal	single-ended	V_{in} = −0.5 dB to −24 dB referred to V_{ref}, See Note 7		70		dB
	differential		55	70		
Attenuation of third and higher harmonics of A/D input signal	single-ended	V_{in} = −0.5 dB to −24 dB referred to V_{ref}, See Note 7		65		dB
	differential		55	65		
Attenuation of second harmonic of D/A input signal	single-ended	V_{in} = −0 dB to −24 dB referred to V_{ref}, See Note 7		70		dB
	differential		55	70		
Attenuation of third and higher harmonics of D/A input signal	single-ended	V_{in} = −0 dB to −24 dB referred to V_{ref}, See Note 7		65		dB
	differential		55	65		

A/D channel signal-to-distortion ratio

PARAMETER	TEST CONDITIONS (see Note 7)	A_v = 1‡		A_v = 2‡		A_v = 4‡		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
A/D channel signal-to-distortion ratio	V_{in} = −6 dB to −0.1 dB	55		>55§		>55§		dB
	V_{in} = −12 dB to −6 dB	55		55		>55§		
	V_{in} = −18 dB to −12 dB	53		55		55		
	V_{in} = −24 dB to −18 dB	47		53		55		
	V_{in} = −30 dB to −24 dB	41		47		53		
	V_{in} = −36 dB to −30 dB	35		41		47		
	V_{in} = −42 dB to −36 dB	29		35		41		
	V_{in} = −48 dB to −42 dB	23		29		35		
	V_{in} = −54 dB to −48 dB	17		23		29		

D/A channel signal-to-distortion ratio

PARAMETER	TEST CONDITIONS (see Note 7)	MIN	MAX	UNIT
D/A channel signal-to-distortion ratio	V_{in} = −6 dB to 0 dB	55		dB
	V_{in} = −12 dB to −6 dB	55		
	V_{in} = −18 dB to −12 dB	53		
	V_{in} = −24 dB to −18 dB	47		
	V_{in} = −30 dB to −24 dB	41		
	V_{in} = −36 dB to −30 dB	35		
	V_{in} = −42 dB to −36 dB	29		
	V_{in} = −48 dB to −42 dB	23		
	V_{in} = −54 dB to −48 dB	17		

†All typical values are at T_A = 25°C.
‡ A_v is the programmable gain of the input amplifier.
§ A value >55 is over range and signal clipping occurs.
NOTE 7: The test condition is a 1-kHz input signal with an 8-kHz conversion rate (0 dB relative to V_{ref}). The load impedance for the DAC is 600 Ω.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (unless otherwise noted)

gain and dynamic range

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Absolute transmit gain tracking error while transmitting into 600 Ω	−42 dB to 0 dB signal range, See Note 8		±0.05	±0.15	dB
Absolute receive gain tracking error	−42 dB to 0 dB signal range, See Note 8		±0.05	±0.15	dB
Absolute gain of the A/D channel	Signal input is a −0.5-dB, 1-kHz sinewave		0.2		dB
Absolute gain of the D/A channel	Signal input is a 0-dB, 1-kHz sinewave		−0.3		dB

power supply rejection and crosstalk attenuation

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{CC+} or V_{CC-} supply voltage rejection ratio, receive channel	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at DR (ADC output)		30		dB
	f = 30 kHz to 50 kHz			45		
V_{CC+} or V_{CC-} supply voltage rejection ratio, transmit channel (single-ended)	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at OUT+		30		dB
	f = 30 kHz to 50 kHz			45		
Crosstalk attenuation, transmit-to-receive (single-ended)				80		dB

†All typical values are at T_A = 25°C.

NOTE 8: Gain tracking is relative to the absolute gain at 1 kHz and 0 dB (0 dB relative to V_{ref}).

delay distortion

bandpass filter transfer function, SCF f_{clock} = 288 kHz IN+ – IN– is a ±3 V sinewave† (see Note 9)

PARAMETER	TEST CONDITION	FREQUENCY RANGE	ADJUSTMENT ADDEND‡	MIN	TYP§	MAX	UNIT
Gain relative to gain at 1 kHz (except passband ripple specification)	Input signal reference is 0 dB (see Note 9)	f ≤ 50 Hz	IK1 × 0 dB	–33	–29	–25	dB
		f = 100 Hz	K1 × – 0.26 dB	–4	–2	–1	
		f = 150 Hz to 3100 Hz	K1 × 0 dB	–0.25	0	0.25	
		f = 3100 Hz to 3300 Hz	K1 × 0 dB	–0.3	0	0.3	
		f = 3300 Hz to 3650 Hz	K1 × 0 dB	–0.5	0	0.5	
		f = 3800 Hz	K1 × 2.3 dB	–5	–3	–1	
		f = 4000 Hz	K1 × 2.7 dB	–20	–17	–16	
		f ≥ 4400 Hz	K1 × 3.2 dB			–40	
		f ≥ 5000 Hz	K1 × 0 dB			–65	

low-pass filter transfer function (see curves), SCF f_{clock} = 288 kHz (see Note 9)

PARAMETER	TEST CONDITION	FREQUENCY RANGE	ADJUSTMENT ADDEND‡	MIN	TYP§	MAX	UNIT
Gain relative to gain at 1 kHz (except passband ripple specification)	Input signal reference is 0 dB (see Note 9)	f = 0 Hz to 3100 Hz	K1 × 0 dB	–0.25	0	0.25	dB
		f = 3100 Hz to 3300 Hz	K1 × 0 dB	–0.3	0	0.3	
		f = 3300 Hz to 3650 Hz	K1 × 0 dB	–0.5	0	0.5	
		f = 3800 Hz	K1 × 2.3 dB	–5	–3	–1	
		f = 4000 Hz	K1 × 2.7 dB	–20	–17	–16	
		f ≥ 4400 Hz	K1 × 3.2 dB			–40	
		f ≥ 5000 Hz	K1 × 0 dB			–65	

serial port

PARAMETER		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –300 μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4	V
I_I	Input current				±10	μA
C_i	Input capacitance			15		pF
C_o	Output capacitance			15		pF

† See filter curves in typical characteristics.

‡ The MIN, TYP, and MAX specifications are given for a 288-kHz SCF clock frequency. A slight error in the 288-kHz SCF may result from inaccuracies in the MSTR CLK frequency, resulting from crystal frequency tolerances. If this frequency error is less than 0.25%, the ADJUSTMENT ADDEND should be added to the MIN, TYP, and MAX specifications, where K1 = 100 • [(SCF frequency – 288 kHz)/ 288 kHz]. For errors greater than 0.25%, see Note 10.

§ All typical values are at T_A = 25°C.

NOTE 9: The filter gain outside of the passband is measured with respect to the gain at 1 kHz. The filter gain within the passband is measured with respect to the average gain within the passband. The passbands are 150 to 3600 Hz and 0 to 3600 Hz for the bandpass and low-pass filters respectively. For switched-capacitor filter clocks at frequencies other than 288 kHz, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 288 kHz.

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V

noise (measurement includes low-pass and bandpass switched-capacitor filters)

PARAMETER		TEST CONDITIONS	TYP†	MAX	UNIT
Transmit noise	with (sin x)/x correction	DX input = 00000000000000, constant input code		600	μV rms
	without (sin x)/x correction			450	μV rms
			24		dBrnc0
Receive noise (see Note 10)		Inputs grounded, gain = 1		530	μV rms
			24		dBrnc0

timing requirements

serial port recommended input signals

PARAMETER		MIN	MAX	UNIT
$t_{c(MCLK)}$	Master clock cycle time	95		ns
$t_{r(MCLK)}$	Master clock rise time		10	ns
$t_{f(MCLK)}$	Master clock fall time		10	ns
	Master clock duty cycle	25%	75%	
	$\overline{\text{RESET}}$ pulse duration (see Note 11)	800		ns
$t_{su(DX)}$	DX setup time before SCLK↓	20		ns
$t_{h(DX)}$	DX hold time after SCLK↓	$t_{c(SCLK)}/4$		ns

NOTES: 10. The noise is computed by statistically evaluating the digital output of the A/D converter.
11. $\overline{\text{RESET}}$ pulse duration is the amount of time that the reset pin is held below 0.8 V after the power supplies have reached their recommended values.

serial port—AIC output signals, C_L = 30 pF for SHIFT CLK output, C_L = 15 pF for all other outputs

PARAMETER		MIN	TYP†	MAX	UNIT
$t_{c(SCLK)}$	Shift clock (SCLK) cycle time	380			ns
$t_{f(SCLK)}$	Shift clock (SCLK) fall time		3	8	ns
$t_{r(SCLK)}$	Shift clock (SCLK) rise time		3	8	ns
	Shift clock (SCLK) duty cycle	45		55	%
$t_{d(CH-FL)}$	Delay from SCLK↑ to $\overline{\text{FSR}}$/$\overline{\text{FSX}}$/$\overline{\text{FSD}}$↓		30		ns
$t_{d(CH-FH)}$	Delay from SCLK↑ to $\overline{\text{FSR}}$/$\overline{\text{FSX}}$/$\overline{\text{FSD}}$↑		35	90	ns
$t_{d(CH-DR)}$	DR valid after SCLK↑			90	ns
$t_{dw(CH-EL)}$	Delay from SCLK↑ to $\overline{\text{EODX}}$/$\overline{\text{EODR}}$↓ in word mode			90	ns
$t_{dw(CH-EH)}$	Delay from SCLK↑ to $\overline{\text{EODX}}$/$\overline{\text{EODR}}$↑ in word mode			90	ns
$t_{f(EODX)}$	$\overline{\text{EODX}}$ fall time		2	8	ns
$t_{f(EODR)}$	$\overline{\text{EODR}}$ fall time		2	8	ns
$t_{db(CH-EL)}$	Delay from SCLK↑ to $\overline{\text{EODX}}$/$\overline{\text{EODR}}$↓ in byte mode			90	ns
$t_{db(CH-EH)}$	Delay from SCLK↑ to $\overline{\text{EODX}}$/$\overline{\text{EODR}}$↑ in byte mode			90	ns
$t_{d(MH-SL)}$	Delay from MSTR CLK↑ to SCLK↓		65	170	ns
$t_{d(MH-SH)}$	Delay from MSTR CLK↑ to SCLK↑		65	170	ns

†Typical values are at T_A = 25°C.

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (continued)

serial port — AIC output signals

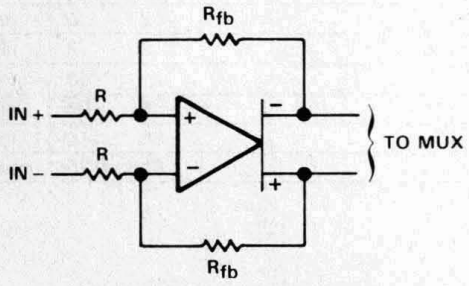
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{c(SCLK)}$	Shift clock (SCLK) cycle time		380			ns
$t_{f(SCLK)}$	Shift clock (SCLK) fall time				50	ns
$t_{r(SCLK)}$	Shift clock (SCLK) rise time				50	ns
	Shift clock (SCLK) duty cycle		45		55	%
$t_{d(CH-FL)}$	Delay from SCLK↑ to $\overline{FSR}/FSX$↓	C_L = 50 pF			52	ns
$t_{d(CH-FH)}$	Delay from SCLK↑ to $\overline{FSR}/FSX$↑	C_L = 50 pF			52	ns
$t_{d(CH-DR)}$	DR valid after SCLK↑				90	ns
$t_{dw(CH-EL)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↓ in word mode				90	ns
$t_{dw(CH-EH)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↑ in word mode				90	ns
$t_{f(EODX)}$	$\overline{EODX}$ fall time				15	ns
$t_{f(EODR)}$	$\overline{EODR}$ fall time				15	ns
$t_{db(CH-EL)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↓ in byte mode				100	ns
$t_{db(CH-EH)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↑ in byte mode				100	ns
$t_{d(MH-SL)}$	Delay from MSTR CLK↑ to SCLK↓			65		ns
$t_{d(MH-SH)}$	Delay from MSTR CLK↑ to SCLK↑			65		ns

†Typical values are at T_A = 25°C.

TABLE 3. GAIN CONTROL TABLE
(ANALOG INPUT SIGNAL REQUIRED FOR FULL-SCALE A/D CONVERSION)

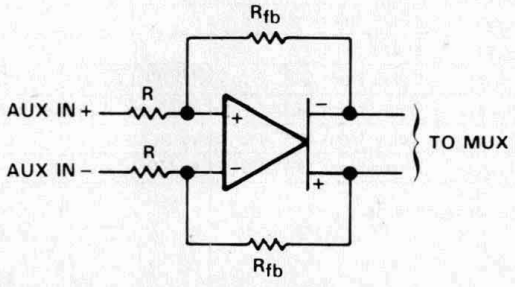
INPUT CONFIGURATIONS	CONTROL REGISTER BITS		ANALOG INPUT‡	A/D CONVERSION RESULT
	d6	d7		
Differential configuration	1	1	±6 V	full-scale
Analog input = IN+ − IN−	0	0		
= AUX IN+ − AUX IN−	1	0	±3 V	full-scale
	0	1	±1.5 V	full-scale
Single-ended configuration	1	1	±3 V	half-scale
Analog input = IN+ − ANLG GND	0	0		
= AUX IN+ − ANLG GND	1	0	±3 V	full-scale
	0	1	±1.5 V	full-scale

‡In this example, V_{ref} is assumed to be 3 V. In order to minimize distortion, it is recommended that the analog input not exceed 0.1 dB below full scale.



R_{fb} = R for d6 = 1, d7 = 1
d6 = 0, d7 = 0
R_{fb} = 2R for d6 = 1, d7 = 0
R_{fb} = 4R for d6 = 0, d7 = 1

FIGURE 3. IN+ AND IN− GAIN CONTROL CIRCUITRY



R_{fb} = R for d6 = 1, d7 = 1
d6 = 0, d7 = 0
R_{fb} = 2R for d6 = 1, d7 = 0
R_{fb} = 4R for d6 = 0, d7 = 1

FIGURE 4. AUX IN+ AND AUX IN− GAIN CONTROL CIRCUITRY

(sin x)/x correction section

If the designer does not wish to use the on-board second-order (sin x)/x correction filter, correction can be accomplished in digital signal processor (DSP) software. (Sin x)/x correction can be accomplished easily and efficiently in digital signal processor (DSP) software. Excellent correction accuracy can be achieved to a band edge of 3000 Hz by using a first-order digital correction filter. The results, which are shown below, are typical of the numerical correction accuracy that can be achieved for sample rates of interest. The filter requires only seven instruction cycles per sample on the TMS320 DSPs. With a 200-ns instruction cycle, nine instructions per sample represents an overhead factor of 1.4% and 1.7% for sampling rates of 8000 Hz and 9600 Hz, respectively. This correction will add a slight amount of group delay at the upper edge of the 300–3000-Hz band.

(sin x)/x roll-off for a zero-order hold function

The (sin x)/x roll-off for the AIC DAC zero-order hold function at a band-edge frequency of 3000 Hz for the various sampling rates is shown in the table below.

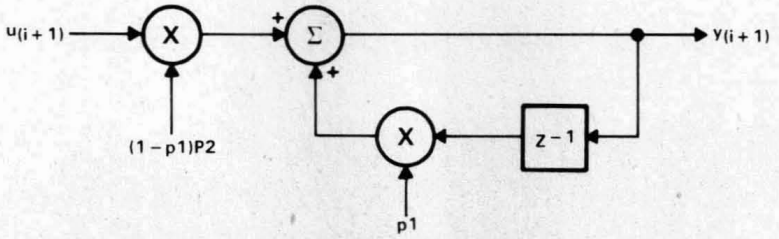
TABLE 4. (sin x)/x ROLL-OFF

f_S (Hz)	$20 \log \frac{\sin \pi f/f_S}{\pi f/f_S}$ (f = 3000 Hz) (dB)
7200	−2.64
8000	−2.11
9600	−1.44
14400	−0.63
19200	−0.35

Note that the actual AIC (sin x)/x roll-off will be slightly less than the above figures, because the AIC has less than a 100% duty cycle hold interval.

correction filter

To compensate for the (sin x)/x roll-off of the AIC, a first-order correction filter shown below, is recommended.



The difference equation for this correction filter is:

$$y_{i+1} = p2(1-p1)\,(u_{i+1}) + p1\,y_i$$

where the constant p1 determines the pole locations.

The resulting squared magnitude transfer function is:

$$|H(f)|^2 = \frac{p2^2\,(1-p1)^2}{1 - 2p1\cos(2\pi f/f_S) + p1^2}$$

correction results

Table 5 below shows the optimum p values and the corresponding correction results for 8000-Hz and 9600-Hz sampling rates.

TABLE 5

f (Hz)	ERROR (dB) f_S = 8000 Hz p1 = −0.14813 p2 = 0.9888	ERROR (dB) f_S = 9600 Hz p1 = −0.1307 p2 = 0.9951
300	−0.099	−0.043
600	−0.089	−0.043
900	−0.054	0
1200	−0.002	0
1500	0.041	0
1800	0.079	0.043
2100	0.100	0.043
2400	0.091	0.043
2700	−0.043	0
3000	−0.102	−0.043

TMS320 software requirements

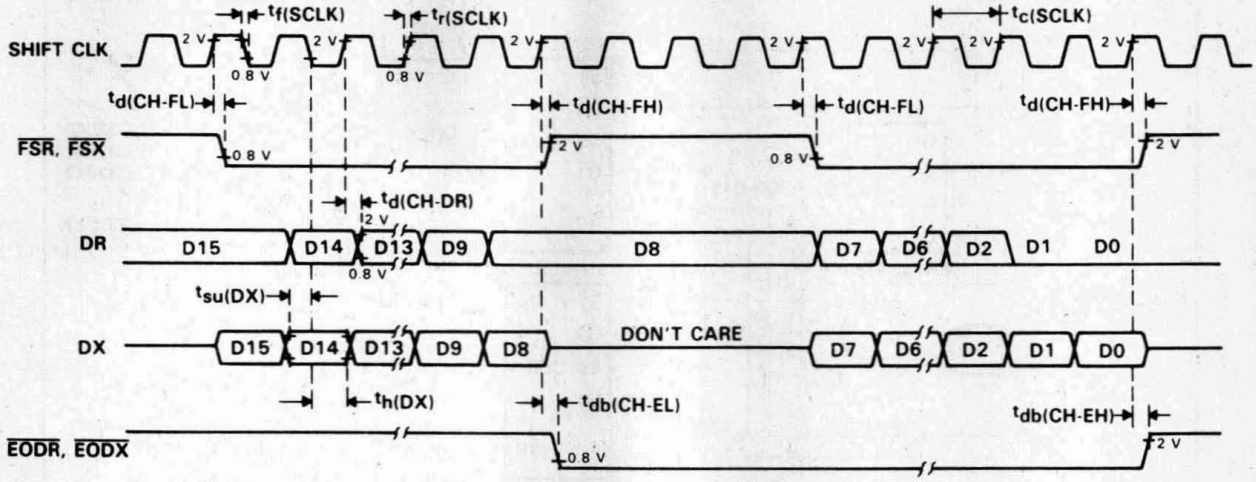
The digital correction filter equation can be written in state variable form as follows:

$$Y = k1Y + k2U$$

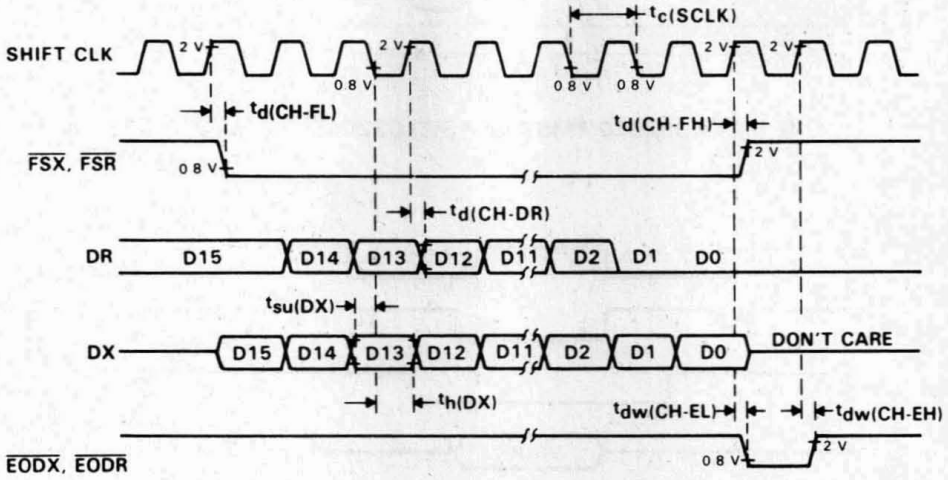
where k1 equals p1 (from the preceding page), k2 equals (1 − p1)p2 (from the preceding page), Y is the filter state, and U is the next I/O sample. The coefficients k1 and k2 must be represented as 16-bit integers. The SACH instruction (with the proper shift) will yield the correct result. With the assumption that the TMS320 processor page pointer and memory configuration are properly initialized, the equation can be executed in seven instructions or seven cycles with the following program:

```
ZAC
LT K2
MPY U
LTA K1
MPY Y
APAC
SACH (dma), (shift)
```

byte-mode timing



word-mode timing



shift-clock timing

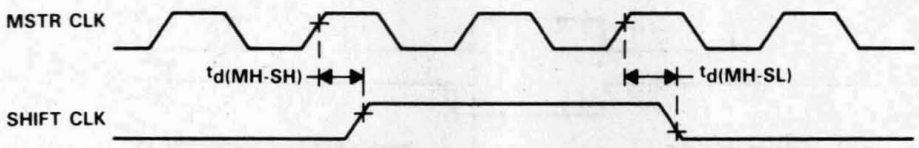


FIGURE 5. SERIAL PORT TIMING

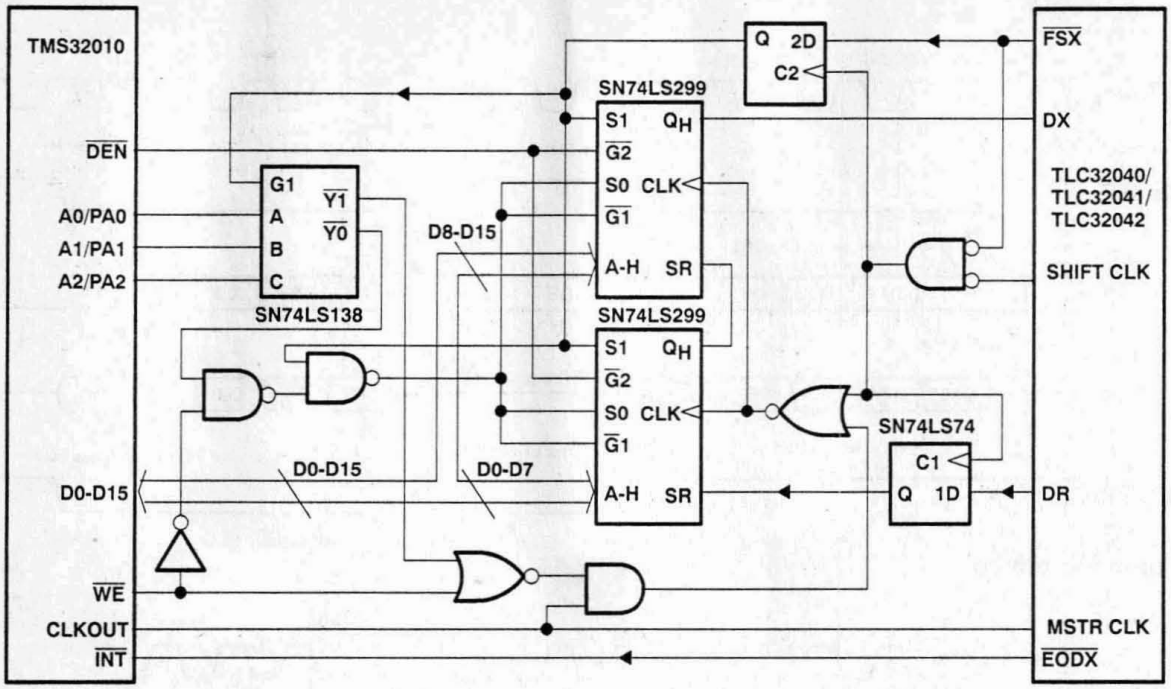
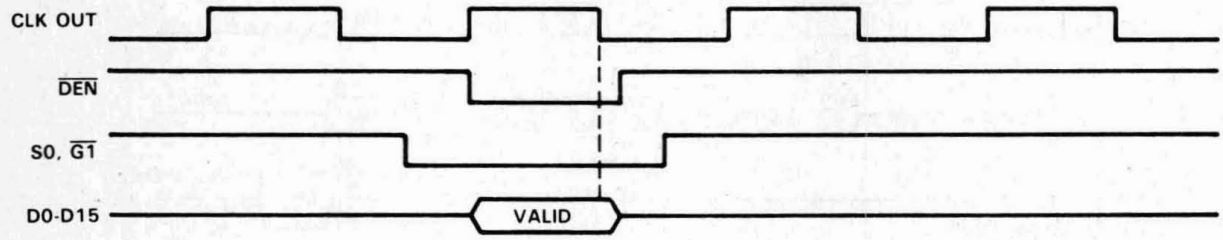


FIGURE 6. TMS32010/TMS320C15-TLC32045 INTERFACE CIRCUIT

in instruction timing



out instruction timing

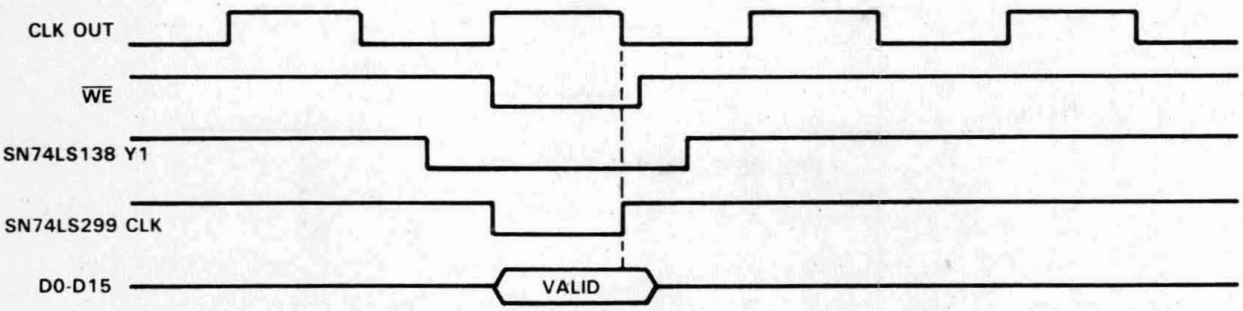


FIGURE 7. TMS32010/TMS320C15-TLC32045 INTERFACE TIMING

TYPICAL CHARACTERISTICS

AIC TRANSMIT AND RECEIVE LOW-PASS FILTER

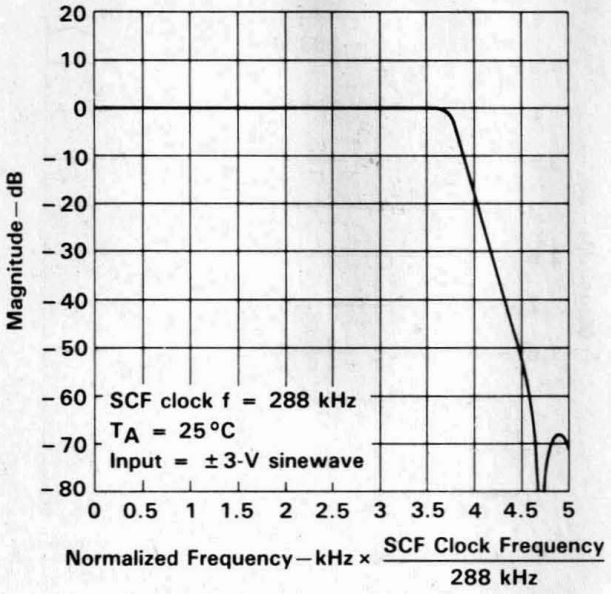


FIGURE 8

AIC TRANSMIT AND RECEIVE LOW-PASS FILTER

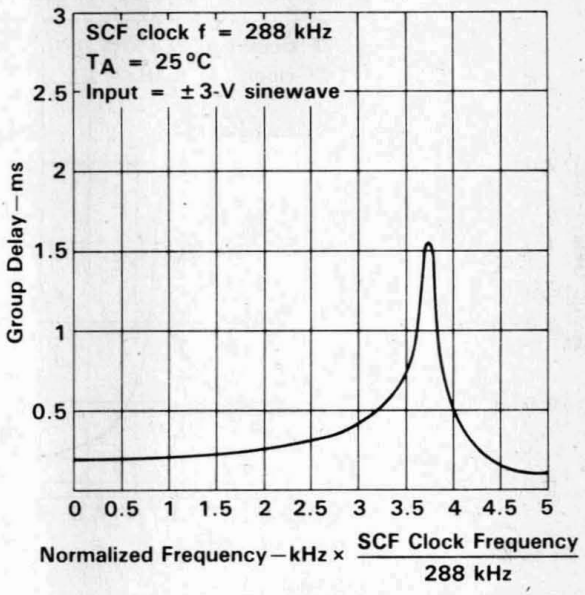


FIGURE 9

AIC RECEIVE-CHANNEL BANDPASS FILTER

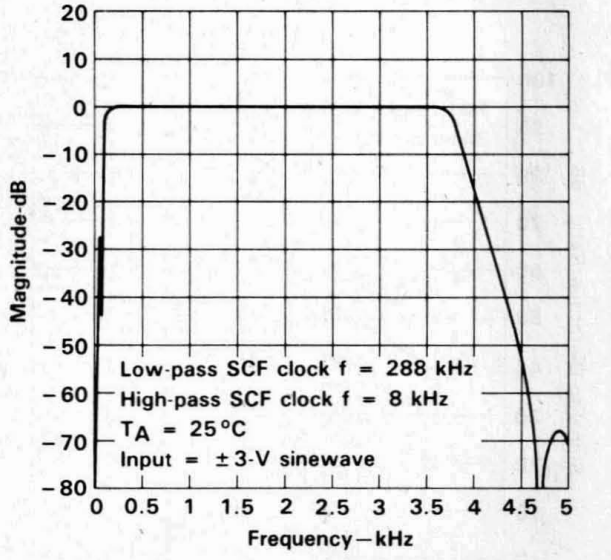


FIGURE 10

AIC RECEIVE-CHANNEL HIGH-PASS FILTER

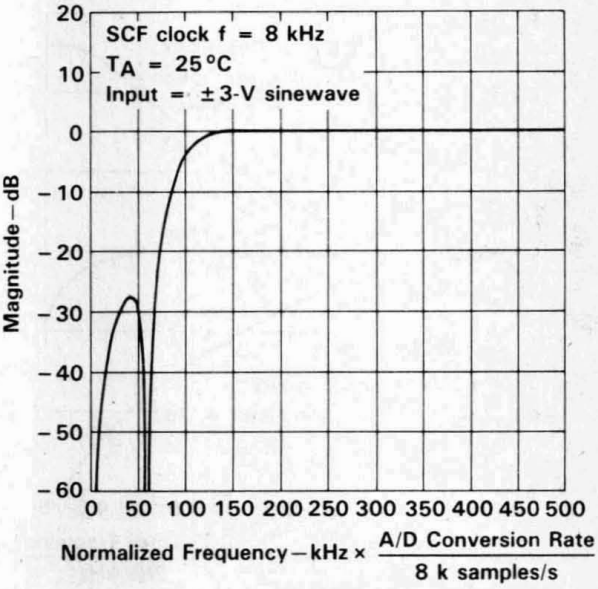


FIGURE 11

TYPICAL CHARACTERISTICS

AIC RECEIVE CHANNEL BANDPASS FILTER

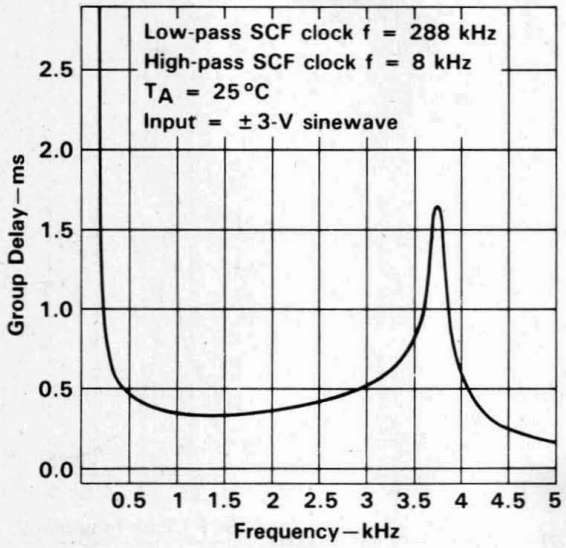


FIGURE 12

AIC (SIN X)/X CORRECTION FILTER

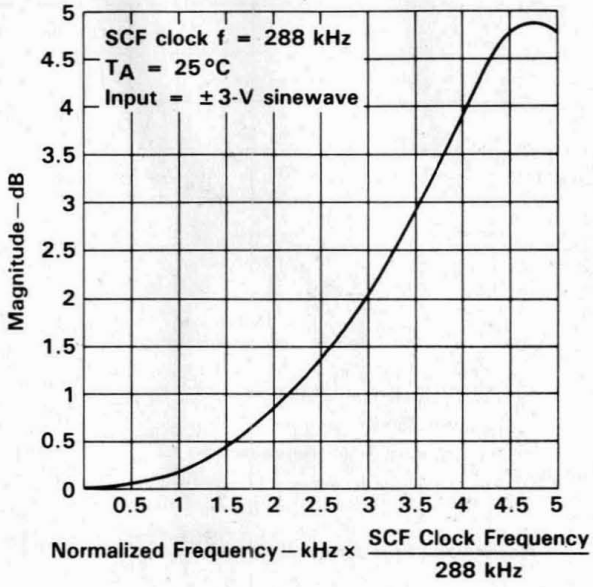


FIGURE 13

(SIN X)/X CORRECTION FILTER

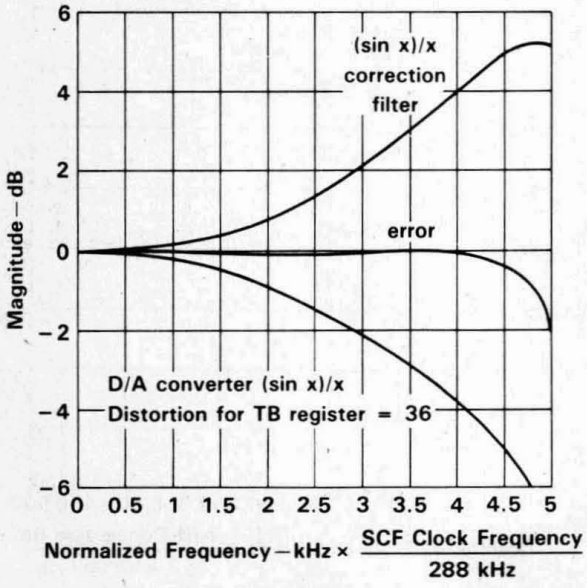


FIGURE 14

A/D SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL

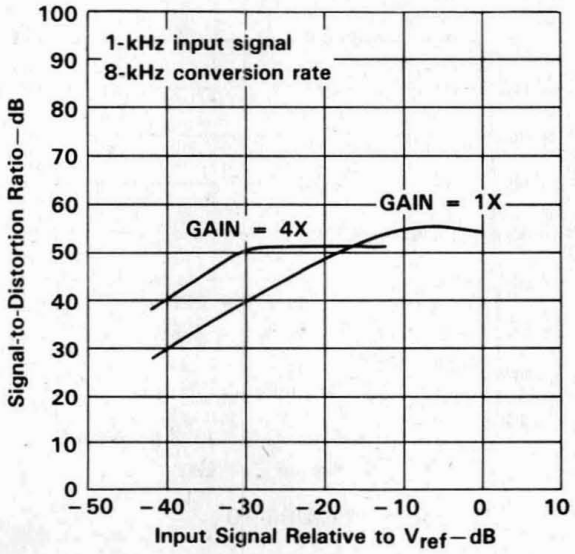


FIGURE 15

TYPICAL CHARACTERISTICS

A/D GAIN TRACKING
(GAIN RELATIVE TO GAIN AT 0 dB INPUT SIGNAL)

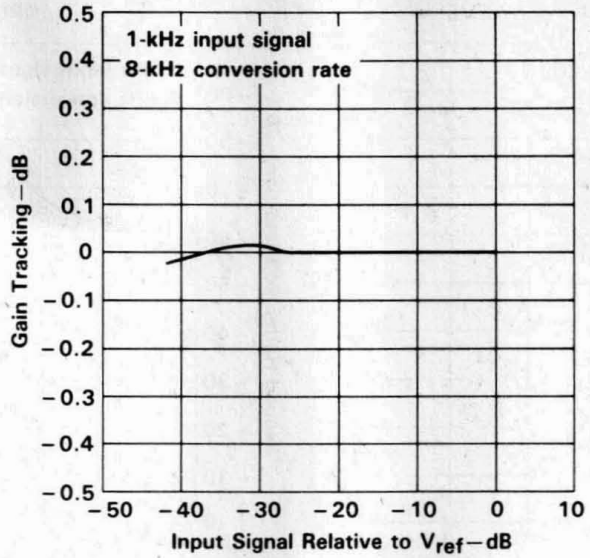


FIGURE 16

D/A CONVERTER SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL LEVEL

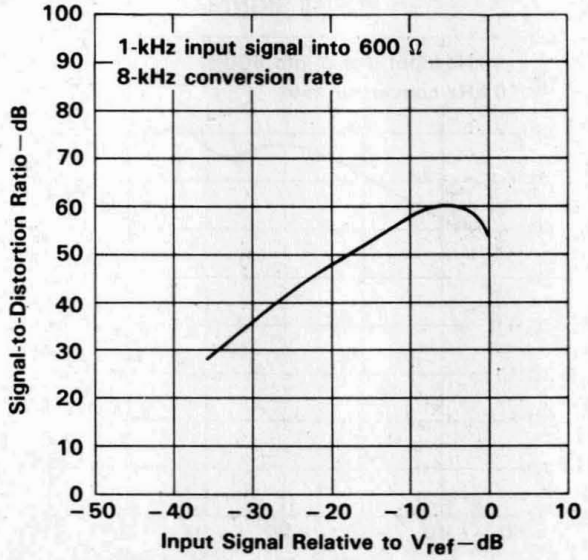


FIGURE 17

TYPICAL CHARACTERISTICS

D/A GAIN TRACKING
(GAIN RELATIVE TO GAIN
AT 0 dB INPUT SIGNAL LEVEL)

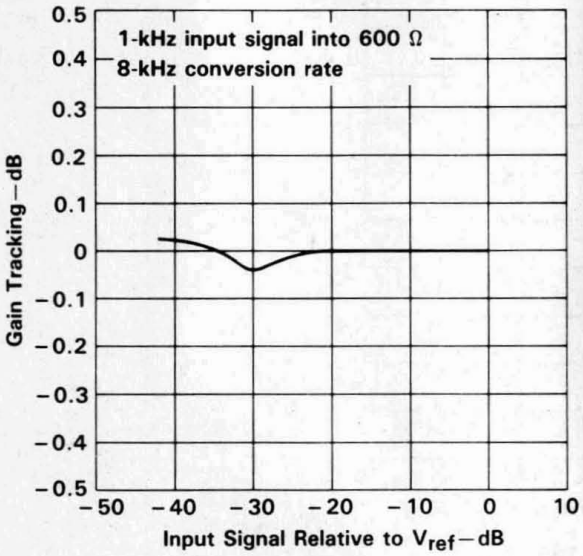


FIGURE 18

A/D SECOND HARMONIC DISTORTION
vs
INPUT SIGNAL

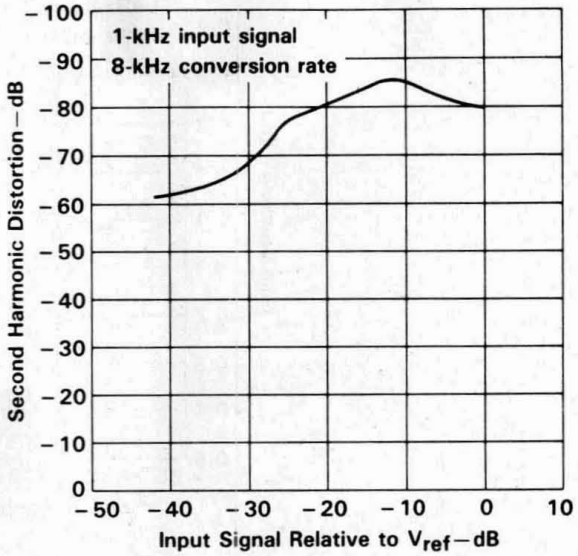


FIGURE 19

D/A SECOND HARMONIC DISTORTION
vs
INPUT SIGNAL

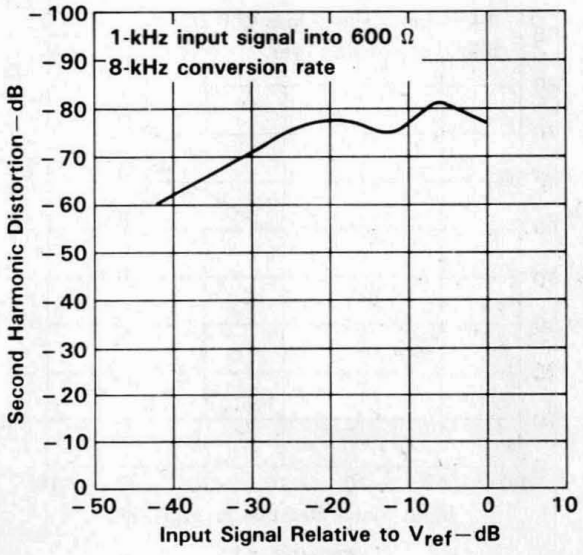


FIGURE 20

TYPICAL CHARACTERISTICS

A/D THIRD HARMONIC DISTORTION
vs
INPUT SIGNAL

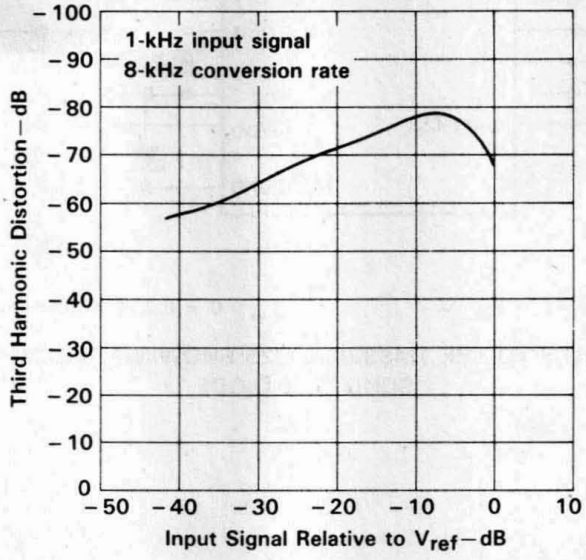


FIGURE 21

D/A THIRD HARMONIC DISTORTION
vs
INPUT SIGNAL

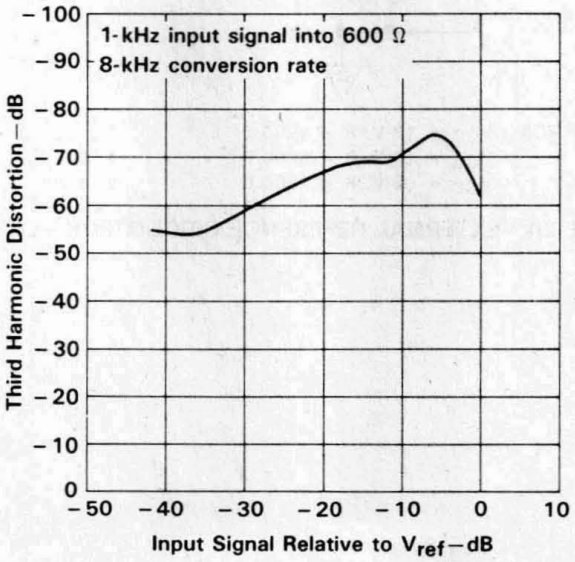
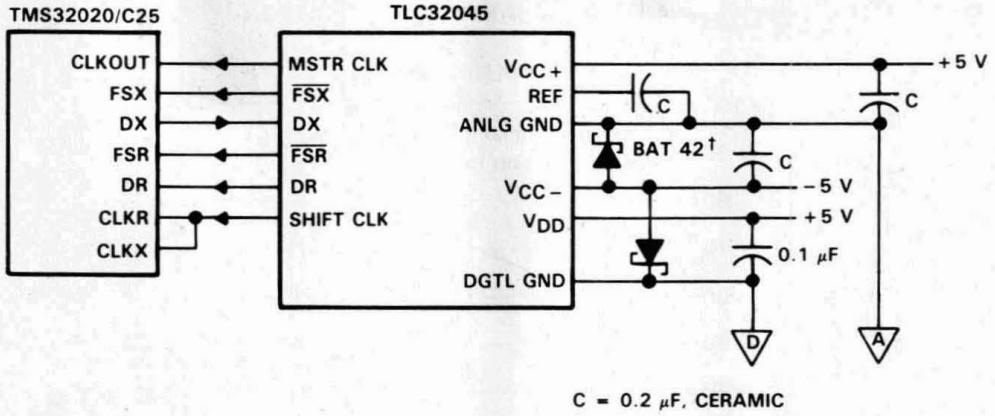


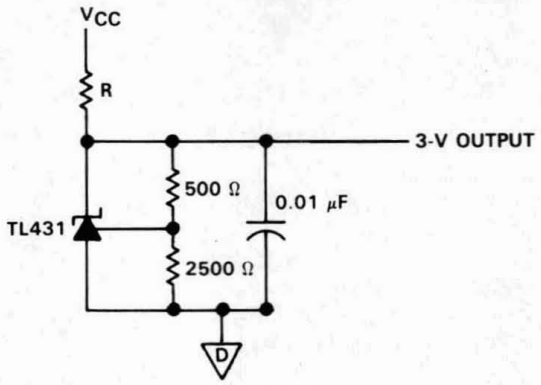
FIGURE 22

TYPICAL APPLICATION INFORMATION



C = 0.2 μF, CERAMIC

FIGURE 23. AIC INTERFACE TO THE TMS32020/C25 SHOWING DECOUPLING CAPACITORS AND SCHOTTKY DIODE



FOR: V_{CC} = 12 V, R = 7200 Ω
V_{CC} = 10 V, R = 5600 Ω
V_{CC} = 5 V, R = 1600 Ω

FIGURE 24. EXTERNAL REFERENCE CIRCUIT FOR TLC32045

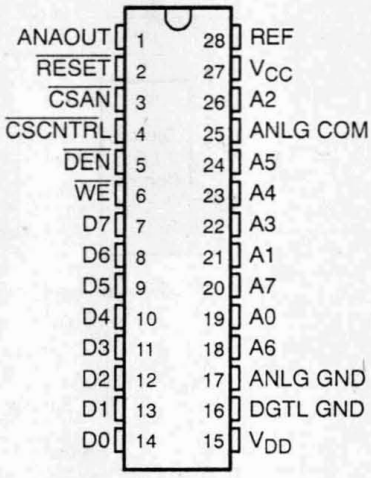
†Thomson Semiconductors

See the TLC32046 Wide-Band Analog Interface Circuits Data Manual in Section 9 for product information.

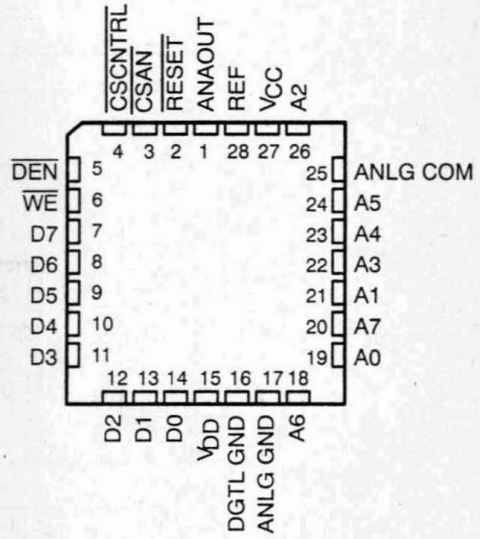
See the TLC32047 Wide-Band Analog Interface Circuits Data Manual in Section 9 for product information.

- **Advanced LinCMOS™ Technology**
- **8-Bit Analog-to-Digital Converter**
- **8-Bit Digital-to-Analog Converter**
- **Monotonic Over Entire Analog-to-Digital and Digital-to-Analog Conversion Range**
- **8-Input Analog Multiplexer with Latched Channel Select**
- **Programmable Input Range on Two Input Amplifiers**
- **Interfaces Directly to Many Digital Signal Processors Including the TMS320 Family**
- **Low-Glitch Impulse at DAC Output**
- **Built-In Scaling and Level Shifting on Six of the Analog Inputs**
- **Designed for Servo-Loop Control Systems Including Disk Drives**

N PACKAGE
(TOP VIEW)



FN CHIP CARRIER PACKAGE
(T0P VIEW)



description

The TLC32071 is an analog interface integrated circuit that converts between the analog and digital domains. The device includes an 8-bit voltage-output digital-to-analog converter (DAC), an 8-bit analog-to-digital converter (ADC), an analog input multiplexer with eight analog inputs, an output reference MUX, and a high-speed 8-bit bidirectional data bus that interfaces directly to the TMS320 family of digital signal processors. The reset input ($\overline{\text{RESET}}$) is used to clear the DAC and control registers. The 8-bit DAC converts digital signals to the equivalent analog values. The DAC is followed by a level shifter, which adjusts the center of the DAC output range to the voltage externally applied to the ANLG COM input. One of three output ranges can be selected by an internal register.

The 8-bit ADC converts any one of eight analog inputs selected by a programmable internal register through an input multiplexer. Six of these have inverting inputs with built-in level shifting so that these six output ranges are centered at the ADC input voltage midpoint. Two of the six inputs have register selectable gains. The first conversion result after selection of one of the six inverting inputs should be discarded as invalid. The two remaining inputs are direct inputs to the ADC multiplexer with output ranges centered at the internal 2.5-V reference (V_{ref}). After reset, this reference is available at the REF output. The REF output can also be programmed by an internal control register to provide access to other internal references, any of the analog inputs after scaling and shifting, or the unscaled output of the DAC.

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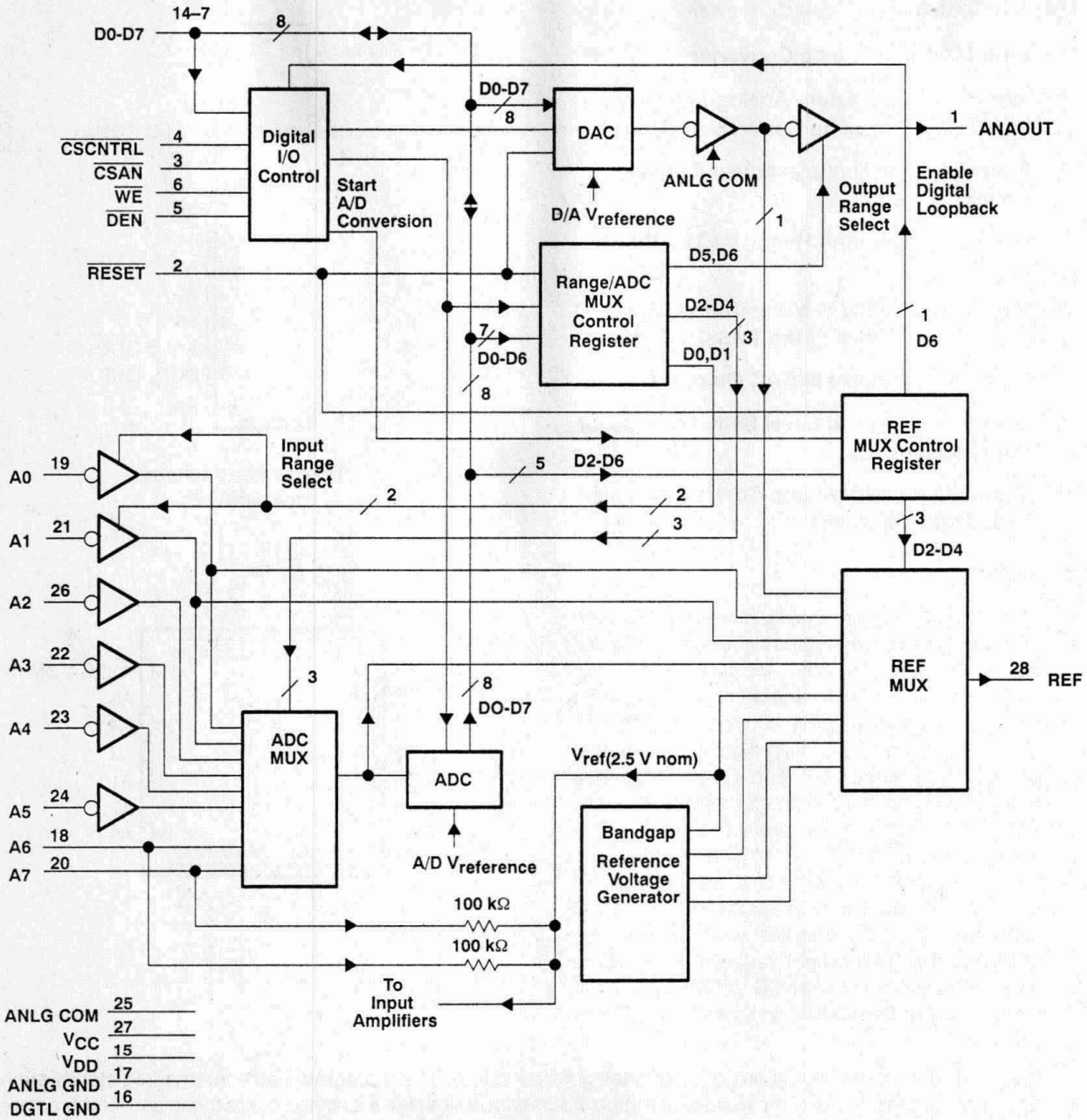
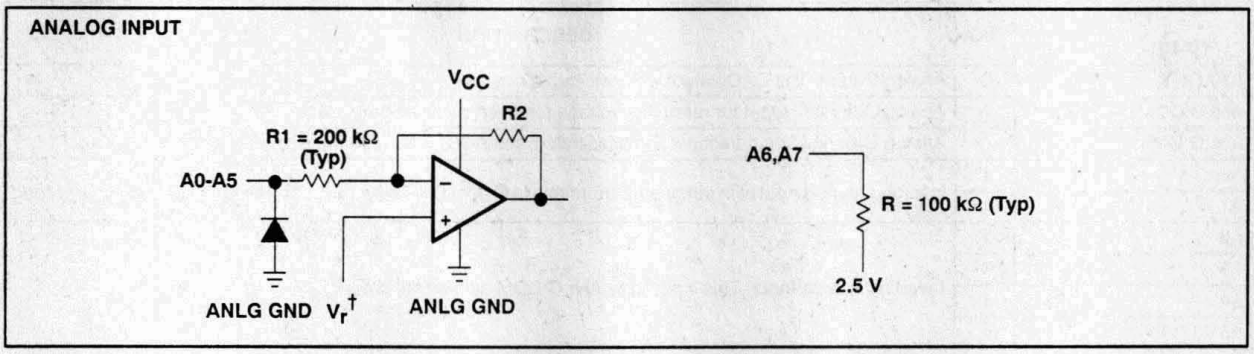
functional block diagram



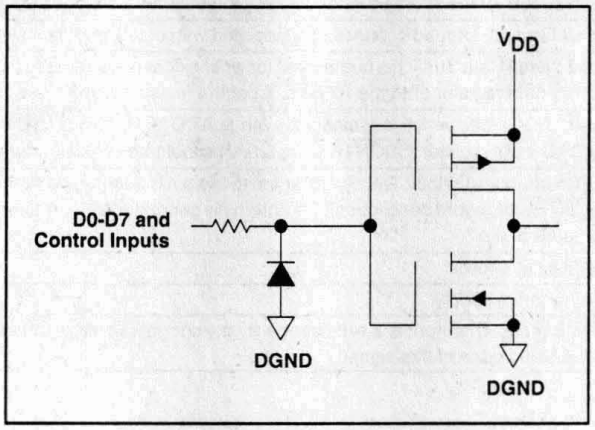
All resistor values shown are nominal.

equivalents of analog input circuit



† V_r is an internally generated voltage with the following typical values: at range = 1, V_r = 3.33 V; at range = 1/2, V_r = 3.75; at range = 1/4, V_r = 4.167 V.

equivalent of digital input circuit



Terminal Functions

PIN NAME	PIN NO.	I/O	DESCRIPTION
ANAOUT	1	O	Analog Output. The DAC output with selectable ranges.
ANLG COM	25	I	Analog Common. Input for reference voltage for inverting analog inputs.
ANLG GND	17		Analog Ground. Ground connection associated with ADC, DAC, and other analog circuits.
A0	19	I	Inverting Analog input with range programmable to 8, 4, or 2 V. This input uses ANLG COM as a signal ground.
A1	21	I	
A2	26	I	Inverting Analog Input. This input uses ANLG COM as a signal ground.
A3	22	I	
A4	23	I	
A5	24	I	
A6	18	I	Auxiliary noninverting analog input with input range of 0.5 to 4.5 V. This input uses the internal reference VR2.5 as a signal ground.
A7	20	I	
$\overline{\text{CSAN}}$	3	I	Chip select for writing to the D/A converter and reading the results of an A/D conversion.
$\overline{\text{CSCNTRL}}$	4	I	Chip select for the control register, which selects DAC and ADC ranges and the analog input channel.
$\overline{\text{DEN}}$	5	I	Read strobe for the A/D converter output. Output buffers are enabled when this signal is held low.
DGTL GND	16		Digital Ground. Ground connection associated with digital data-bus signals and other digital circuits.
D7–D0	7–14	I/O	Bidirectional Data Bus. This bus is used for writing conversion data to the DAC, writing data to the range/ADC MUX control register or to the REF MUX control register, and for reading the ADC conversion result.
$\overline{\text{RESET}}$	2	I	Reset. This strobe, when low, clears the range/ADC MUX control register, the REF MUX control register, and the DAC input register. $\overline{\text{CSCNTRL}}$ and $\overline{\text{CSAN}}$ should be held high during a reset operation.
REF	28	O	2.5-V Reference Output. The signal routed to this pin is determined by the contents of an internal register (see $\overline{\text{CSCNTRL}}$ data word description). The internally generated 2.5-V reference may be selected for use in biasing inputs A6 and A7.
V_{DD}	15		5-V (digital) supply
V_{CC}	27		10-V (analog) supply
$\overline{\text{WE}}$	6	I	Write Enable. This input is a write strobe for the control registers and the DAC input register. Data is latched on the rising edge of this signal.

PRINCIPLES OF OPERATION

writing control words to the TLC32071

With the $\overline{\text{CSCNTRL}}$ input low, a control word is written to the TLC32071 by placing data on the D7-D0 inputs and applying a low-going pulse to the write enable input ($\overline{\text{WE}}$). Data is latched on the rising edge of the $\overline{\text{WE}}$ pulse. The values of D0 and D1 of the control word determine whether the data is latched in the range/ADC MUX control register or the REF MUX register. See Tables 1, 2, 3, and 4 for data-bit formats.

operation of the ADC channel

Analog-to-digital conversion begins when gain-select and channel-select data word is latched in the range/ADC MUX control register by the rising edge of the $\overline{\text{WE}}$ pulse. This data word controls the state of the range/ADC input multiplexer. After the conversion time, the conversion result may be read by taking the $\overline{\text{DEN}}$ input low while the $\overline{\text{CSAN}}$ input is low. Writing of data to the REF MUX control register (using $\overline{\text{CSCNTRL}}$ and $\overline{\text{WE}}$ with D0 and D1 both 0) does not start a conversion. Each time one of the A0 through A5 signal channels is selected, the first conversion result after selection should be ignored due to internal input amplifier settling time. If this channel remains selected, subsequent conversions are valid.

operation of the DAC channel

When the $\overline{\text{CSAN}}$ input is low, digital-to-analog conversion is performed by placing input data on data bus DB7-DB0 and applying a low-going pulse to $\overline{\text{WE}}$. The data word is latched on the rising edge of the $\overline{\text{WE}}$ pulse and is decoded to an equivalent analog voltage. The conversion occurs internally in approximately 100 ns with the D/A conversion result available at the ANAOUT output after a specified settling time.

digital loopback mode

Digital loopback enables the simultaneous testing of the A/D and D/A channels. When digital loopback is enabled, the A/D conversion result is transferred to the D/A input latches on the next rising edge of $\overline{\text{DEN}}$. The analog signal from the input pin at the A/D converter is transferred through the D/A converter to the analog output ANAOUT. To enable digital loopback, write to the REF MUX control register (see data word format in Table 3) to set bit D6. Then, perform A/D conversion (as in normal operation) by writing channel select and range select information to the range/ADC MUX control register. This is done by strobing $\overline{\text{WE}}$ while $\overline{\text{CSCTRL}}$ is low. Read the conversion result by strobing $\overline{\text{DEN}}$ while holding $\overline{\text{CSAN}}$ low when digital loopback is enabled. The A/D conversion result is transferred to the DAC on the rising edge of $\overline{\text{DEN}}$ (See Tables 1, 2, 3, and 4).

reset operation

$\overline{\text{CSAN}}$ and $\overline{\text{CSCNTRL}}$ should be held high during a reset operation. When the $\overline{\text{RESET}}$ input is taken low, the internal reset signal clears the range/ADC MUX control register, the REF MUX control register, and the DAC input register. The following conditions exist after reset:

1. The DAC output is set to the voltage at the ANLG COM input.
2. The DAC range is set to ANLG COM ±4 V.
3. The A0 analog channel is selected and the A0 and A1 amplifier ranges are set to ANLG COM ±4 V.
4. The 2.5 V reference is selected at the REF output.
5. Digital loopback is disabled.

analog inputs

The ANLG COM voltage establishes the operating midpoint of the input amplifiers, A0 through A5. When the input signal voltage equals this voltage, the ADC output is ideally digital count zero. These amplifiers level shift to the ADC midpoint of 2.5 V and scale the input voltage range to the ADC range of 0.5 to 4.5 V. The A6 and A7 noninverting inputs are centered at the 2.5 V internally generated voltage reference and are connected directly to the input MUX. Table 5 gives the full scale input range and the midpoint voltages applicable for the individual analog inputs.

Table 1. Data Word Formats (Channel Range Selection)

D1	D0	A0/A1 CHANNEL PROGRAMMABLE GAIN	DATA DESTINATION	INPUT FULL SCALE RANGE (ANLG COM=5)	MIN	MAX
L	L	No range selection	Higher-order bits are sent to REF-MUX register			
L	H	Range is set to 1	Higher-order bits are sent to ADC channel-select register	ANLG COM ±4 V	1 V	9 V
H	L	Range is set to 1/2		ANLG COM ±2 V	3 V	7 V
H	H	Range is set to 1/4		ANLG COM ±1 V	4 V	6 V

Table 2. Data Word Formats (RANGE/ADC-Multiplexer Channel Selection)
(Data chosen from this table is only valid when data bits D1 and D0 are not both low)

SELECTED CHANNEL	D7	D6	D5	D4	D3	D2
A0	X	X	X	L	L	L
A1	X	X	X	L	L	H
A2	X	X	X	L	H	L
A3	X	X	X	L	H	H
A4	X	X	X	H	L	L
A5	X	X	X	H	L	H
A6	X	X	X	H	H	L
A7	X	X	X	H	H	H

Table 3. Data Word Formats (DAC Output Range Selection)
(Data chosen from this table is only valid when data bits D1 and D0 are not both low)

D6	D5	DAC OUTPUT RANGE	OUTPUT FULL SCALE RANGE (ANLG COM=5)	MIN	MAX
L	X	Range is set to 1	ANLG COM ±4 V	1 V	9 V
H	L	Range is set to 1/2	ANLG COM ±2 V	3 V	7 V
H	H	Range is set to 1/4	ANLG COM ±1 V	4 V	6 V

Table 4. Data Word Formats (REF-Multiplexer Channel Selection)
(Data chosen from this table is valid only when data bits D1 and D0 are both low)

SELECTED CHANNEL	D6	D5	D4	D3	D2
V_{ref} (2.5 V nom)	X	X	L	L	L
Bandgap (ACOM + 1.25 V)	X	X	L	L	H
A/D reference (approximately 4.6 V)	X	X	L	H	L
D/A reference (ANLG COM −3 V)	X	X	L	H	H
A0 amp output†	X	X	H	L	L
A1 amp output†	X	X	H	L	H
ADC MUX output†	X	X	H	H	L
DAC level shift output‡	X	X	H	H	H
Enable digital loopback	H	X	X	X	X

† These signals are outputs of scaling/level-shifting amplifiers. The range of these signals is V_{ref} ±2 V.

‡ The unscaled output of the DAC. This analog output is proportional to the DAC value with a fixed range of ANLG COM ±1 V, but inverted relative to the twos-complement code written to the DAC.

Table 5. Analog Input Characteristics

INPUT	V_{mid}†	NOMINAL FSR‡	INPUT VOLTAGE RANGE (ANLG COM=5)	
			MIN	MAX
A0, A1§ (1)	ANLG COM	±4 V	1 V	9 V
(1/2)	ANLG COM	±4 V	3 V	7 V
(1/4)	ANLG COM	±4 V	4 V	6 V
A2 thru A5§	ANLG COM	±4 V	1 V	9 V
A6, A7	V_{ref}¶	±2 V	0.5 V	4.5 V

† V_{mid} is (VP127-VM127)•127.5/254+VM127 where VP127 is the minimum input voltage to produce an output code of +127, and VM127 is the minimum input voltage to produce an output code of −127.

‡ Full-scale range is (VP127–VM127)•256/254 where VP127 is the minimum input voltage to produce an output code of +127, and VM127 is the minimum input voltage to produce an output code of −127.

§ Inverting inputs

¶ V_{ref} is an internally generated reference voltage that can be available at the REF output. The inputs A6 and A7 are connected to V_{ref} through an on-chip resistor.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (analog supply) (see Note 1) ..... −0.5 V to 14 V
Supply voltage range, V_{DD} (digital supply) (see Note 2) ..... −0.5 V to 7 V
Digital ground voltage range, DGTL GND ..... −0.5 V to 0.5 V
Analog output voltage range (see Note 1) ..... −0.5 V to V10 + 0.5 V
Analog input voltage range (see Note 1) ..... −0.5 V to 14 V
Digital output voltage range (see Note 2) ..... −0.5 V to V5 + 0.5 V
Digital input voltage range (see Note 2) ..... −0.5 V to V5 + 0.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 10 seconds: FN package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package ..... 260°C

NOTES: 1. All voltage values are given with respect to ANLG GND unless otherwise noted.
2. All voltage values are with respect to DGTL GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	9	10	12	V
Supply voltage, V_{DD}	4.5	5	5.5	V
High-level input voltage, V_{IH} (digital inputs)	2.4			V
Low-level input voltage, V_{IL} (digital inputs)			0.5	V
Reference voltage input at ANLG COM† input, V_{ref}	3.5	5	6	V
Setup time, $\overline{\text{CSCNTRL}}$ low before $\overline{\text{WE}}$ low, $t_{su(CS)}$	0			ns
Hold time, $\overline{\text{CSCNTRL}}$ high after $\overline{\text{WE}}$ high, $t_{h(CS)}$	0			ns
Setup time, data bus before $\overline{\text{CSCNTRL}}$ high, $t_{su(D)}$	15			ns
Hold time, data bus after $\overline{\text{CSCNTRL}}$ high, $t_{h(D)}$	15			ns
Pulse duration, $\overline{\text{DEN}}$, $t_{w(DEN)}$	t_a‡			ns
Setup time, $\overline{\text{CSAN}}$ low before $\overline{\text{DEN}}$ low, $t_{su(CS)}$	0			ns
Hold time, $\overline{\text{CSAN}}$ high after $\overline{\text{DEN}}$ high, $t_{h(CS)}$	0			ns
Setup time, $\overline{\text{CSAN}}$ low before $\overline{\text{WE}}$ low, $t_{su(CS)}$	0			ns
Hold time, $\overline{\text{CSAN}}$ high after $\overline{\text{WE}}$ high, $t_{h(CS)}$	0			ns
Pulse duration, $\overline{\text{RESET}}$, $t_{w(RE)}$	25			ns
Pulse duration, $\overline{\text{WE}}$, $t_{w(WE)}$	30			ns
Operating free-air temperature, T_A	0		70	°C

† For a DAC range of R = (1, 1/2, 1/4), ANLG COM should be chosen so that ANLG COM ±4R is greater than 0.5 V and less then V_{CC} −0.5 V or the DAC output may not be able to deliver the specified maximum current without voltage-limiting occurring.
‡ Access time

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_{OH}	High-level output voltage	V_{DD} at 4.5 V, I_{OH} = −360 µA	2.4			V
V_{OL}	Low-level output voltage	V_{DD} at 4.5 V, I_{OL} = 1.6 mA			0.4	V
V_{ref}	Reference voltage output (see Note 3)	ANLG COM = 5 V	2.42	2.5	2.58	V
$R_{O(ref)}$	Reference output resistance	ANLG COM = 5 V		0.8	1.2	kΩ
I_{IH}	High-level input current	V_{IH} = 5 V			10	µA
I_{IL}	Low-level input current	V_{IL} = 0			−10	µA
I_{DD}	Supply current, digital	D0-D7 at V_{IH} or V_{IL}			20	mA
I_{CC}	Supply current, analog				22	mA
I_{OZ}	Off-state output current (high-impedance state)	V_O = 5 V			3	µA
		V_O = 0			−3	
I_{OS}	Short-circuit output current	V_O = 5 V	25	40		mA
		V_O = 0	−45	−60		
C_o	Output capacitance (digital outputs)				5	pF

§ All typical values are at T_A = 25°C.
NOTE 3: This voltage is an internal reference voltage (2.5 V) that is available at the output-multiplexer output.

ADC operating characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
	Linearity error				±1	LSB
$V_{I(FS)}$†	Input voltage for full-scale output code (Input channel = A6 or A7)			3.92	4.08	V
V_{mid}‡	ADC input offset voltage (Input channel = A6 or A7)			$V_{ref}-0.06$	$V_{ref}+0.06$	V
t_{conv}	Conversion time	See Figure 2			2.5	µs
t_a	Access time (delay from falling edge of $\overline{DEN}$ to data output)	See Figure 3	C_L = 100 pF§		50	ns
			C_L = 50 pF§		41	
			C_L = 25 pF§		37	
t_{dis}	Disable time (delay from rising edge of $\overline{DEN}$ to high-impedance state of data output)	See Figure 3	C_L = 100 pF		35	ns

† Full-scale range is (VP127–VM127) • 256/254 where VP127 is the minimum input voltage to produce an output code of +127, and VM127 is the minimum input voltage to produce an output code of –127.

‡ V_{mid} is (VP127–VM127) • 127.5/254 + VM127 where VP127 is the minimum input voltage to produce an output code of +127, and VM127 is the minimum input voltage to produce an output code of –127.

§ C_L is in addition to the internal capacitance of the digital output.

DAC operating characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP¶	MAX	UNIT
t_s	Settling time (to 1 LSB)	Load on ANAOUT = 20 pF + 5 kΩ (to ANLG COM)			8	15	µs
E_L	Linearity error					±1	LSB
	Code width			0.25		1.75	LSB
$V_{O(FS)}$	Output voltage swing#, full scale (VP127–VM128) • 256/255	DAC input = –128 to +127	Range = 1	7.84	8	8.16	V
			Range = 1/2	3.92	4	4.08	
			Range = 1/4	1.96	2	2.04	
	Output bias level#, full scale (VP127–VM128) • 128/255+VM128	DAC input = 0	Range = 1	ANLG COM–0.08		ANLG COM+0.08	V
			Range = 1/2	ANLG COM–0.06		ANLG COM+0.06	
			Range = 1/4	ANLG COM–0.05		ANLG COM+0.05	
	Glitch energy	Sample rate = 30 kHz				1.2	mV
I_{OM}	Maximum output current, ANAOUT	Source from V_{CC}–0.5 V or sink from 0.5 V		1.2			mA

¶ Typical values are at T_A = 25°C.

VP127 is the voltage output for an input code of +127. VM128 is the voltage output for an input code of –128.

ADC electrical characteristics for inputs A0 and A1 over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
A_V1	Voltage amplification	Range = 1		0.99	1	1.01	V/V
A_V2	Voltage amplification	Range = 1/2		1.98	2	2.02	V/V
A_V4	Voltage amplification	Range = 1/4		3.96	4	4.04	V/V
$V_{OB}1$	Output bias voltage at input of ADC with respect to V_{ref}	$V_I = V_{(ANLG\ COM)}$,	Range = 1		0	±0.02	V
$V_{OB}2$	Output bias voltage at input of ADC with respect to V_{ref}	$V_I = V_{(ANLG\ COM)}$,	Range = 1/2		0	±0.03	V
$V_{OB}4$	Output bias voltage at input of ADC with respect to V_{ref}	$V_I = V_{(ANLG\ COM)}$,	Range = 1/4		0	±0.05	V
r_i	Input resistance			140	200	260	kΩ

ADC electrical characteristics for inputs A2, A3, A4 and A5 over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
A_V	Voltage amplification to ADC		−0.495	−0.5	−0.505	V/V
V_{OB}	Output bias voltage at the input of the ADC with respect to V_{ref}	$V_I = V_{(ANLG\ COM)}$	−0.02	0	+0.02	V
r_i	Input resistance		140	200	260	kΩ

ADC electrical characteristics for inputs A6 and A7 (direct inputs) over recommended free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
A_V	Voltage amplification to ADC			1		V/V
r_i	Input resistance (to REF)		70	100	130	kΩ

PARAMETER MEASUREMENT INFORMATION

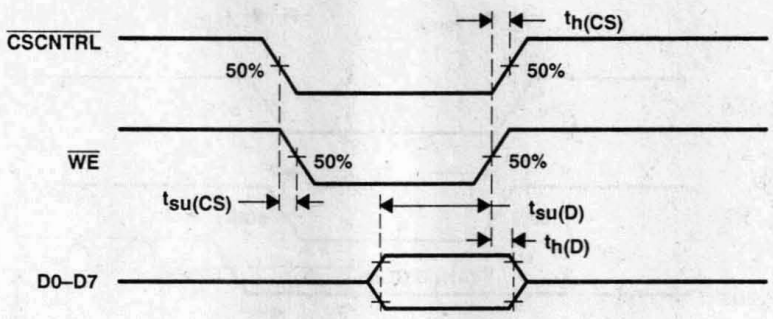


Figure 1. Write Operation

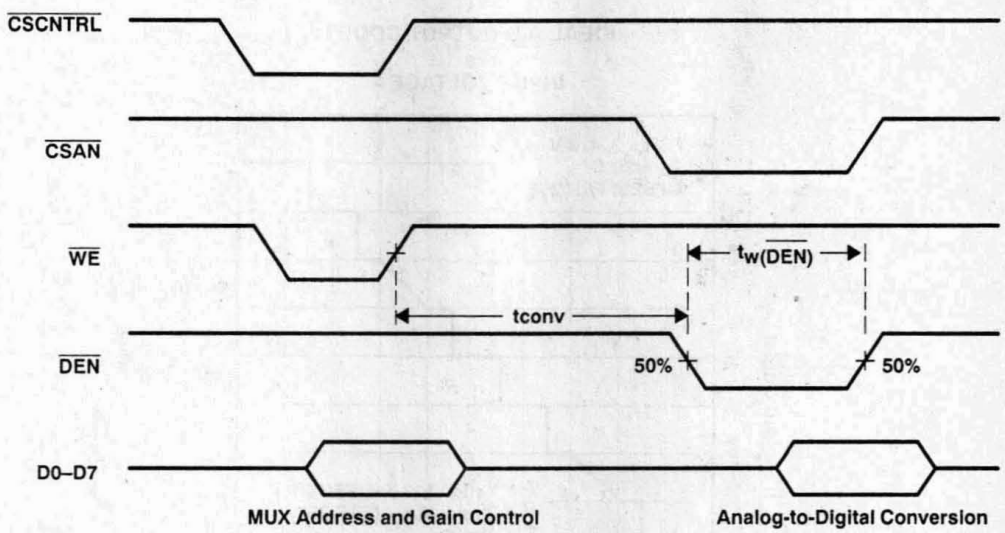


Figure 2. A/D Conversion Cycle

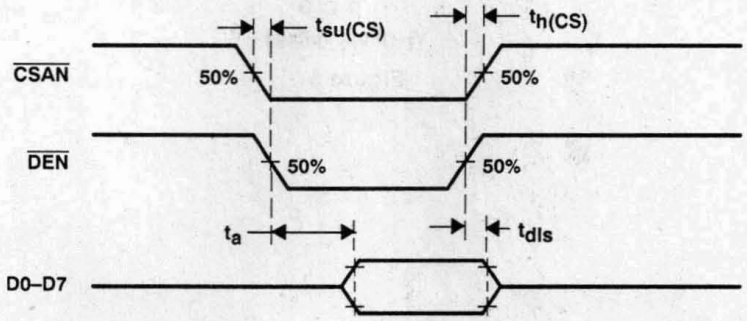


Figure 3. A/D Read Operation

PARAMETER MEASUREMENT INFORMATION

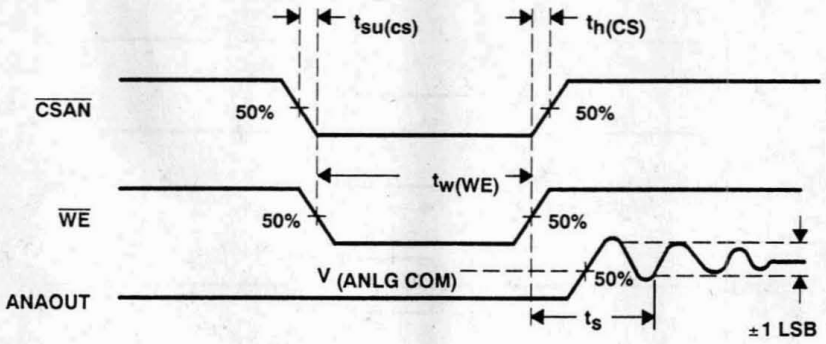


Figure 4. D/A Conversion Operation

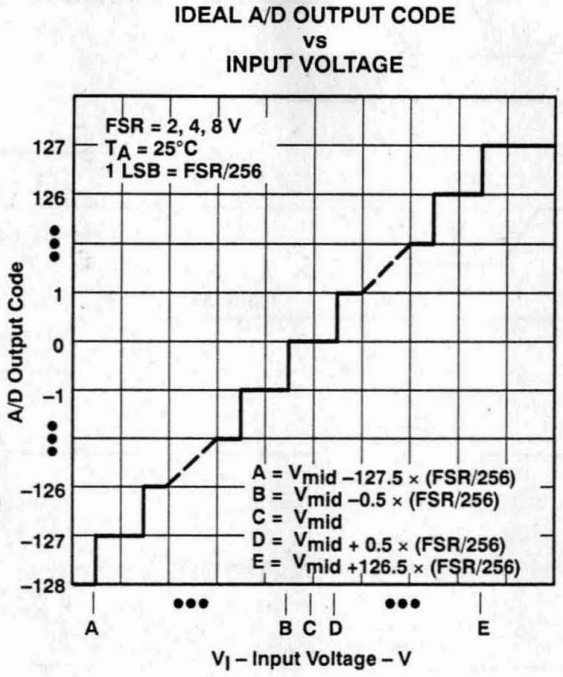


Figure 5

PARAMETER MEASUREMENT INFORMATION

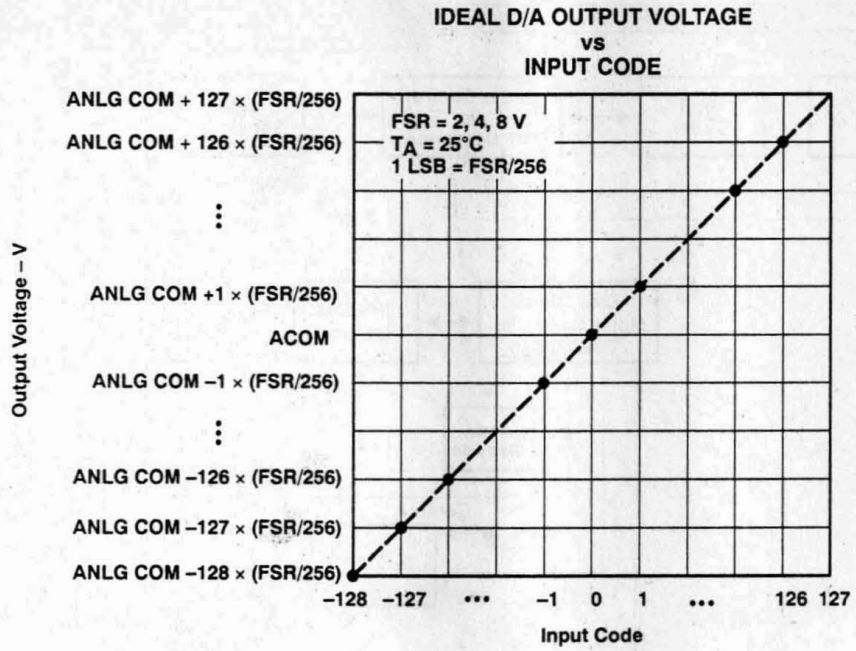


Figure 6

APPLICATION INFORMATION

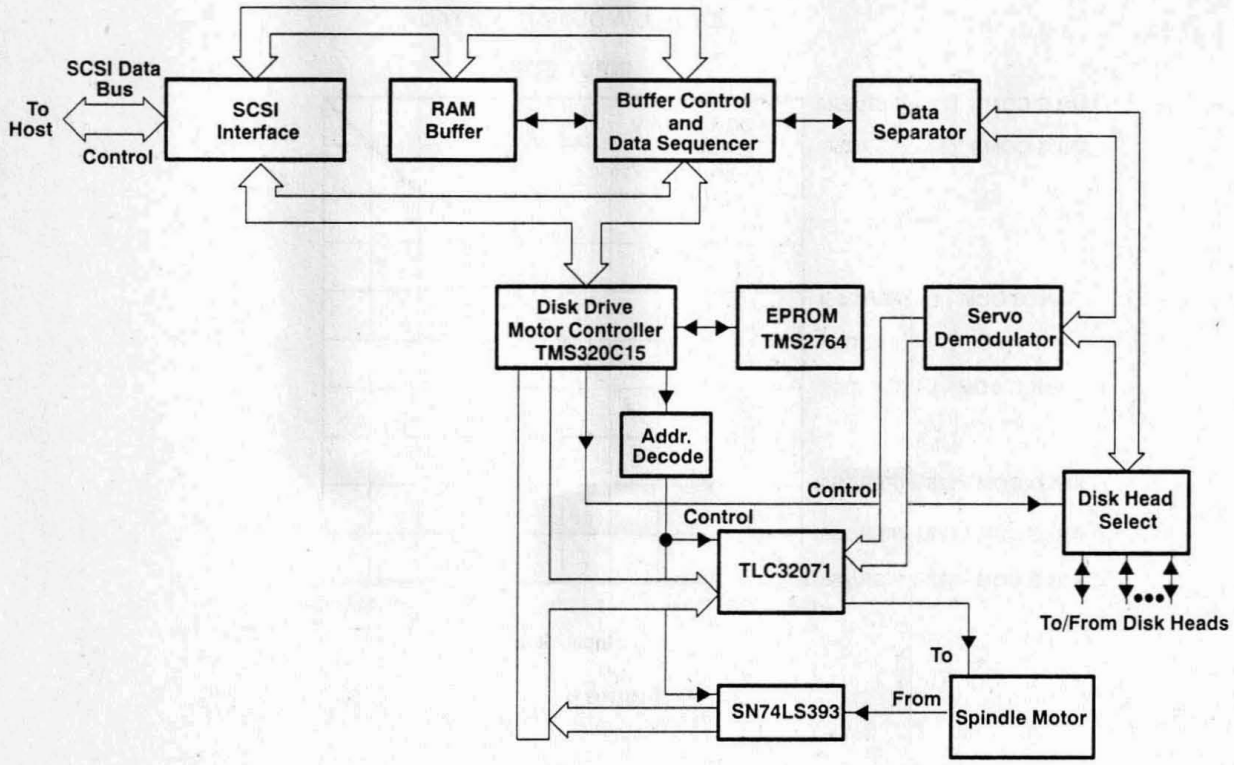


Figure 7. Simplified Disk-Drive Controller

General Information 1
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DSP Analog Interface and Conversion 5
Video Interface Palettes 6
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Mechanical Data 11

D3961, NOVEMBER 1991

- LinEPIC™ 1-μm CMOS Process
- 125-MHz Pipelined Architecture
- Available Clock Rates . . . 80, 110, 125, 135 MHz
- Dual-Port Color RAM 256 Words x 24 Bits
- Bit Plane Read and Blink Masks
- EIA RS-343-A Compatible Outputs
- Functionally Interchangeable With Brooktree® Bt458
- Direct Interface to TMS340XX Graphics Processors
- Standard Microprocessor Unit (MPU) Palette Interface
- Multiplexed TTL Pixel Ports
- Triple Digital-to-Analog Converters (DACs)
- Dual-Port Overlay Registers . . . 4 x 24 Bits
- 5-V Power Supply

description

The TLC34058 color-palette integrated circuit is specifically developed for high-resolution color graphics in such applications as CAE/CAD/CAM, image processing, and video reconstruction.

The architecture provides for the display of 1280 × 1024 bit-mapped color graphics (up to 8 bits per pixel resolution) with 2 bits of overlay information. The TLC34058 has a 256-word × 24-bit RAM used as a lookup table with three 8-bit video D/A converters.

On-chip features such as high-speed pixel clock logic minimize costly ECL interface. Multiple pixel ports and internal multiplexing provide TTL-compatible interface (up to 32 MHz) to the frame buffer while maintaining sophisticated color graphic data rates (up to 135 MHz). Programmable blink rates, bit plane masking and blinking, color overlay capability, and a dual-port palette RAM are other key features. The TLC34058 generates red, green, and blue signals compatible with EIA RS-343-A and can drive, without external buffering, 75-Ω coaxial cables terminated at each end.

AVAILABLE OPTIONS

T_A	SPEED	DAC RESOLUTION	PACKAGE	
			84-Pin Ceramic Grid Array	84-Pin Chip Carrier
0°C to 70°C	80 MHz	8 Bits	TLC34058-80GA	TLC34058-80FN
	110 MHz	8 Bits	TLC34058-110GA	TLC34058-110FN
	125 MHz	8 Bits	TLC34058-125GA	TLC34058-125FN
	135 MHz	8 Bits	TLC34058-135GA	TLC34058-135FN

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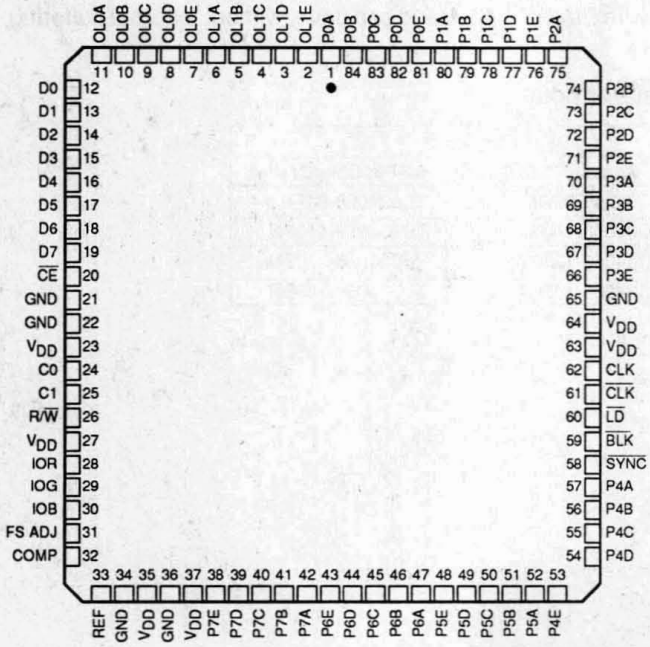
84-PIN GA PACKAGE (TOP VIEW)

	A	B	D	E	F	G	H	J	K	L	M
12	COMP	GND	V_{DD}	P7D	P7B	P6E	P6C	P6B	P5E	P5C	P5B	P4E
11	IOB	GND	V_{DD}	P7E	P7C	P7A	P6D	P6A	P5D	P5A	P4C	P4A
10	IOG	FS ADJ	REF							P4D	P4B	$\overline{SYNC}$
9	V_{DD}	IOR									$\overline{BLK}$	$\overline{LD}$
8	C1	R/$\overline{W}$									$\overline{CLK}$	CLK
7	V_{DD}	C0									V_{DD}	V_{DD}
6	GND	GND									P3E	GND
5	$\overline{CE}$	D7									P3C	P3D
4	D6	D5	D0	• (ESD SYMBOL OR ALIGNMENT DOT - ON TOP)							P3A	P3B
3	D4	D2	OL0B							P2A	P2C	P2E
2	D3	D1	OL0D	OL0E	OL1B	OL1E	P0B	P0D	P1A	P1D	P1E	P2D
1	OL0A	OL0C	C	OL1A	OL1C	OL1D	P0A	P0C	P0E	P1B	P1C	P2B

84-PIN GA PACKAGE (BOTTOM VIEW)

	M	L	K	J	H	G	F	E	D	C	B	A
12	P4E	P5B	P5C	P5E	P6B	P6C	P5E	P7B	P7D	V_{DD}	GND	COMP
11	P4A	P4C	P5A	P5D	P6A	P6D	P7A	P7C	P7E	V_{DD}	GND	IOB
10	$\overline{SYNC}$	P4B	P4D							REF	FS ADJ	IOG
9	$\overline{LD}$	$\overline{BLK}$									IOR	V_{DD}
8	CLK	$\overline{CLK}$									R/$\overline{W}$	C1
7	V_{DD}	V_{DD}									C0	V_{DD}
6	GND	P3E									GND	GND
5	P3D	P3C									D7	$\overline{CE}$
4	P3B	P3A	(ESD SYMBOL OR ALIGNMENT DOT - ON TOP) •								D5	D6
3	P2E	P2C	P2A							D0	D2	D4
2	P2D	P1E	P1D	P1A	P0D	P0B	OL1E	OL1B	OL0E	OL0B	D1	D3
1	P2B	P1C	P1B	P0E	P0C	P0A	OL1D	OL1C	OL1A	OL0D	OL0C	OL0A

FN PACKAGE
(TOP VIEW)



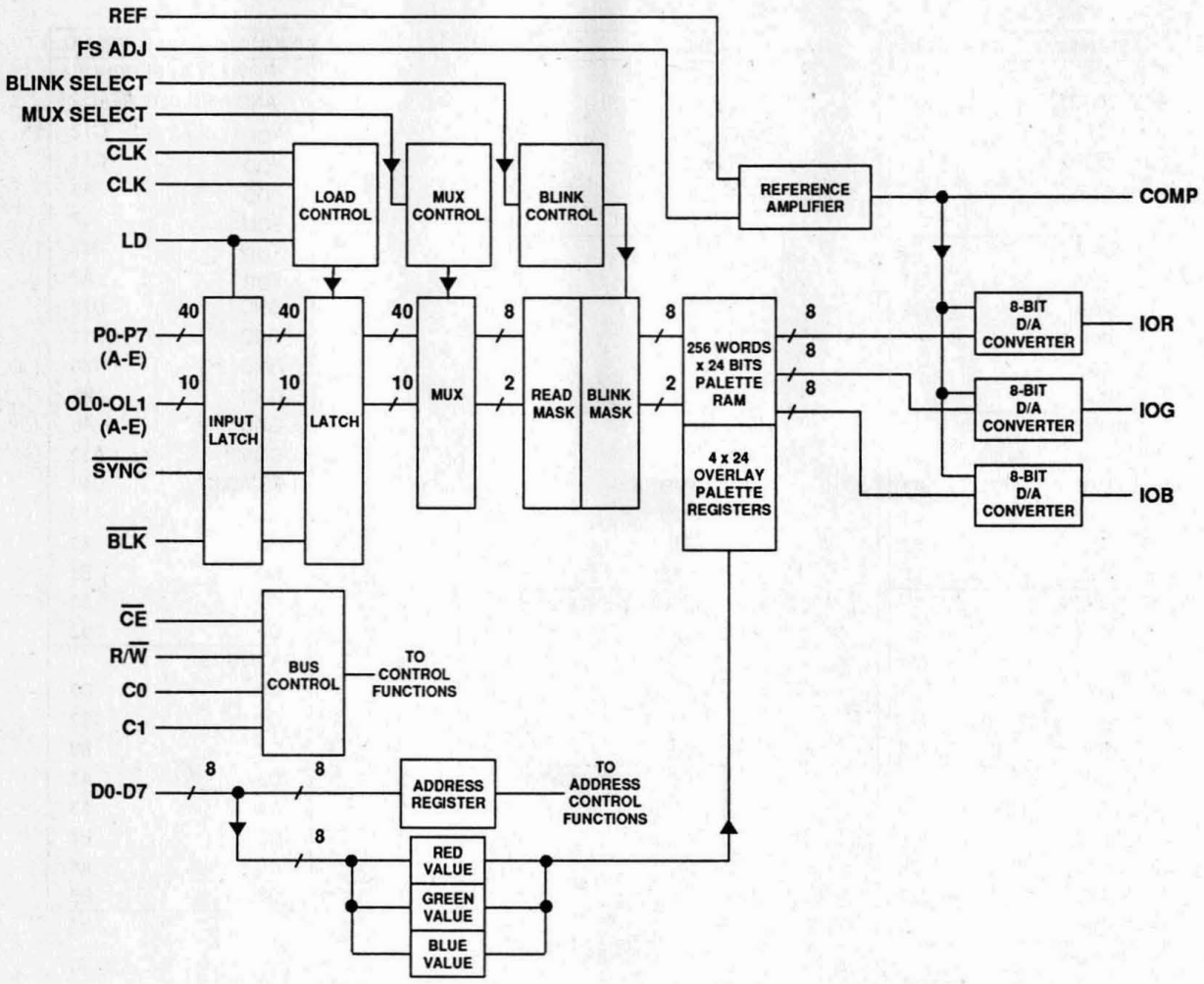
84-pin GA package pin assignments

SIGNAL	PIN NO.
$\overline{BLK}$	L9
$\overline{SYNC}$	M10
$\overline{LD}$	M9
$\overline{CLK}$	L8
CLK	M8
PORT 0	
P0A	G1
P0B	G2
P0C	H1
P0D	H2
P0E	J
PORT 1	
P1A	J2
P1B	K1
P1C	L1
P1D	K2
P1E	L2
PORT 2	
P2A	K3
P2B	M1
P2C	L3
P2D	M2
P2E	M3
PORT 3	
P3A	L4
P3B	M4
P3C	L5
P3D	M5
P2E	L6
PORT 4	
P4A	M11
P4B	L10
P4C	L11
P4D	K10
P4E	M12

SIGNAL	PIN NO.
PORT 5	
P5A	K11
P5B	L12
P5C	K12
P5D	J11
P5E	J12
PORT 6	
P6A	H11
P6B	H12
P6C	G12
P6D	G11
P6E	F12
PORT 7	
P7A	F11
P7B	E12
P7C	E11
P7D	D12
P7E	D11
OVERLAY SELECT 0	
OL0A	A1
OL0B	C2
OL0C	B1
OL0D	C1
OL0E	D2
OVERLAY SELECT 1	
OL1A	D1
OL1B	E2
OL1C	E1
OL1D	F1
OL1E	F2
DAC CURRENT OUTPUTS	
IOG	A10
IOB	A11
IOR	B9

SIGNAL	PIN NO.
POWER, REFERENCE AND MPU INTERFACE	
V_{DD}	C12
V_{DD}	C11
V_{DD}	A9
V_{DD}	L7
V_{DD}	M7
V_{DD}	A7
GND	B12
GND	B11
GND	M6
GND	B6
GND	A6
COMP	A12
FS ADJ	B10
REF	C10
$\overline{CE}$	A5
$R/\overline{W}$	B8
C1	A8
C0	B7
DATA BUS	
D0	C3
D1	B2
D2	B3
D3	A2
D4	A3
D5	B4
D6	A4
D7	B5

functional block diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Terminal Functions

PIN NAME	I/O	DESCRIPTION
$\overline{BLK}$	I	Composite blank control. This TTL-compatible blanking input is stored in the input latch on the rising edge of $\overline{LD}$. When low, $\overline{BLK}$ drives the DAC outputs to the blanking level, as shown in Table 6. This causes the P0-P7 [A-E] and OL0-OL1 [A-E] inputs to be ignored. When high, $\overline{BLK}$ allows the device to perform in the standard manner.
$\overline{SYNC}$	I	Composite sync control. This TTL-compatible sync control input is stored in the input latch on the rising edge of $\overline{LD}$. When low, $\overline{SYNC}$ turns off a 40 IRE current source on the IOG output, as shown in Figure 3. This input does not override any control data input, as shown in Table 6. It should be brought low during the blanking interval only, as shown in Figure 3. When high, $\overline{SYNC}$ allows the device to perform in the standard manner.
$\overline{LD}$	I	Load control. This TTL-compatible load control input latches the P0-P7 [A-E], OL0-OL1 [A-E], $\overline{BLK}$, and $\overline{SYNC}$ inputs on its rising edge. The $\overline{LD}$ strobe occurs at 1/4 or 1/5 the clock rate and may be phase independent of the CLK and $\overline{CLK}$ inputs. The $\overline{LD}$ duty cycle limits are specified in the timing requirements table.
P0A-P7A P0B-P7B P0C-P7C P0D-P7D P0E-P7E	I	Address inputs. These TTL-compatible address inputs for the Palette RAM are stored in the input latch on the rising edge of $\overline{LD}$. These address inputs (up to 8-bits per pixel) select one of 256 24-bit words in the palette RAM, which is subsequently input to the red, green, and blue D/A converters as three 8-bit or 4-bit bytes. Four or five addresses are simultaneously input to the P0-P7 [A-D] or P0-P7 [A-E] ports, respectively (see the description of bit CR7 in the command register section). The word addressed by P0A-P7A is first sent to the DACs, then the word addressed by P0B-P7B, and so on. Unused inputs should be connected to GND.
OL0A-AL1A OL0B-OL1B OL0C-OL1C OL0D-OL1D OL0E-OL1E	I	Overlay selection inputs. These TTL-compatible selection inputs for the Palette overlay registers are stored in the input latch on the rising edge of $\overline{LD}$. These inputs (up to 2 bits per pixel), along with bit CR6 of the command register (refer to the command register section and Table 5), specify whether the color information is selected from the palette RAM or the overlay registers. If the color information is selected from the overlay registers, the OL0-OL1 [A-E] inputs address a particular overlay register. The OL0-OL1 [A-D] or OL0-OL1 [A-E] inputs are simultaneously input to the device (see the description of bit CR7 in the command register section). The OL0-OL1 [A-E] inputs are simultaneously input to the device (see the description of bit CR7 in the command register section). The OL0-OL1 [A] inputs are processed first, then the OL0-OL1 [B] inputs, and so on. When obtaining the color information from the overlay registers, the P0-P7 [A-E] inputs are ignored. Unused inputs should be connected to GND.
IOR, IOG, IOB	O	Current outputs, red, green, and blue. High-impedance red, green, and blue video analog current outputs can directly drive a 75-Ω coaxial terminated at each end (see Figure 4).
V_{DD}		Supply voltage. All V_{DD} pins must be connected together.
GND		Ground. All GND pins must be connected together.
COMP	I	Compensation. This input is used to compensate the internal reference amplifier (see the video generation section). A 0.1-μF ceramic capacitor is connected between this pin and V_{DD} (see Figure 4). The highest possible supply voltage rejection ratio is attained by connecting the capacitor to V_{DD} rather than to GND.
FS ADJ	I	Full-scale adjust control. A resistor R_{set}, (see Figure 4) which is connected between this pin and GND, controls the magnitude of the full-scale video signal. Note that the proportional current and voltage relationships in Figure 3 are maintained independent of the full-scale output current. The relationships between R_{set} and the IOR, IOG, and IOB full-scale output currents are: R_{set} (Ω) = 11294 × V_{ref} (V) / IOG (mA) IOR, IOB (mA) = 8067 × V_{ref} (V) / R_{set} (Ω)
REF	I	Reference voltage. 1.235-V is supplied at this input. An external voltage reference circuit, shown in Figure 4, is suggested. Generating the reference voltage with a resistor network is not recommended since low-frequency power supply noise will directly couple into the DAC output signals. This input must be decoupled by connecting a 0.1-μF ceramic capacitor between VREF and GND.
CLK	I	Clock. This input provides the pixel clock rate. CLK and $\overline{CLK}$ inputs are designed to be driven by ECL logic using a 5-V single supply.
$\overline{CLK}$	I	Clock. This input is the complement of CLK and also provides the pixel clock rate.

Terminal Functions (continued)

PIN NAME	I/O	DESCRIPTION
$\overline{CE}$	I	Chip enable. This TTL-compatible input control allows data to be stored and enables data to be written or read (see Figure 1). When low, $\overline{CE}$ enables data to be written or read. When high, $\overline{CE}$ allows data to be internally latched on the rising edge during write operations. Care should be taken to avoid transients on this input.
R/$\overline{W}$	I	Read/write input. This TTL-compatible control input is latched on the falling edge of $\overline{CE}$ (see Figure 1). When low, writes data to the device. Data is internally latched on the rising edge of $\overline{CE}$. When high, reads data from the device.
C0, C1	I	Command control inputs. The inputs specify the type of write or read operation (see Tables 1, 2, 3, and 4). These TTL-compatible inputs are latched on the falling edge of $\overline{CE}$.
D0-D7	I	Data input bus. This TTL-compatible bus transfers data into or out of the device. The data bus is an 8-bit bidirectional bus where D0 is the least significant bit.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 7 V
Voltage range on any digital input (see Note 1) ..... – 0.5 V to V_{DD} + 0.5 V
Analog output short circuit duration to any power supply or common, I_{OS} ..... unlimited
Operating free-air temperature, T_A ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C
Case temperature for 10 seconds: FN package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: GA package ..... 260°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.75	5	5.25	V
High-level input voltage, V_{IH}	CLK, $\overline{CLK}$	V_{DD} –1		V_{DD} + 0.5	V
	Other inputs	2		V_{DD} + 0.5	V
Low-level input voltage, V_{IL}	CLK, $\overline{CLK}$	– 0.5		V_{DD} –1.6	V
	Other inputs	– 0.5		0.8	V
Reference voltage, V_{ref}		1.2	1.235	1.26	V
Output load resistance, R_L			37.5		Ω
FS ADJ resistor, R_{set}			523		Ω
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature, R_{set} = 523 Ω, V_{ref} = 1.235 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{ref}	Input reference current					10		µA
k_{SVR}	Supply voltage rejection ratio		f = 1 kHZ, C8 = 0.1 µF (see Figure 4)			0.5		$\frac{\%}{\%\Delta V_{DD}}$
I_{DD}	Supply current	80 MHz	V_{DD} = 5 V,	T_A = 20°C		175		mA
			V_{DD} = 5.25 V,	T_A = 0°C			400	
		110 MHz	V_{DD} = 5 V,	T_A = 20°C		195		
			V_{DD} = 5.25 V,	T_A = 0°C			420	
		125 MHz	V_{DD} = 5 V,	T_A = 20°C		205		
			V_{DD} = 5.25 V,	T_A = 0°C			435	
		135 MHz	V_{DD} = 5 V,	T_A = 20°C		200		
			V_{DD} = 5.25 V,	T_A = 0°C			435	
I_{IH}	High-level input current	CLK, $\overline{CLK}$	V_I = 4 V				1	µA
		Other inputs	V_I = 2.4 V				1	µA
I_{IL}	Low-level input current	CLK, $\overline{CLK}$	V_I = 0.4 V				–1	µA
		Other inputs	V_I = 0.4 V				–1	µA
C_i	Input capacitance, digital		f = 1 MHz,	V_I = 2.4V		4	10	pF
$C_{i(CLK)}$	Input capacitance, CLK, $\overline{CLK}$		f = 1 MHz,	V_I = 4 V		4	10	pF
V_{OH}	High-level output voltage, D0-D7		I_{OH} = – 800 µA		2.4			V
V_{OL}	Low-level output voltage, D0-D7		I_{OL} = 6.4 mA				0.4	V
I_{OZ}	High-impedance-state output current						10	µA
z_o	Output impedance					50		kΩ
C_o	Output capacitance (f = 1 MHz, I_O = 0)					13	20	pF

†All typical values are at T_A = 25°C.

timing requirements over recommended ranges of supply voltage and operating free-air temperature, R_{set} = 523 Ω, V_{ref} = 1.235 V (see Note 2)

PARAMETER	REFERENCE	LIMIT	VERSION				UNITS
			135 MHz	125 MHz	110 MHz	80 MHz	
Clock frequency	–	MAX	135	125	110	80	MHz
$\overline{LD}$ frequency	–	MAX	33.75	31.25	27.5	20	MHz
Setup time, R/$\overline{W}$, C0, C1 high before $\overline{CE}$ ↓	1	MIN	0	0	0	0	ns
Hold time, R/$\overline{W}$, C0, C1 high after $\overline{CE}$ ↓	2	MIN	15	15	15	15	ns
Pulse duration, $\overline{CE}$ low	3	MIN	50	50	50	50	ns
Pulse duration, $\overline{CE}$ high	4	MIN	25	25	25	25	ns
Setup time, write data before $\overline{CE}$ ↑	8	MIN	35	35	35	50	ns
Hold time, write data after $\overline{CE}$ ↓	9	MIN	0	0	0	0	ns
Pixel and control setup time	10	MIN	3	3	3	4	ns
Pixel and control hold time	11	MIN	2	2	2	2	ns
Clock cycle time	12	MIN	7.4	8	9.09	12.5	ns
Pulse duration, CLK high	13	MIN	3	3.2	4	5	ns
Pulse duration, CLK low	14	MIN	3	3.2	4	5	ns
$\overline{LD}$ cycle time	15	MIN	29.6	32	36.36	50	ns
$\overline{LD}$ pulse duration high time	16	MIN	12	13	15	20	ns
$\overline{LD}$ pulse duration low time	17	MIN	12	13	15	20	ns

NOTE 2. TTL input signals are 0 to 3 V with less than 3 ns rise/fall times between 10% and 90% levels. ECL input signals are V_{DD} –1.8 V to VDD – 0.8 V with less than 2 ns rise/fall times between 20% and 80% levels. For input and output signals, timing reference points are at the 50% signal level. Analog output loads are less than 10 pF. D0-D7 output loads are less than 40 pF.

operating characteristics over recommended ranges of supply voltage and operating free-air temperature, R_{set} = 523 Ω, V_{ref} = 1.235 V (unless otherwise noted).

analog outputs

PARAMETER			MIN	TYP†	MAX	UNIT
E_L	Integral linearity error (each DAC)				±1	LSB
E_D	Differential linearity error				±1	LSB
	Gray scale error				±5	
I_O	Output current	White level relative to blank	17.69	19.05	20.4	mA
		White level relative to black	16.74	17.62	18.5	
		Black level relative to blank	0.95	1.44	1.9	
		Blank level on IOR, IOB	0	5	50	µA
		Blank level on IOG	6.29	7.6	8.96	mA
		Sync level on IOG	0	5	50	µA
	LSB size			69.1		µA
	DAC to DAC matching			2%	5%	
	Output compliance voltage		–1		1.2	V

†All typical values are at T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, R_{set} = 523 Ω, V_{ref} = 1.235 V (see Note 2)

PARAMETER	REFERENCE	LIMIT	VERSION				UNITS
			135 MHz	125 MHz	110 MHz	80 MHz	
$\overline{CE}$ low to data bus enabled	5	MIN	10	10	10	10	ns
$\overline{CE}$ low to data valid	6	MAX	75	75	75	100	ns
$\overline{CE}$ high to data bus disabled	7	MAX	15	15	15	15	ns
Analog otuput delay time (see Note 3)	18	TYP	20	20	20	20	ns
Analog output rise or fall time (see Note 4)	19	TYP	2	2	2	3	ns
Analog output settling time (see Note 5)	20	MAX	8	8	9	12	ns
Glitch impulse (see Note 6)		TYP	50	50	50	50	pV-s
Analog output skew		TYP	0	0	0	0	ns
		MAX	2	2	2	2	ns
Pipeline delay		MIN	6	6	6	6	clock
		MAX	10	10	10	10	cycles

NOTES: 2. TTL input signals are 0 to 3 V with less than 3 ns rise/fall times between 10% and 90% levels. ECL input signals are V_{DD} –1.8 to VDD – 0.8 V with less than 2 ns rise/fall times between 20% and 80% levels. For input and output signals, timing reference points are at the 50% signal level. Analog output loads are less than 10 pF. D0-D7 output loads are less than 40 pF.

3. Measured from 50% point of rising clock edge to 50% point of full-scale transition.
4. Measured between 10% and 90% of full-scale transition.
5. Measured from 50% point of full-scale transition to output settling within ± 1 LSB. Settling time does not include clock and data feedthrough.
6. Glitch impulse includes clock and data feedthrough. The – 3-dB test bandwidth is twice the clock rate.

PARAMETER MEASUREMENT INFORMATION

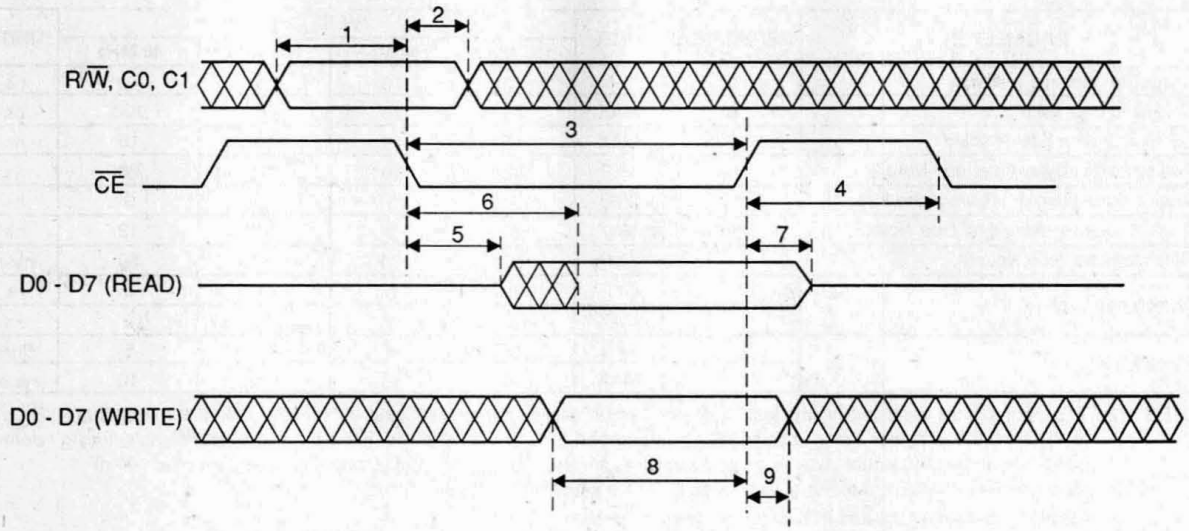


Figure 1. Read/Write Timing Waveform

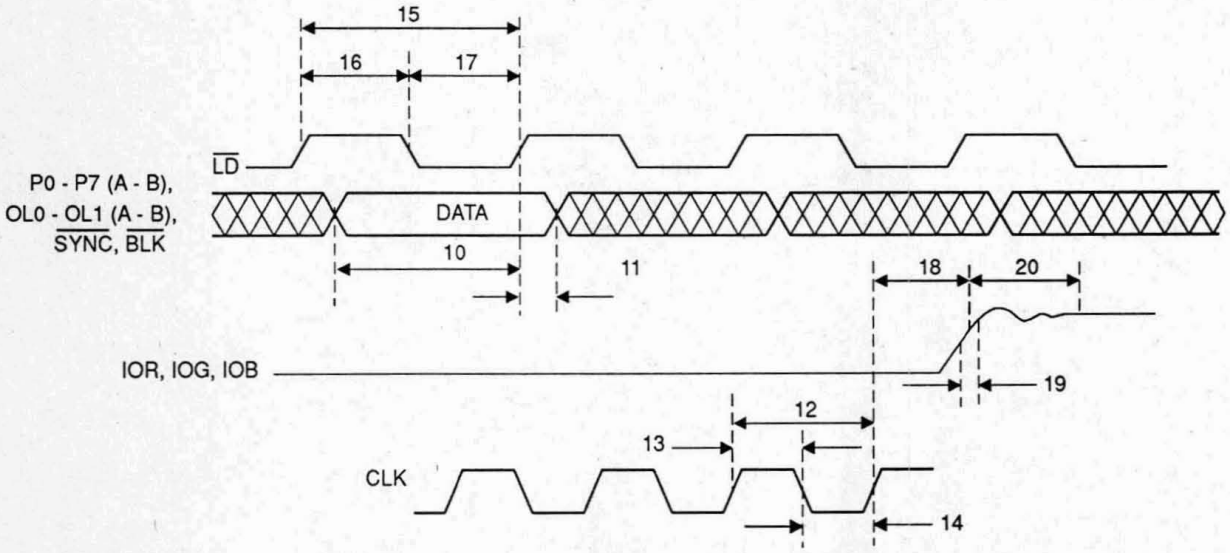
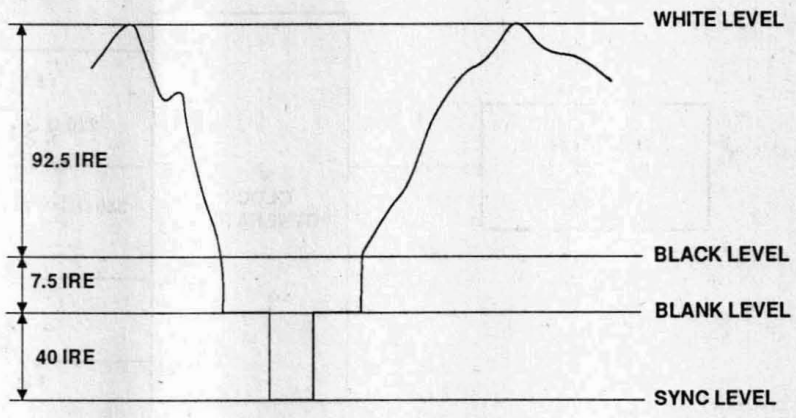


Figure 2. Video Input/Output Timing Waveform

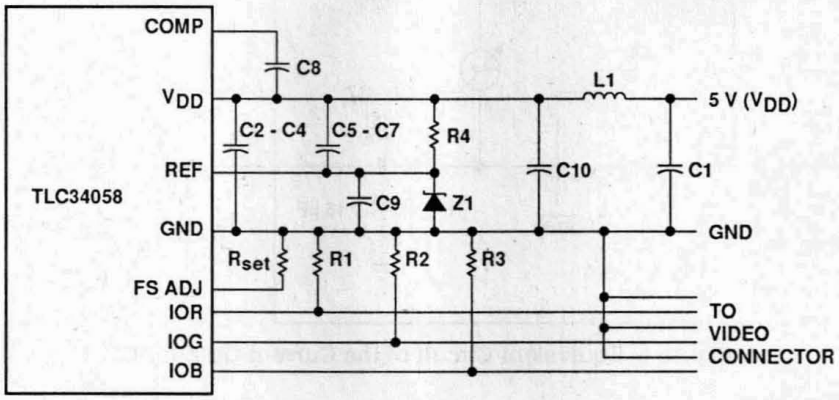
PARAMETER MEASUREMENT INFORMATION

RED, BLUE		GREEN	
mA	V	mA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



NOTE A: The IRE (Institute of Radio Engineers — now IEEE) scale is used for defining the relative voltage levels of the sync, white, black, and blank levels in a monitor circuit. The reference white level is set at 100 IRE units. The blanking level is set at ø IRE units. One IRE unit is equivalent to 1/100 of the difference between the reference white level and the blanking level.

Figure 3. Composite Video Output Waveforms



Location	Description	Vendor Part Number
C1 - C4, C8,C9	0.1-µF ceramic capacitor	Erie RPE112Z5U104M50V
C5 - C7	0.01-µF ceramic chip capacitor	AVX 12102T903QA1018
C10	33-µF tantalum capacitor	Mallory CSR13-K336KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75-Ω 1% metal film resistor	Dale CMF-55C
R4	1000-Ω 1% metal film resistor	Dale CMF-55C
R_{set}	523-Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2-V diode	National Semiconductor LM385Z-1.2

NOTE A: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not degrade the performance of the TLC34058.

Figure 4. Circuit Diagram

PARAMETER MEASUREMENT INFORMATION

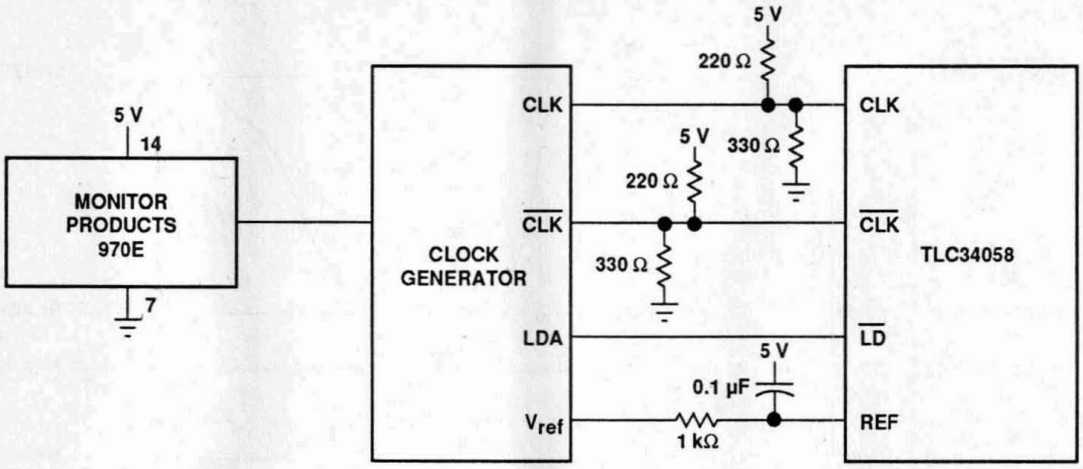


Figure 5. Generating the Clock, Load, and Voltage Reference Signals

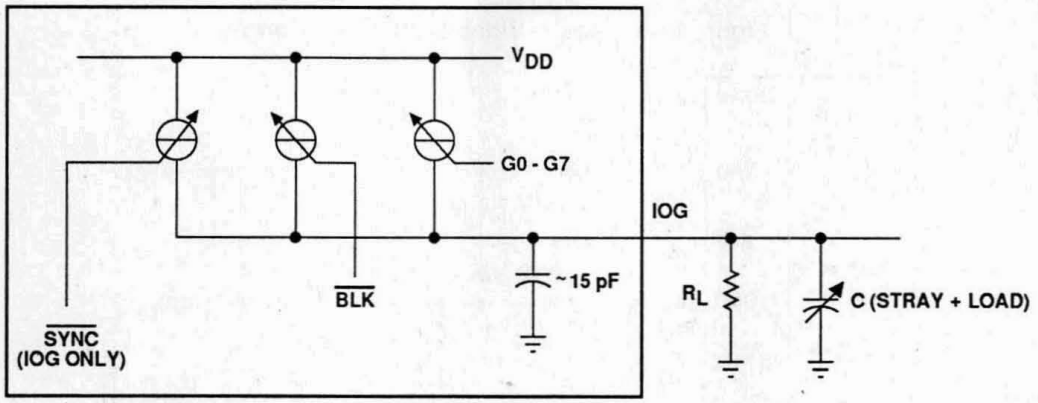


Figure 6. Equivalent Circuit of the Current Output (IOG)

APPLICATION INFORMATION

device ground plane

Use of a four-layer PC board is recommended. All of the ground pins, voltage reference circuitry, power supply bypass circuitry, analog output signals, and digital signals, as well as any output amplifiers, should have a common ground plane.

device analog power plane (APP)

The device plus associated analog circuitry should have a separate analog power plane (APP) for V_{DD}. The APP powers the device, voltage reference circuitry, and any output amplifiers. It should be connected to the overall PCB power plane (V_{DD}) at a single point through a ferrite bead, which should be within 3 inches of the device. This connection is shown in Figure 4.

PCB power plane and PCB ground plane

The PCB power plane powers the digital circuitry. The PCB power plane and PCB ground planes should not overlay the APP unless the plane-to-plane noise is common-mode.

supply decoupling

Bypass capacitors should have the shortest possible lead lengths to reduce lead inductance. For best results, a parallel combination of 0.1-µF ceramic and 0.01-µF chip capacitors should be connected from each V_{DD} pin to GND. If chip capacitors are not feasible, radial-lead ceramic capacitors may be substituted. These capacitors should be located as close to the device as possible.

The performance of the internal power supply noise rejection circuitry decreases with noise frequency. If a switching power supply is used for V_{DD}, close attention must be paid to reducing power supply noise. To reduce such noise, the APP could be powered with a three-terminal voltage regulator.

digital interconnect

The digital inputs should be isolated from the analog outputs and other analog circuitry as much as possible. Shielding the digital inputs will reduce noise on the power and ground lines. The lengths of clock and data lines should be minimized to prevent high-frequency clock and data information from inducing noise into the analog part of the video system. Active termination resistors for the digital inputs should be connected to the PCB power plane, not the APP. These digital inputs should not overlay the device ground plane.

analog signal interconnect

Minimizing the lead lengths between groups of V_{DD} and GND will minimize inductive ringing. To minimize noise pickup due to reflections and impedance mismatch, the device should be located as close to the output connectors as possible. The external voltage reference should also be as close to the device as possible, to minimize noise pickup.

To maximize high-frequency supply voltage rejection, the video output signals should overlay the device ground plane and not the APP.

Each analog output should have a 75-Ω load resistor connected to GND for maximum performance. To minimize reflections, the resistor connections between current output and ground should be as close to the device as possible.

APPLICATION INFORMATION

clock interfacing

To facilitate the generation of high-frequency clock signals, the CLK and $\overline{\text{CLK}}$ pins are designed to accept differential signals that can be generated with 5-V (single supply) ECL logic. Due to noise margins of the CMOS process, the CLK and $\overline{\text{CLK}}$ inputs must be differential signals. Connecting a single-ended clock signal to CLK and connecting $\overline{\text{CLK}}$ to GND will not work.

The CLK and $\overline{\text{CLK}}$ pins require termination resistors (220-Ω to V_{DD} and 330-Ω to GND) that should be as close to the device as possible.

$\overline{\text{LD}}$ is typically generated by dividing the clock frequency by four (4:1 multiplexing) or five (5:1 multiplexing) and translating the resulting signal to TTL levels. Since no phase relationship between the $\overline{\text{LD}}$ and CLK signals is required, any propagation delay in $\overline{\text{LD}}$ caused by the divider circuitry will not affect device performance.

The pixel, overlay, sync and blank data are latched on the rising edge of $\overline{\text{LD}}$. $\overline{\text{LD}}$ may also be used as the shift clock for the video DRAMs. In short, $\overline{\text{LD}}$ provides the fundamental timing for the video system.

The Bt438 Clock Generator (from Brooktree) is recommended for generating the CLK, $\overline{\text{CLK}}$, $\overline{\text{LD}}$, and REF signals. It supports both 4:1 and 5:1 multiplexing. Alternatively, the Bt438 can interface the device to a TTL clock. Figure 5 illustrates the interconnection between the Bt438 and the device.

PRINCIPLES OF OPERATION

microprocessor unit (MPU) interface

As shown in the functional block diagram, the MPU has direct access to the internal control registers and color overlay palettes via a standard MPU interface. Since the palette RAM and overlay registers have dual ports, they can be updated without affecting the display refresh process. One port is allocated for updating or reading data and the other for display.

palette RAM write or read

The palette RAM location is addressed by the internal 8-bit address register (ADDR0-7). THE MPU can either write to or read from this register. The register eliminates the need for external address multiplexers. ADDR0-ADDR7 are updated via D0-D7. To address the red, green, and blue part of a particular RAM location, the internal address register is provided with two additional bits, ADDRa and ADDRb. These address bits count modulo 3 and are reset to 0 when the MPU accesses the internal address register.

After writing to or reading from the internal address register, the MPU executes three write or read cycles (red, green and blue). The register ADDRab is incremented after each of these cycles so that the red, green, and blue information is addressed from the correct part of the particular RAM location. During the blue write cycle, the red, green, and blue color information is adjoined to form a 24-bit word, which is then written to the particular RAM location. After the blue write/read cycle, the internal address register bits ADDR0-7 are incremented to access the next RAM location. For an entire palette RAM write or read, the bits ADDR0-7 are reset to 00 after accessing the FF (256) palette RAM location.

Two additional control bits, C0 and C1, are used to differentiate the palette RAM read/write function from other operations that utilize the internal address register. C0 and C1 are respectively set high and low for writing to or reading from the palette RAM. Table 1 summarizes this differentiation, along with other internal address register operations. Note that C0 and C1 are each set low for writing to or reading from the internal address register.

PRINCIPLES OF OPERATION

Table 1. Writing to or Reading from Palette RAM

R/$\overline{W}$	C1	C0	ADDRb	ADDRa	Function
L	L	L	X	X	write ADDR0-7: D0-D7→ADDR0-7; 0→ADDRa,b
L	L	H	L	L	write red color: D0-D7→RREG; increment ADDRa,b
L	L	H	L	H	write green color: D0-D7→GREG; increment ADDRa,b
L	L	H	H	L	write blue color: D0-D7→BREG; increment ADDRa,b; increment ADDR0-7; write palette RAM
H	L	L	X	X	read ADDR0-7: ADDR0-7→D0-D7; 0→ADDRa,b
H	L	H	L	L	read red color: R0-R7→D0-D7; increment ADDRa,b
H	L	H	L	H	read green color: G0-G7→D0-D7; increment ADDRa,b
H	L	H	H	L	read blue color: B0-B7→D0-D7; increment ADDRa,b; increment ADDR0-7

X = irrelevant

overlay register write/read

With a few exceptions, the overlay register operation is identical to the palette RAM write/read operation (refer to the palette RAM write/read section). Upon writing to or reading from the internal address register, the additional address register ADDRab is automatically reset to 0. ADDRab counts modulo 3 as the red, green, and blue information is written to or read from a particular overlay register. The four overlay registers are addressed with internal address register values 00-03. After writing/reading blue information, the internal address register bits ADDR0-7 are incremented to the next overlay location. After accessing overlay register value 03, the internal address register does not reset to 00 but is advanced to 04.

For writing to or reading from the internal address register, C0 and C1 are set low. When accessing the overlay registers, C0 and C1 are set high. Refer to Table 2 for quick reference.

Table 2. Writing to or Reading from Overlay Registers

R/$\overline{W}$	C1	C0	ADDRb	ADDRa	Function
L	L	L	X	X	write ADDR0-7: D0-D7→ADDR0-7; 0→ADDRa,b
L	H	H	L	L	write red color: D0-D7→RREG; increment ADDRa,b
L	H	H	L	H	write green color: D0-D7→GREG; increment ADDRa,b
L	H	H	H	L	write blue color: D0-D7→BREG; increment ADDRa,b; increment ADDR0-7; write overlay register
H	L	L	X	X	read ADDR0-7: ADDR0-7→D0-D7; 0→ADDRa,b
H	H	H	L	L	read red color: R0-R7→D0-D7; increment ADDRa,b
H	H	H	L	H	read green color: G0-G7→D0-D7; increment ADDRa,b
H	H	H	H	L	read blue color: B0-B7→D0-D7; increment ADDRa,b; increment ADDR0-7

X = irrelevant

PRINCIPLES OF OPERATION

control register write/read

The four control registers are addressed with internal address register values 04-07. Upon writing to or reading from the internal address register, the additional address bits ADDRab are automatically reset to 0. To facilitate read-modify-write operations, the internal address register does not increment after writing to or reading from the control registers. All control registers may be accessed at any time. When accessing the control registers, C0 and C1 are respectively set low and high. Refer to Table 3 for quick reference.

Table 3. Writing to or Reading from Control Registers

R/$\overline{W}$	C1	C0	ADDRba	ADDRab	Function
L	L	L	X	X	write ADDR0-7: D0-D7→ADDR0-7; 0→ADDRa,b
L	H	L	L	L	write control register: D0-D7→control register
H	L	L	X	X	read ADDR0-7: ADDR0-7→D0-D7; 0→ADDRa,b
H	H	L	L	L	read control register: control register→D0-D7

X = irrelevant

summary of internal address register operations

Table 4 provides a summary of operations that use the internal address register. Figure 1 presents the read/write timing for the device.

If an invalid address is loaded into the internal address register, the device will ignore subsequent data from the MPU during a write operation and will send incorrect data to the MPU during a read operation.

Table 4. Internal Address Register Operations

INTERNAL ADDRESS REGISTER VALUE (ADDR0-7) (HEX)	C1	C0	MPU ACCESS	ADDRab (counts modulo 3)	COLOR
00-FF	L	H	color palette RAM	00 01 11	red value green value blue value
00-03	H	H	over color 0 to 3	00 01 110	red value green value blue value
04	H	L	read mask register		
05	H	L	blink mask register		
06	H	L	command register		
07	H	L	test register		

interruption of display refresh pixel data (via simultaneous pixel data retrieval and MPU write)

If the MPU is writing to a particular palette RAM location or overlay register (during the blue cycle) and the display refresh process is accessing pixel data from the same RAM location or overlay register, one or more pixels on the display screen may be disturbed. If the MPU write data is valid during the complete chip enable period, a maximum of one pixel will be disturbed.

PRINCIPLES OF OPERATION

frame buffer interface and timing

An internal latch and multiplexer enables the frame buffer to send the pixel data to the device at TTL rates. On the rising edges of $\overline{LD}$, information for four or five consecutive pixels is latched into the device. This information includes the palette RAM address (up to 8 bits), the overlay register address (up to 2 bits), and the sync and blank information for each of the four or five consecutive pixels. The timing diagram for this pixel data input transfer is shown in Figure 2, along with the video output waveforms (IOR, IOG, and IOB). Note that with this architecture, the sync and blank timing can only be recognized with four- or-five-pixel resolution.

The display refresh process follows the first-in first-out format. Color data is output from the device in the same order in which palette RAM and overlay addresses are input. This process continues until all four or five pixels have been output, at which point the cycle will repeat.

The overlay timing can be controlled by the pixel timing. However, this approach requires that the frame buffer emit additional bit planes to control the overlay selection on a pixel basis. Alternatively, the overlay timing can be controlled by external character or cursor generation timing (see the color selection section).

No phase relationship between the $\overline{LD}$ and CLK signals is required (see Figure 2). Therefore, the $\overline{LD}$ signal can be derived by externally dividing the CLK signal by four or five. Any propagation delay in $\overline{LD}$ caused by the divider circuitry will not render the device nonfunctional. Regardless of the phase relationship between $\overline{LD}$ and CLK, the pixel, overlay, sync, and blank data are latched on the rising edge of $\overline{LD}$.

The device has an internal load signal (not brought out to a pin), which is synchronous to CLK and will follow $\overline{LD}$ by at least one and not more than four clock cycles. This internal load signal transfers the $\overline{LD}$-latched data into a second set of latches, which are then internally multiplexed at the pixel clock or CLK signal frequency.

For 4:1 or 5:1 multiplexing, a rising edge of $\overline{LD}$ should occur every four or five clock cycles. Otherwise, the internal load signal generation circuitry cannot lock onto or synchronize with $\overline{LD}$.

color selection

The read mask, blink mask, and command registers process eight bits of color information (P0-P7) and two bits of overlay information (OL0-OL1) for each pixel every clock cycle. Control registers allow individual bit planes to be enabled/disabled for display and/or blinked at one of four blink rates and duty cycles (see the command register section, bits CR4-CR5).

By monitoring the $\overline{BLK}$ input to determine vertical retrace intervals, the device ensures that a color change due to blinking occurs only during the nonactive display time. Thus, a color change does not occur in the middle of the screen. A vertical retrace is sensed when $\overline{BLK}$ is low for at least 256 $\overline{LD}$ cycles. The color information is then selected from the palette RAM or overlay registers, in accordance with the processed input pixel data. Table 5 presents the effect of the processed input pixel data upon color selection. Note that P0 is the least significant bit (LSB) of the color palette RAM. When CR6 is high and both OL1 and OL0 are low, color information resides in the color palette RAM. When CR6 is low or either of the overlay inputs is high, the overlay registers provide the DAC inputs.

PRINCIPLES OF OPERATION

Table 5. Input Pixel Data versus Color Selection

COMMAND REGISTER BIT	OVERLAY SELECT INPUT		COLOR ADDRESS (HEX)	COLOR INFORMATION
CR6	OL1	OL0	P7-P0	
H	L	L	00	color palette entry 00
H	L	L	01	color palette entry 01
.	.	.	.	. . . .
.	.	.	.	. . . .
.	.	.	.	. . . .
H	L	L	FF	color palette entry FF
L	L	L	XX	overlay register 0
X	L	H	XX	overlay register 1
X	H	L	XX	overlay register 2
X	H	H	XX	overlay register 3

X = irrelevant

video generation

The TLC34058 presents 8 bits of red, green, and blue information from either the palette RAM or overlay registers to the three 8-bit DACs during every clock cycle. The DAC outputs produce currents that correlate to their respective color input data. These output currents are translated to voltage levels that drive the color CRT monitor. The $\overline{\text{SYNC}}$ and $\overline{\text{BLK}}$ signals adjust the DAC analog output currents to generate specific output levels that are required in video applications. Table 6 shows the effect of $\overline{\text{SYNC}}$ and $\overline{\text{BLK}}$ upon the DAC output currents. Figure 3 presents the overall composite video output waveforms. Note that only the green output (IOG) contains sync information.

The DAC architecture ensures monotonicity and reduced switching transients by using identical current sources and routing their outputs to the DAC current output or GND. Utilizing identical current sources eliminates the need for precision component ratios within the DAC ladder circuitry. An on-chip operational amplifier stabilizes the DAC full-scale output current over temperature and power supply variations.

Table 6. Effects of Sync and Blank Upon DAC Output Currents (see Note 7)

DESCRIPTION	IOG (mA)	IOR, IOB (mA)	$\overline{\text{SYNC}}$	$\overline{\text{BLK}}$	DAC INPUTS
WHITE	26.67	19.05	H	H	FF
DATA	data + 9.05	data + 1.44	H	H	data
DATA w/o $\overline{\text{SYNC}}$	data + 1.44	data + 1.44	L	H	data
BLACK	9.05	1.44	H	H	00
BLACK w/o $\overline{\text{SYNC}}$	1.44	1.44	L	H	00
BLACK	7.62	0	H	L	xx
$\overline{\text{SYNC}}$	0	0	L	L	xx

command register

The MPU can write to or read from the command register at any time. The command register is not initialized. CR0 corresponds to the D0 data bus line. Refer to Table 7 for quick reference.

NOTE 7: The data in this table was measured with full-scale IOG current = 26.67 mA, R_{set} = 523 Ω, V_{ref} = 1.235 V.

PRINCIPLES OF OPERATION

TABLE 7. COMMAND REGISTER

COMMAND REGISTER BIT	COMMAND REGISTER BIT FUNCTION	COMMAND REGISTER BIT DESCRIPTION
CR7	Multiplex Select Bit low: selects 4:1 multiplexing high: selects 5:1 multiplexing	This bit selects either 4:1 or 5:1 multiplexing for the palette RAM and overlay register address, $\overline{SYNC}$, and $\overline{BLK}$ inputs. If 4:1 multiplexing is selected, the device ignores the 'E' palette RAM and overlay register address inputs. These inputs should be connected to GND, and the $\overline{LD}$ signal frequency should be 1/4 of the clock frequency. If 5:1 is specified, all of the palette RAM and overlay register address inputs are used and the $\overline{LD}$ signal should be 1/5 of the clock frequency.
CR6	RAM Enable Bit low: use overlay register 0 high: use palette RAM	When the overlay select bits, OL0 and OL1, are both low, this bit causes the DACs color information to be selected from overlay register 0 or the palette RAM.
CR5, CR4	Blink Rate Select Bits 00: 16 on, 48 off (25/75) 01: 16 on, 16 off (50/50) 10: 32 on, 32 off (50/50) 11: 64 on, 64 off (50/50)	These two bits select the blink rate cycle time and duty cycle. The on and off numbers specify the blink rate cycle time as the number of vertical periods. The numbers in parenthesis specify the duty cycle in (on/off) percent.
CR3	OL1 Blink Enable Bit low: disable blinking high: enable blinking	If this bit is a high, the OL1 [A-E] inputs will toggle between a logic 0 and their input value at the selected blink rate before latching the incoming pixel data. Simultaneously, command register CR1 must be set high. If the CR2 bit is low, the OL0 [A-E] inputs will be unaffected.
CR2	OL0 Blink Enable Bit low: disable blinking high: enable blinking	If this bit is high, the OL0 [A-E] inputs will toggle between a logic 0 and their input value at the selected blink rate before latching the incoming pixel data. Simultaneously, command register CR0 must be set high. If the CR2 bit is low, the OL0 [A-E] inputs will be unaffected.
CR1	OL1 Display Enable Bit low: disable high: enable	If this bit is low, the OL1 [A-E] inputs are forced to a logic 0 before latching the incoming pixel data. If the CR1 bit is high, the OL1 [A-E] inputs will be affected.
CR0	OL0 Display Enable Bit low: disable high: enable	If this bit is low, the OL0 [A-E] inputs are forced to a logic 0 before latching the incoming pixel data. If the CR0 bit is high, the OL0 [A-E] inputs will be affected.

read mask register

The read mask register is used to enable (high) or disable (low) the eight bit planes (P0-P7) within the palette RAM addresses. The enabling or disabling is accomplished by logic ANDing the read mask register with the palette RAM address before addressing the palette RAM. Note that read mask register bit 0 corresponds to data bus line D0. The MPU can write to or read from this register at any time. This register is not initalized.

blink mask register

The blink mask register is used to enable (high) or disable (low) the blinking of bit planes within the palette RAM addresses. For example, if blink mask register bit n is set high, the true Pn value will address the palette RAM during the on portion of the blink cycle. During the off part of the blink cycle, the Pn value will be replaced with a 0 before the palette RAM is addressed. The blink rate cycle time and duty cycle is specified by command register bits CR4 and CR5. If blink mask register bit n is set low, the true Pn value will always address the palette RAM. Note that blink mask register bit 0 corresponds to data bus line D0. This register is not intialized.

PRINCIPLES OF OPERATION

test register

The test register allows the MPU to read the inputs to the DAC for diagnostic purposes. The MPU can write to or read from this register at any time. This register is not initialized. Only the four least significant bits can be written to, while all 8 bits can be read. Note that test register bit 0 corresponds to data bus line D0.

A functional description of this register is presented in Table 8.

Table 8. Functional Description of Test Register

TR3-TR0	D4-D7	FUNCTION
0100	4 MSBs of blue data input	MPU read or write D0-D3
0010	4 MSBs of green data input	
0001	4 MSBs of red data input	
1100	4 LSBs of blue data input	MPU read D0 -D7
1010	4 LSBs of green data input	
1001	4 LSBs of red data input	

To read the DAC inputs, the MPU must first load the test register's four least significant bits. One of the test register bits, b0 (red DAC), b1 (green DAC), or b2 (blue DAC), must be set high and the other two bits low. This process determines whether the inputs to the red, green, or blue DAC will be read. The test register bit b3 must be set high for reading the four most significant DAC inputs or low for reading the four least significant inputs. The MPU then reads the test register while the test register's four least significant bits contain the previously written information. Note that either the device clock must be slowed down to the MPU cycle time or the same pixel and overlay data must be continuously presented to the device during the entire MPU read cycle.

See the TLC34075 Video Interface Palette Data Manual in Section 9 for product information.

General Information 1
General Purpose ADCs 2
General Purpose DACs 3
Video and High-Speed ADCs and DACs 4
DSP Analog Interface and Conversion 5
Video Interface Palettes 6
Analog Switches 7
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Data Manuals 9
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Mechanical Data 11

7 Analog Switches

D2234, JUNE 1976—REVISED SEPTEMBER 1986

- **Functionally Interchangeable with Siliconix DG182, DG185, DG188, DG191 with Same Terminal Assignments**
- **Monolithic Construction**
- **Adjustable Reference Voltage**
- **JFET Inputs**
- **Uniform On-State Resistance for Minimum Signal Distortion**
- **±10-V Analog Voltage Range**
- **TTL, MOS, and CMOS Logic Control Compatibility**

description

The TL182, TL185, TL188, and TL191 are monolithic high-speed analog switches using BI-MOS technology. They comprise JFET-input buffers, level translators, and output JFET switches. The TL182 switches are SPST; the TL185 switches are SPDT. The TL188 is a pair of complementary SPST switches as is each half of the TL191.

A high level at a control input of the TL182 turns the associated switch off. A high level at a control input of the TL185 turns the associated switch on. For the TL188, a high level at the control input turns the associated switches S1 on and S2 off.

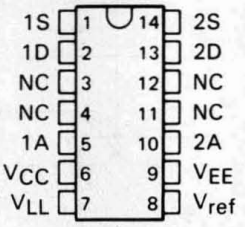
The threshold of the input buffer is determined by the voltage applied to the reference input (V_{ref}). The input threshold is related to the reference input by the equation $V_{th} = V_{ref} + 1.4$ V. Thus, for TTL compatibility, the V_{ref} input is connected to ground. The JFET input makes the device compatible with bipolar, MOD, and CMOS logic families. Threshold compatibility may, again, be determined by $V_{th} = V_{ref} + 1.4$ V.

The output switches are junction field-effect transistors featuring low on-state resistance and high off-state resistance. The monolithic structure ensures uniform matching.

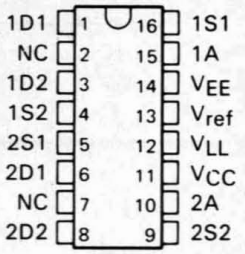
BI-MOS technology is a major breakthrough in linear integrated circuit processing. BI-MOS can have ion-implanted JFETs, p-channel MOS-FETs, plus the usual bipolar components all on the same chip. BI-MOS provides for monolithic circuit designs that previously have been available only as expensive hybrids.

M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. I-suffix devices are characterized for operation from −25°C to 85°C, and C-suffix devices are characterized for operation from 0°C to 70°C.

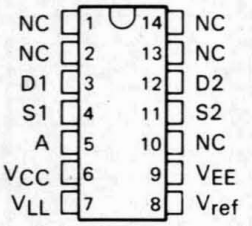
TL182
N PACKAGE
(TOP VIEW)



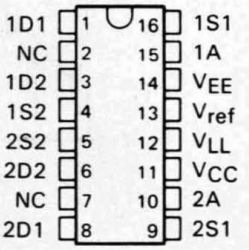
TL185
N PACKAGE
(TOP VIEW)



TL188
N PACKAGE
(TOP VIEW)



TL191
N PACKAGE
(TOP VIEW)



NC—No internal connection

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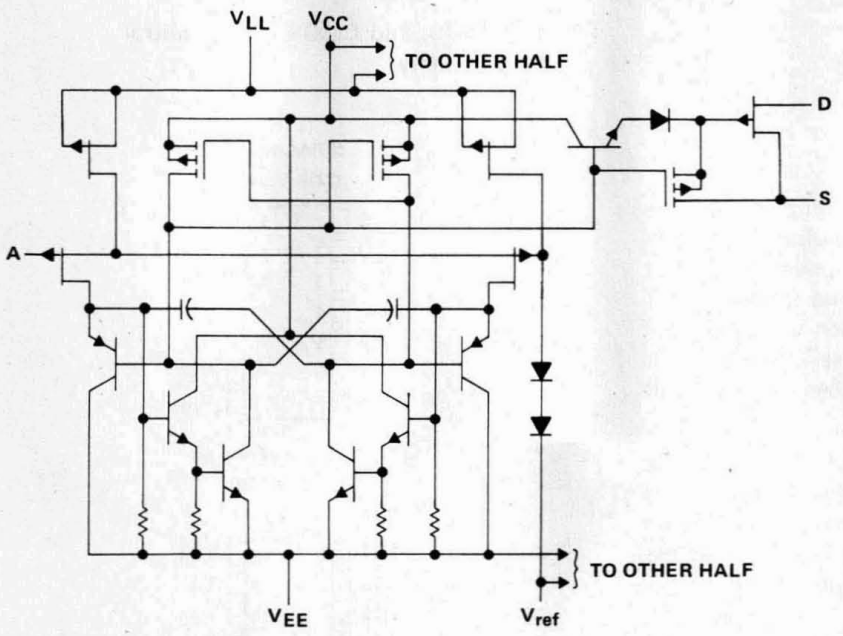
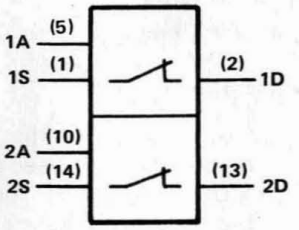
TL182 TWIN SPST SWITCH

schematic (each channel)



symbol

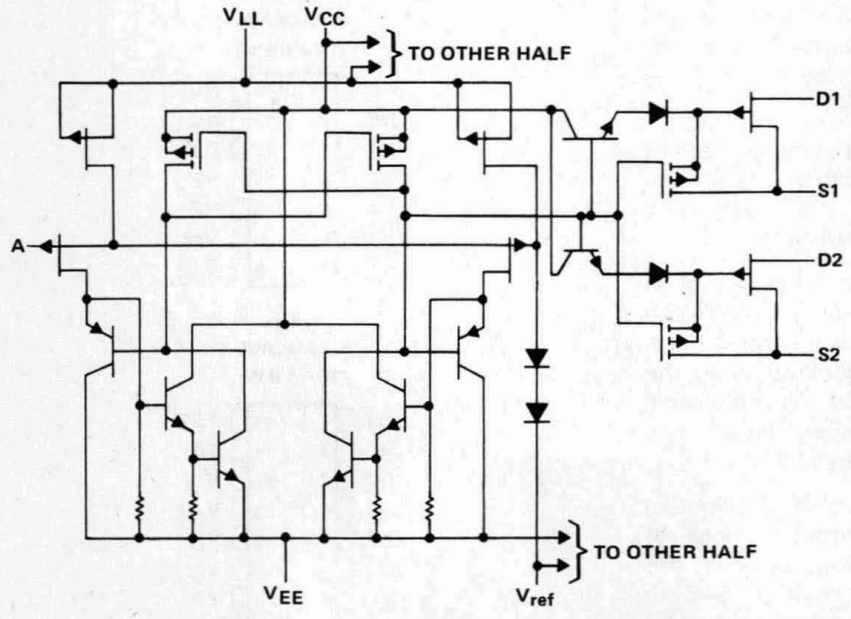


FUNCTION TABLE
(EACH HALF)

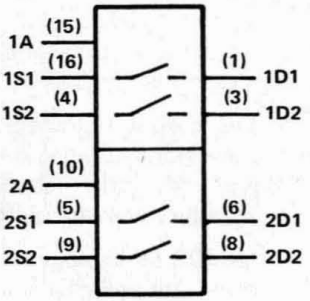
INPUT A	SWITCH S
L	ON (CLOSED)
H	OFF (OPEN)

TL185 TWIN DPST SWITCH

schematic (each channel)



symbol

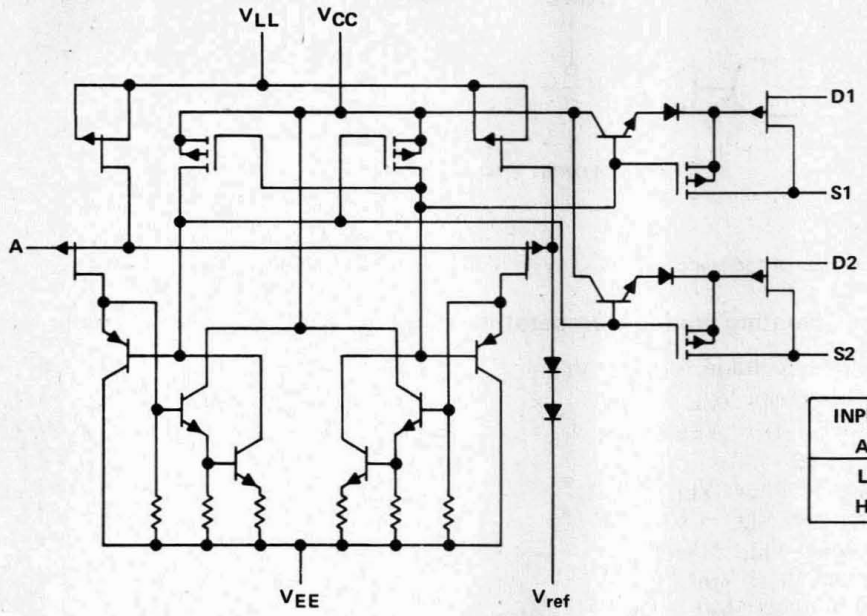


FUNCTION TABLE
(EACH HALF)

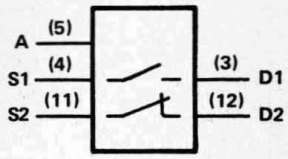
INPUT A	SWITCHES SW1 AND SW2
L	OFF (OPEN)
H	ON (CLOSED)

TL188 DUAL COMPLEMENTARY SPST SWITCH

schematic



symbol

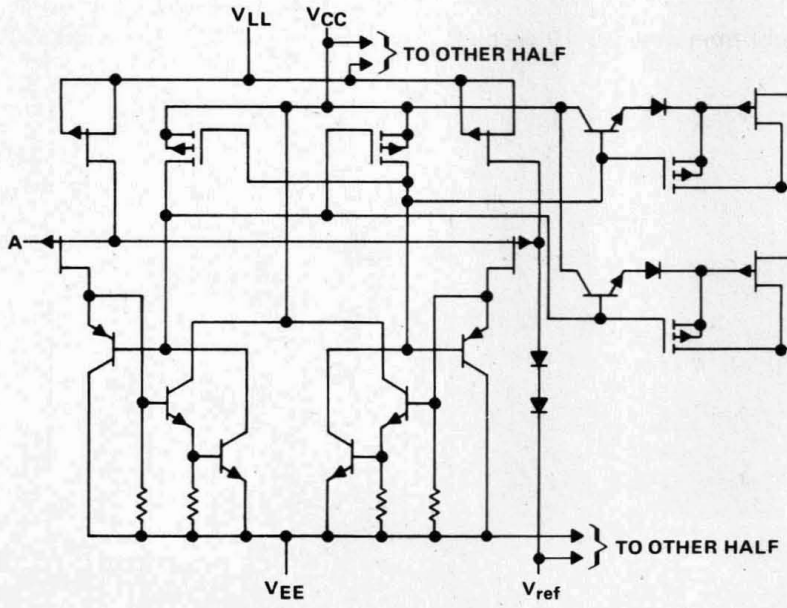


FUNCTION TABLE

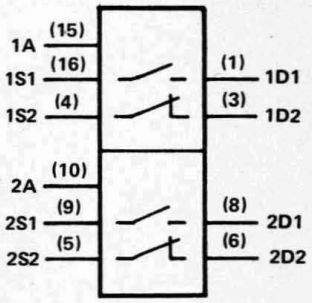
INPUT	SWITCHES	
A	SW1	SW2
L	OFF (OPEN)	ON (CLOSED)
H	ON (CLOSED)	OFF (OPEN)

TL191 TWIN DUAL COMPLEMENTARY SPST SWITCH

schematic (each channel)



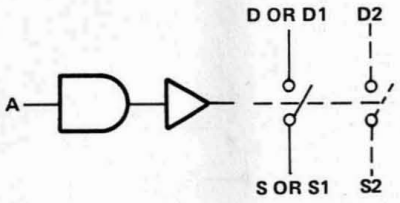
symbol



FUNCTION TABLE

INPUT	SWITCHES	
A	SW1	SW2
L	OFF (OPEN)	ON (CLOSED)
H	ON (CLOSED)	OFF (OPEN)

functional block diagram



See the preceding two pages for operation of the switches.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Positive supply to negative supply voltage, $V_{CC} - V_{EE}$ . . . . . 36 V
Positive supply voltage to either drain, $V_{CC} - V_D$ . . . . . 33 V
Drain to negative supply voltage, $V_D - V_{EE}$ . . . . . 33 V
Drain to source voltage, $V_D - V_S$ . . . . . ±22 V
Logic supply to negative supply voltage, $V_{LL} - V_{EE}$ . . . . . 36 V
Logic supply to logic input voltage, $V_{LL} - V_I$ . . . . . 33 V
Logic supply to reference voltage, $V_{LL} - V_{ref}$ . . . . . 33 V
Logic input to reference voltage, $V_I - V_{ref}$ . . . . . 33 V
Reference to negative supply voltage, $V_{ref} - V_{EE}$ . . . . . 27 V
Reference to logic input voltage, $V_{ref} - V_I$ . . . . . 2 V
Current (any terminal) . . . . . 30 mA
Operating free-air temperature range: TL182M, TL185M, TL188M, TL191M . . . . −55°C to 125°C
TL182I, TL185I, TL188I, TL191I . . . . . −25°C to 85°C
TL182C, TL185C, TL188C, TL191C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

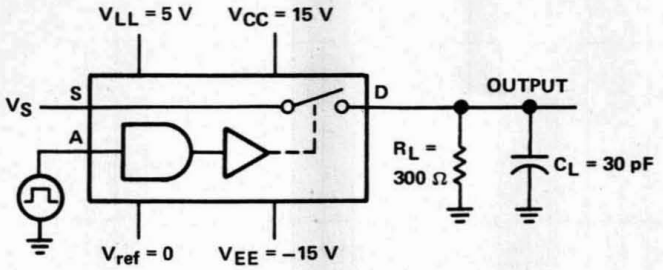
electrical characteristics, V_{CC} = 15 V, V_{EE} = −15 V, V_{LL} = 5 V, V_{ref} = 0 V

PARAMETER		TEST CONDITIONS			TL1_M MIN	TL1_M MAX	TL1_I MIN	TL1_I MAX	TL1_C MIN	TL1_C MAX	UNIT
V_{IH}	High-level control input voltage			T_A = MIN TO MAX	$V_{ref}+2$		$V_{ref}+2$		$V_{ref}+2$		V
V_{IL}	Low-level control input voltage			T_A = MIN to MAX		$V_{ref}+0.8$		$V_{ref}+0.8$		$V_{ref}+0.8$	V
I_{IH}	High-level control input current	V_I = 5 V		T_A = 25°C		10		10		20	μA
				T_A = MAX		20		20		20	
I_{IL}	Low-level control input current	V_I = 0		T_A = MIN to MAX		−250		−250		−250	μA
$I_{D(off)}$	Off-state drain current	V_D = 10 V, V_S = −10 V, V_{IH} = 2 V, V_{IL} = 0.8 V		T_A = 25°C				5		5	nA
				T_A = MAX		100		100		100	
$I_{S(off)}$	Off-state source current	V_D = −10 V, V_S = 10 V, V_{IH} = 2 V, V_{IL} = 0.8 V		T_A = 25°C				5		5	nA
				T_A = MAX		100		100		100	
$I_{D(on)}+I_{S(on)}$	On-state channel leakage current	V_D = −10 V, V_S = −10 V, V_{IH} = 2 V, V_{IL} = 0.8 V		T_A = 25°C				−10		−10	nA
				T_A = MAX		−200		−200		−200	
$r_{DS(on)}$	Drain-to-source on-state resistance	V_D = −10 V, I_S = 1 mA, V_{IH} = 2 V, V_{IL} = 0.8 V	TL182, TL188	T_A = MIN to 25°C		75		100		100	Ω
				T_A = MAX		100		150		150	
			TL185, TL191	T_A = MIN to 25°C		125		150		150	
				T_A = MAX		250		300		300	
I_{CC}	Supply current from V_{CC}	Both control inputs at 0 V		T_A = 25°C		1.5		1.5		1.5	mA
I_{EE}	Supply current from V_{EE}					−5		−5		−5	
I_{LL}	Supply current from V_{LL}					4.5		4.5		4.5	
I_{ref}	Reference current					−2		−2		−2	
I_{CC}	Supply current from V_{CC}	Both control inputs at 5 V		T_A = 25°C		1.5		1.5		1.5	mA
I_{EE}	Supply current from V_{EE}					−5		−5		−5	
I_{LL}	Supply current from V_{LL}					4.5		4.5		4.5	
I_{ref}	Reference current					−2		−2		−2	

switching characteristics, V_{CC} = 10 V, V_{EE} = −20 V, V_{LL} = 5 V, V_{ref} = 0 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TL1_M TYP	TL1_I TYP	TL1_C TYP	UNIT
t_{on}	Turn-on time	R_L = 300 Ω, C_L = 30 pF, Figure 1	175	175	175	ns
t_{off}	Turn-off time		350	350	350	

PARAMETER MEASUREMENT INFORMATION

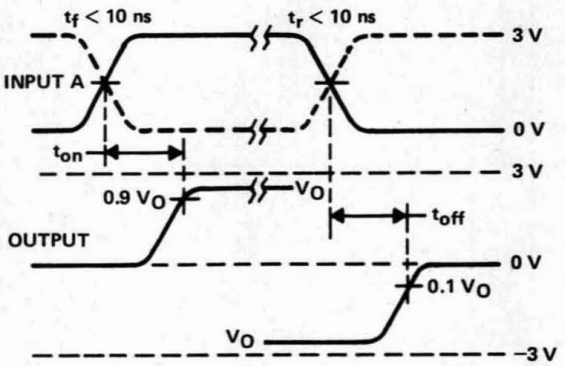


C_L includes probe and jig capacitance

V_S = 3 V for t_{on} and −3 V for t_{off}

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

TEST CIRCUIT



NOTE: A. The solid waveform applies for TL185 and SW1 of TL185 and TL191; the dashed waveform applies for TL182 and SW2 of TL185 and TL191.

B. V_O is the steady-state output with the switch on. Feed through via the gate capacitance may result in spikes (not shown) at the leading and trailing edges of the output waveform.

FIGURE 1. VOLTAGE WAVEFORMS

D2161, JUNE 1976—REVISED OCTOBER 1986

- **Switch ±10-V Analog Signals**
- **TTL Logic Capability**
- **5- to 30-V Supply Ranges**
- **Low (100 Ω) On-State Resistance**
- **High (10^{11} Ω) Off-State Resistance**
- **8-Pin Functions**

description

The TL601, TL604, TL607, and TL610 are a family of monolithic P-MOS analog switches that provide fast switching speeds with high r_{off}/r_{on} ratio and no offset voltage. The p-channel enhancement-type MOS switches accept analog signals up to ±10 V and are controlled by TTL-compatible logic inputs. The monolithic structure is made possible by BI-MOS technology, which combines p-channel MOS with standard bipolar transistors.

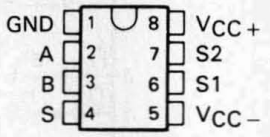
These switches are particularly useful in military, industrial, and commercial applications such as data acquisition, multiplexers, A/D and D/A converters, MODEMS, sample-and-hold systems, signal multiplexing, integrators, programmable operational amplifiers, programmable voltage regulators, crosspoint switching networks, logic interface, and many other analog systems.

The TL601 is an SPDT switch with two logic control inputs. The TL604 is a dual complementary SPST switch with a single control input. The TL607 is an SPDT switch with one logic control input and one enable input. The TL610 is an SPST switch with three logic control inputs. The TL610 features a higher r_{off}/r_{on} ratio than the other members of the family.

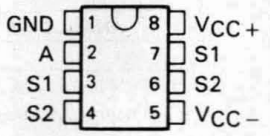
The TL601M, TL604M, TL607M, and TL610M are characterized for operation over the full military temperature range of −55°C to 125°C, the TL601I, TL604I, TL607I, and TL610I are characterized for operation from −25°C to 85°C, and the TL601C, TL604C, TL607C, and TL610C are characterized for operation from 0°C to 70°C.

JG OR P PACKAGE
(TOP VIEW)

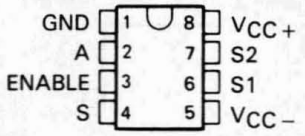
TL601



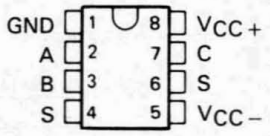
TL604



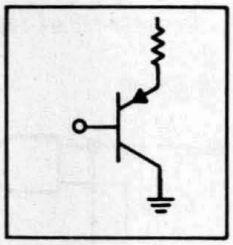
TL607



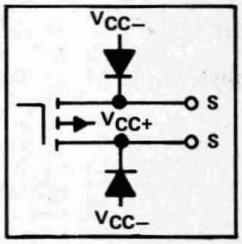
TL610



TYPICAL OF ALL INPUTS



TYPICAL OF ALL SWITCHES



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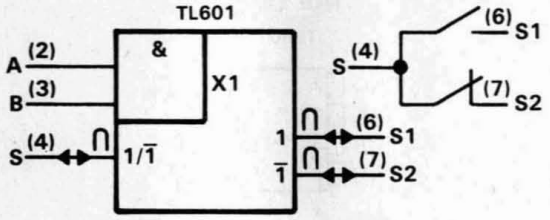
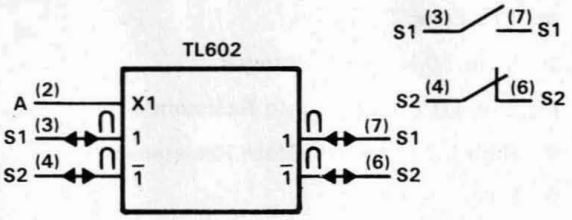
logic symbols† and switch diagrams



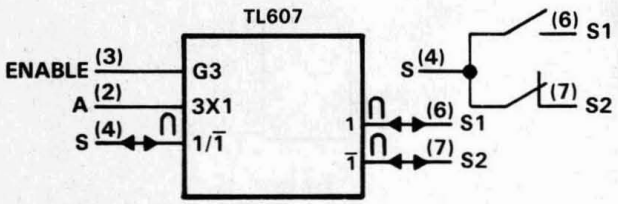
FUNCTION TABLE

LOGIC INPUTS		ANALOG SWITCH	
A	B	S1	S2
L	X	OFF (OPEN)	ON (CLOSED)
X	L	OFF (OPEN)	ON (CLOSED)
H	H	ON (CLOSED)	OFF (OPEN)



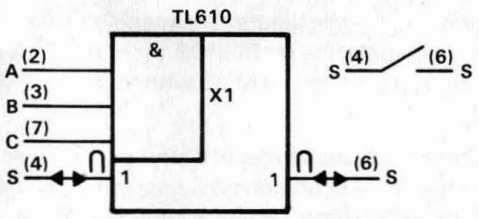
FUNCTION TABLE

LOGIC INPUT	ANALOG SWITCH	
A	S1	S2
H	ON (CLOSED)	OFF (OPEN)
L	OFF (OPEN)	ON (CLOSED)



FUNCTION TABLE

INPUTS		ANALOG SWITCH	
A	ENABLE	S1	S2
X	L	OFF (OPEN)	OFF (OPEN)
L	H	OFF (OPEN)	ON (CLOSED)
H	H	ON (CLOSED)	OFF (OPEN)

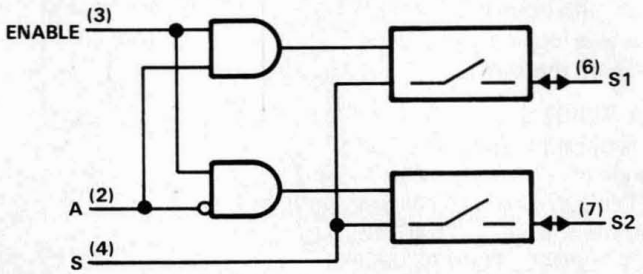


FUNCTION TABLE

INPUTS			ANALOG SWITCH
A	B	C	S
L	X	X	OFF (OPEN)
X	L	X	OFF (OPEN)
X	X	L	OFF (OPEN)
H	H	H	ON (CLOSED)

†These symbols are in accordance with ANSI/IEEE Std 91-1984.

TL607 logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 30 V
Supply voltage, V_{CC-} . . . . . −30 V
V_{CC+} to V_{CC-} supply voltage differential . . . . . 35 V
Control input voltage . . . . . V_{CC+}
Switch off-state voltage . . . . . 30 V
Switch on-state current . . . . . 10 mA
Operating free-air temperature range: TL601M, TL604M, TL607M, TL610M . . . . −55°C to 125°C
TL601I, TL604I, TL607I, TL610I . . . . . −25°C to 85°C
TL601C, TL604C, TL607C, TL610C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature (1,6 mm) 1/16 inch from case for 60 seconds: JG package . . . . . 300°C
Lead temperature (1,6 mm) 1/16 inch from case for 10 seconds: P package . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

	TL601M, TL604M TL607M, TL610M			TL601I, TL604I TL607I, TL610I			TL601C, TL604C TL607C, TL610C			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+} (see Figure 1)	5	10	25	5	10	25	5	10	25	V
Supply voltage, V_{CC-} (see Figure 1)	−5	−20	−25	−5	−20	−25	−5	−20	−25	V
V_{CC+} to V_{CC-} supply voltage differential (see Figure 1)	15		30	15		30	15		30	V
High-level control input voltage, V_{IH}	2		5.5	2		5.5	2		5.5	V
Low-level control input voltage, V_{IL} All inputs			0.8			0.8			0.8	
Voltage at any analog switch (S) terminal	$V_{CC-}+8$		V_{CC+}	$V_{CC-}+8$		V_{CC+}	$V_{CC-}+8$		V_{CC+}	V
Switch on-state current			10			10			10	mA
Operating free-air temperature, T_A	−55		125	−25		85	0		70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 10 V, V_{CC-} = −20 V, analog switch test current = 1 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			TL6__M TL6__I			TL6__C			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
I_{IH}	High-level input current	V_I = 5.5 V				0.5	10		0.5	10	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−50	−250		−50	−250	μA
I_{off}	Switch off-state current	$V_{I(sw)}$ = −10 V, See Note 2		T_A = 25°C		−400			−500		pA
				T_A = MAX†		−50	−100		−10	−20	nA
r_{on}	Switch on-state resistance	$V_{I(sw)}$ = 10 V, $I_{O(sw)}$ = −1 mA		TL601 TL604 TL607		55	100		75	200	Ω
				TL610		40	80		40	100	
		$V_{I(sw)}$ = −10 V, $I_{O(sw)}$ = −1 mA		TL601 TL604 TL607		220	400		220	600	
				TL610		120	300		120	400	
r_{off}	Switch off-state resistance					25			20		GΩ
C_{on}	Switch on-state input capacitance	$V_{I(sw)}$ = 0 V, f = 1 MHz				16			16		pF
C_{off}	Switch off-state input capacitance	$V_{I(sw)}$ = 0 V, f = 1 MHz				8			8		pF
I_{CC+}	Supply current from V_{CC+}	Logic input(s) at 5.5 V, All switch terminals open		TL601 TL604		5	10		5	10	mA
			Enable input high	TL607		5	10		5	10	
			Enable input low			3	5		3	5	
				TL610		5	10		5	10	
I_{CC-}	Supply current from V_{CC-}	Logic input(s) at 5.5 V, All switch terminals open		TL601 TL604		−1.2	−2.5		−1.2	−2.5	mA
			Enable input high	TL607		−2.5	−5		−2.5	−5	
			Enable input low			−0.05	−0.5		−0.05	−0.5	
				TL610		−1.2	−2.5		−1.2	−2.5	

†MAX is 125°C for M-suffix types, 85°C for I-suffix types, and 70°C for C-suffix types.
‡All typical values are at T_A = 25°C except for I_{off} at T_A = MAX.
NOTE 2: The other terminal of the switch under test is at V_{CC+} = 10 V.

switching characteristics, V_{CC+} = 10 V, V_{CC-} = −20 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{off}	Switch turn-off time	R_L = 1 kΩ, C_L = 35 pF, See Figure 2		400	500	ns
t_{on}	Switch turn-on time			100	150	

Figure 1 shows power supply boundary conditions for proper operation of the TL601 Series. The range of operation for supply V_{CC+} from +5 V to +25 V is shown on the vertical axis. The range of V_{CC-} from −5 V to −25 V is shown on the horizontal axis. A recommended 30-V maximum voltage differential from V_{CC+} to V_{CC-} governs the maximum V_{CC+} for a chosen V_{CC-} (or vice versa). A minimum recommended difference of 15 V from V_{CC+} to V_{CC-} and the boundaries shown in Figure 1 allow the designer to select the proper combinations of the two supplies.

The designer-selected V_{CC+} supply value for a chosen V_{CC-} supply value limits the maximum input voltage that can be applied to either switch terminal; that is, the input voltage should be between V_{CC-} +8 V and V_{CC+} to keep the on-state resistance within specified limits.

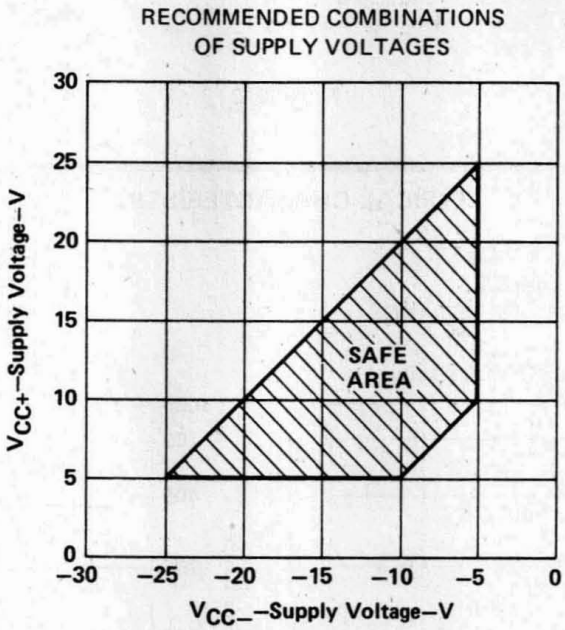
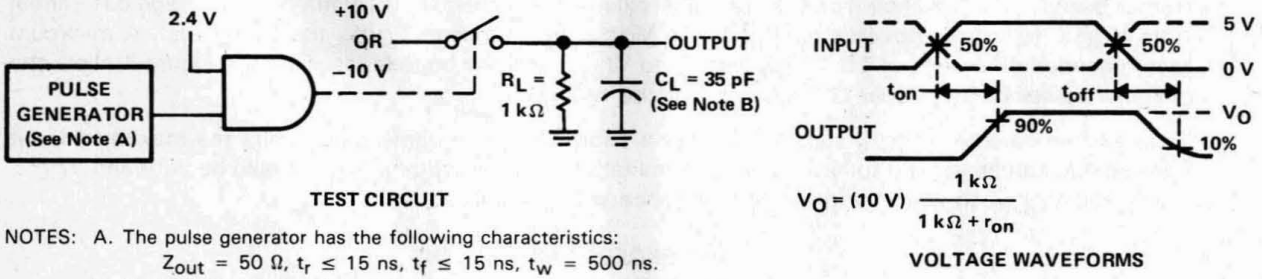


FIGURE 1

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics:
Z_{out} = 50 Ω, $t_r \le 15$ ns, $t_f \le 15$ ns, t_w = 500 ns.
B. C_L includes probe and jig capacitance.

FIGURE 2

TYPICAL CHARACTERISTICS

M-SUFFIX DEVICES
I-SUFFIX DEVICES
SWITCH ON-STATE RESISTANCE
vs
SWITCH ANALOG VOLTAGE

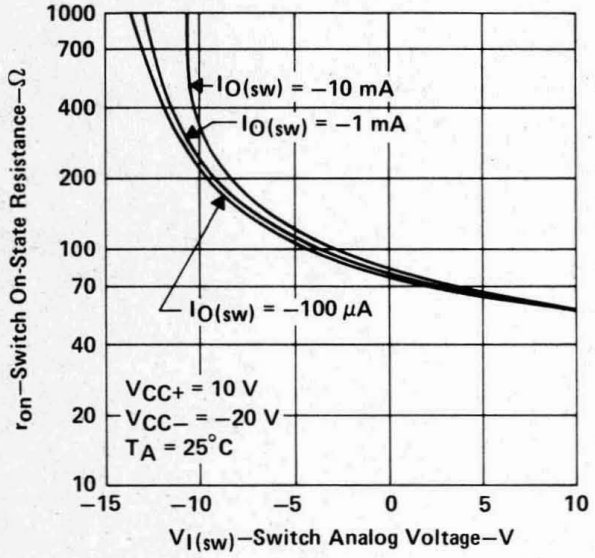


FIGURE 3

M-SUFFIX DEVICES
I-SUFFIX DEVICES
SWITCH ON-STATE RESISTANCE
vs
FREE-AIR TEMPERATURE

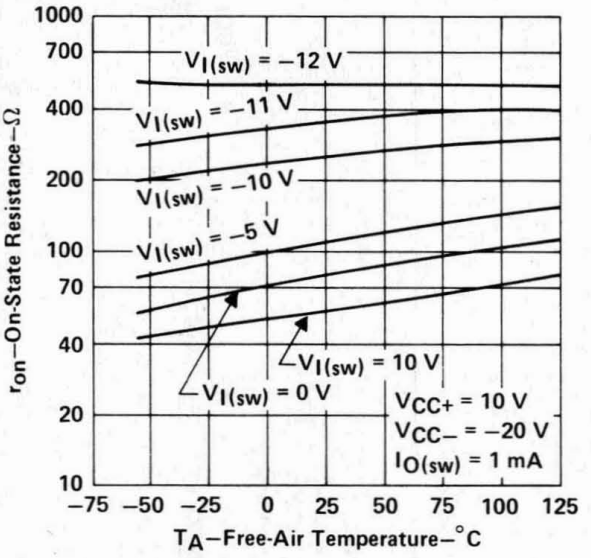
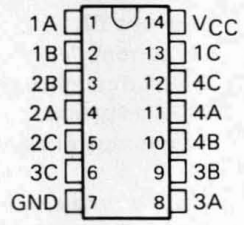


FIGURE 4

D2922, JANUARY 1986—REVISED OCTOBER 1988

- **High Degree of Linearity**
- **High On-Off Output Voltage Ratio**
- **Low Crosstalk Between Switches**
- **Low On-State Impedance . . . 50 Ω Typ at V_{CC} = 9 V**
- **Individual Switch Controls**
- **Extremely Low Input Current**

TLC4016M . . . J OR N PACKAGE
TLC4016I . . . D OR N PACKAGE
(TOP VIEW)



description

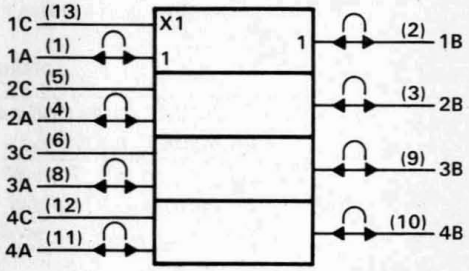
The TLC4016 is a silicon-gate CMOS quadruple analog switch designed to handle both analog and digital signals. Each switch permits signals with amplitudes up to 12 V peak to be transmitted in either direction.

Each switch section has its own enable input control. A high-level voltage applied to this control terminal turns on the associated switch section.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

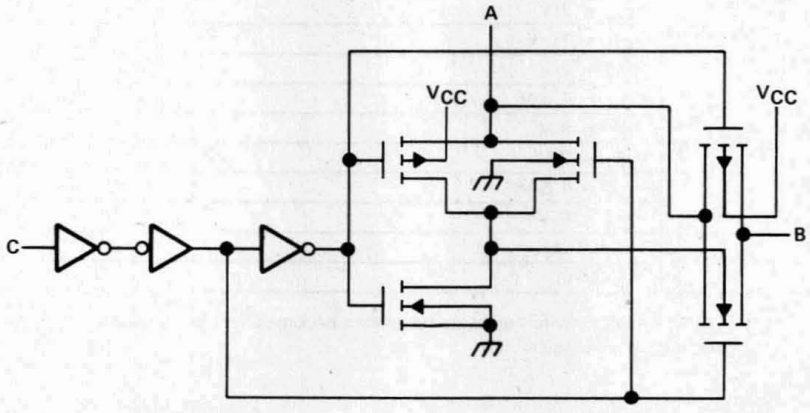
The TLC4016M is characterized for operation from −55°C to 125°C, and the TLC4016I is characterized from −40°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range (see Note 1) . . . . . −0.5 V to 15 V
Control-input diode current ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
I/O port diode current ($V_I < 0$ or $V_{I/O} > V_{CC}$) . . . . . ±20 mA
On-state switch current ($V_{I/O}$ = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Continuous total dissipation . . . . . see Dissipation Rating Table
Operating free-air temperature range: TLC4016M . . . . . −55°C to 125°C
TLC4016I . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTE 1: All voltages are with respect to ground unless otherwise specified.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	N/A
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		2†	5	12	V
I/O port voltage, $V_{I/O}$		0		V_{CC}	V
High-level input voltage, V_{IH}	V_{CC} = 2 V	1.5		V_{CC}	V
	V_{CC} = 4.5 V	3.15		V_{CC}	
	V_{CC} = 9 V	6.3		V_{CC}	
	V_{CC} = 12 V	8.4		V_{CC}	
Low-level input voltage, V_{IL}	V_{CC} = 2 V	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	
	V_{CC} = 9 V	0		1.8	
	V_{CC} = 12 V	0		2.4	
Input rise time, t_r	V_{CC} = 2 V			1000	ns
	V_{CC} = 4.5 V			500	
	V_{CC} = 9 V			400	
Input fall time, t_f	V_{CC} = 2 V			1000	ns
	V_{CC} = 4.5 V			500	
	V_{CC} = 9 V			400	
Operating free-air temperature, T_A	TLC4016M	−55		125	°C
	TLC4016I	−40		85	

†With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER			TEST CONDITIONS	V_{CC}	TLC4016M			TLC4016I			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
r_{Son}	On-state switch resistance		I_S = 1 mA, V_A = 0 to V_{CC}, See Figure 1	4.5 V		100	220		100	200	Ω
				9 V		50	120		50	105	
				12 V		30	100		30	85	
			I_S = 1 mA, V_A = 0 or V_{CC}, See Figure 1	2 V		120	240		120	215	
				4.5 V		50	120		50	100	
				9 V		35	80		35	75	
				12 V		20	70		20	60	
	On-state switch resistance matching		V_A = 0 to V_{CC}, See Figure 1	4.5 V		10	20		10	20	Ω
				9 V		5	15		5	15	
				12 V		5	15		5	15	
I_I	Control input current		V_I = 0 or V_{CC}	2 V to 6 V			±1			±1	μA
			V_I = 0 or V_{CC}, T_A = 25°C				±0.1			±0.1	
I_{Soff}	Off-state switch leakage current		V_S = ±V_{CC}, See Figure 2	5.5 V		±10	±600		±10	±600	nA
				9 V		±15	±800		±15	±800	
				12 V		±20	±1000		±20	±1000	
I_{Son}	On-state switch leakage current		V_A = 0 or V_{CC}, See Figure 3	5.5 V		±10	±150		±10	±150	nA
				9 V		±15	±200		±15	±200	
				12 V		±20	±300		±20	±300	
I_{CC}	Supply current		V_I = 0 or V_{CC}, I_O = 0	5.5 V		2	40		2	20	μA
				9 V		8	160		8	80	
				12 V		16	320		16	160	
C_i	Input capacitance	A or B		2 V to 12 V		15			15		pF
		C				5	10		5	10	
C_f	Feedthrough capacitance	A to B	V_I = 0	2 V to 12 V		5			5		pF

†All typical values are at T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	TLC4016M			TLC4016I			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	Propagation delay time, A to B or B to A	See Figure 4	2 V		25	75		25	62	ns
			4.5 V		5	15		5	13	
			9 V		4	14		4	12	
			12 V		3	13		3	11	
t_{on}	Switch turn-on time	R_L = 1 kΩ, See Figures 5 and 6	2 V		32	150		32	125	ns
			4.5 V		8	30		8	25	
			9 V		6	18		6	15	
			12 V		5	15		5	13	
t_{off}	Switch turn-off time	R_L = 1 kΩ, See Figures 5 and 6	2 V		45	252		45	210	ns
			4.5 V		15	54		15	45	
			9 V		10	48		10	40	
			12 V		8	45		8	38	
f_{co}	Switch cutoff frequency (channel loss = 3 dB)		4.5 V		100			100		MHz
			9 V		120			120		
$V_{OCF(PP)}$	Control feedthrough voltage to any switch, peak to peak	See Figure 7	4.5 V			350			350	mV
	Frequency at which crosstalk attenuation between any two switches equals 50 dB	See Figure 8	4.5 V		1			1		MHz

†All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

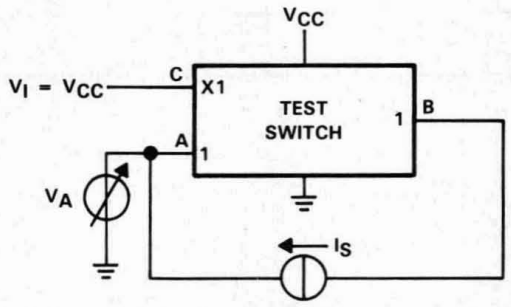
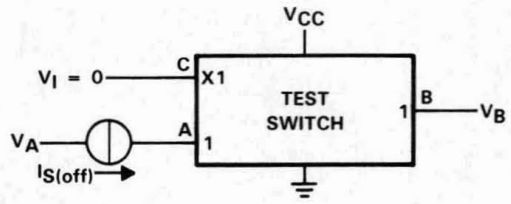


FIGURE 1. TEST CIRCUIT FOR ON-STATE RESISTANCE



$V_S = V_A - V_B$

CONDITION 1: V_A = 0, $V_B = V_{CC}$

CONDITION 2: $V_A = V_{CC}$, V_B = 0

FIGURE 2. TEST CIRCUIT FOR OFF-STATE SWITCH LEAKAGE CURRENT

PARAMETER MEASUREMENT INFORMATION

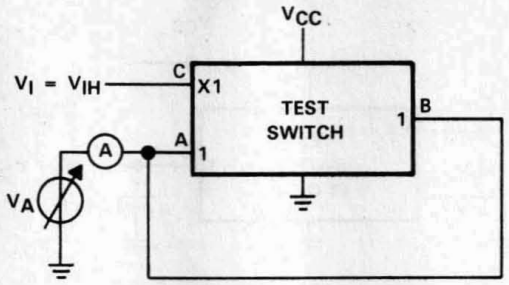
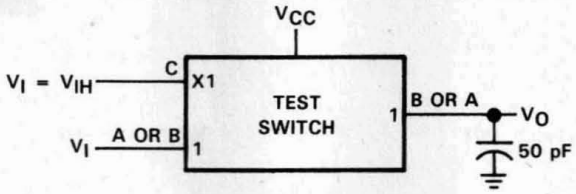
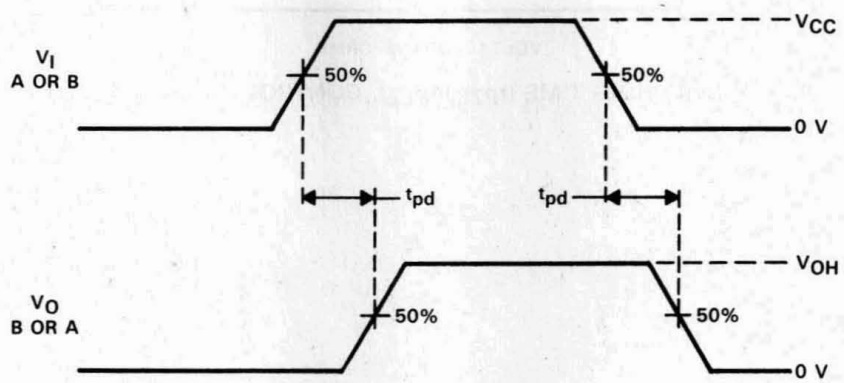


FIGURE 3. TEST CIRCUIT FOR ON-STATE SWITCH LEAKAGE CURRENT



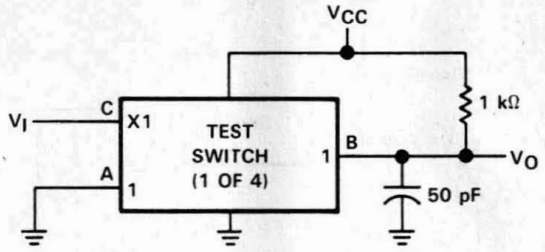
TEST CIRCUIT



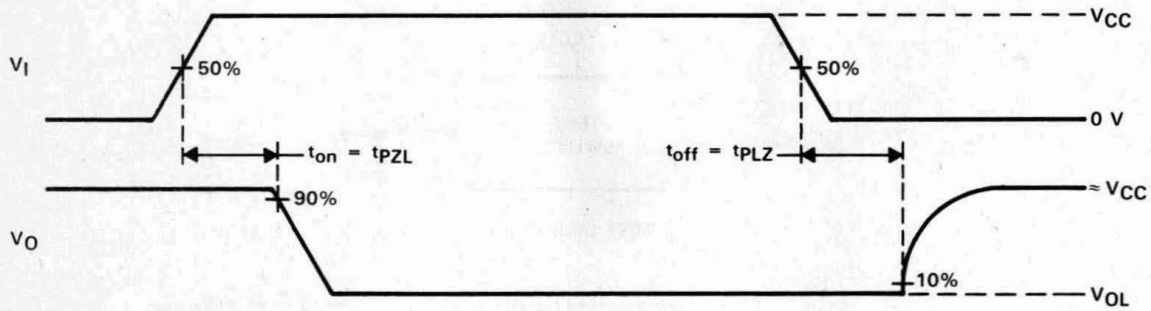
VOLTAGE WAVEFORMS

FIGURE 4. PROPAGATION DELAY TIME, SIGNAL INPUT TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION



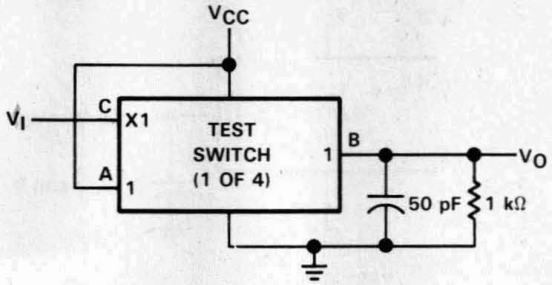
TEST CIRCUIT



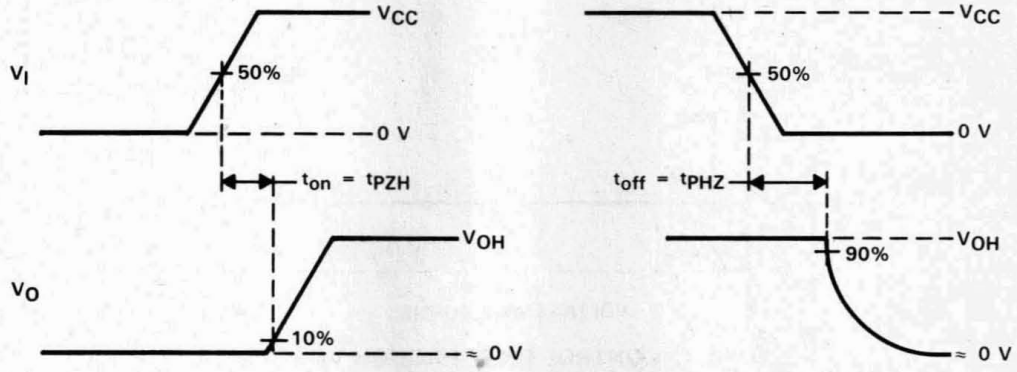
VOLTAGE WAVEFORMS

FIGURE 5. SWITCHING TIME (t_{PZL}, t_{PLZ}), CONTROL TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION



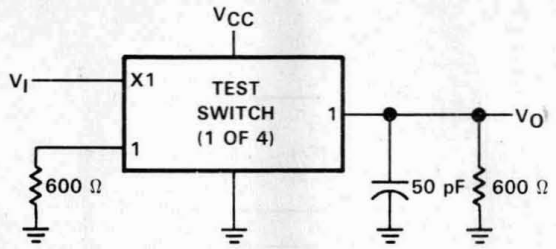
TEST CIRCUIT



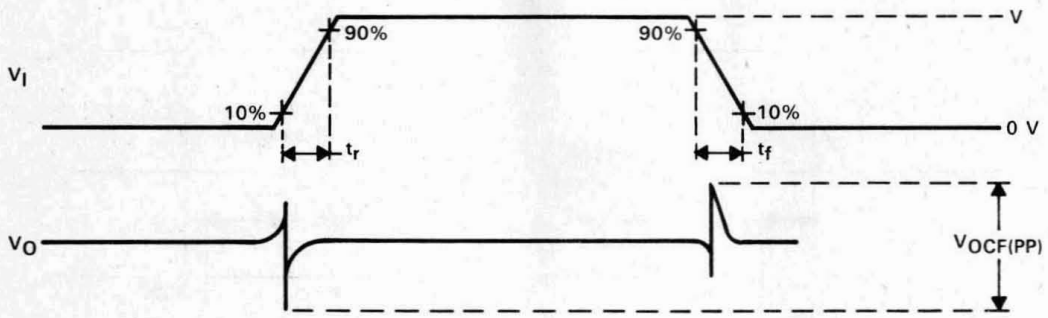
VOLTAGE WAVEFORMS

FIGURE 6. SWITCHING TIME (t_{PZH}, t_{PHZ}), CONTROL TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION

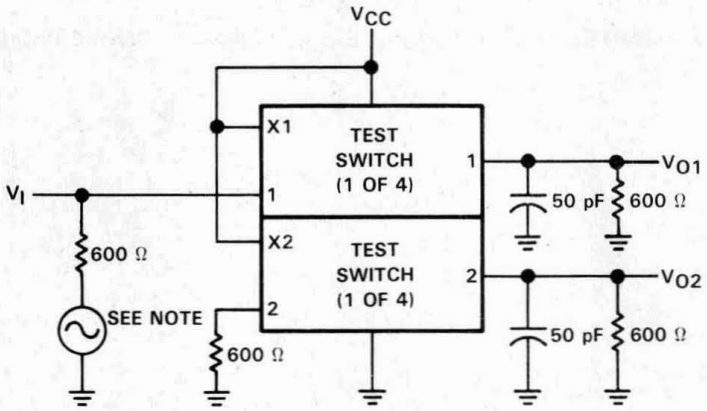


TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 7. CONTROL FEEDTHROUGH VOLTAGE



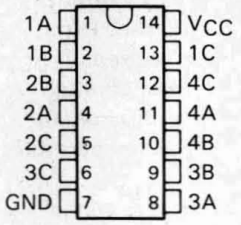
NOTE: ADJUST f for $a_X = \frac{V_{O2}}{V_{O1}} = 50$ dB.

FIGURE 8. CROSSTALK BETWEEN ANY TWO SWITCHES, TEST CIRCUIT

D2922, JANUARY 1986—REVISED OCTOBER 1988

- **High Degree of Linearity**
- **High On-Off Output Voltage Ratio**
- **Low Crosstalk Between Switches**
- **Low On-State Impedance . . . 30 Ω Typ at V_{CC} = 12 V**
- **Individual Switch Controls**
- **Extremely Low Input Current**
- **Functionally Interchangeable with National Semiconductor MM54/74HC4066, Motorola MC54/74HC4066, and RCA CD4066A**

TLC4066M . . . J OR N PACKAGE
TLC4066I . . . D OR N PACKAGE
(TOP VIEW)



description

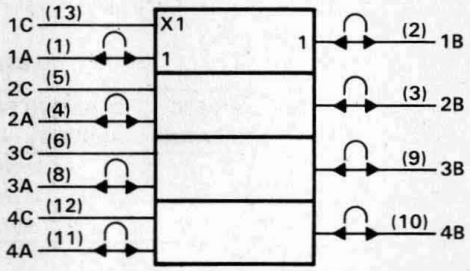
The TLC4066 is a silicon-gate CMOS quadruple analog switch designed to handle both analog and digital signals. Each switch permits signals with amplitudes up to 12 V peak to be transmitted in either direction.

Each switch section has its own enable input control. A high-level voltage applied to this control terminal turns on the associated switch section.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

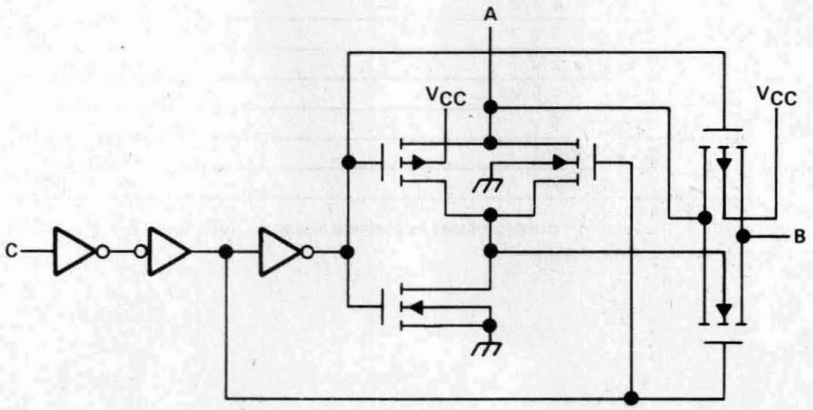
The TLC4066M is characterized for operation from −55°C to 125°C. The TLC4066I is characterized from −40°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range (see Note 1) . . . . . −0.5 V to 15 V
Control-input diode current ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
I/O port diode current ($V_I < 0$ or $V_{I/O} > V_{CC}$) . . . . . ±20 mA
On-state switch current ($V_{I/O}$ = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Continuous total dissipation . . . . . see Dissipation Rating Table
Operating free-air temperature: TLC4066M . . . . . −55°C to 125°C
TLC4066I . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTE 1: All voltages are with respect to ground unless otherwise specified.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	N/A
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		2†	5	12	V
I/O port voltage, $V_{I/O}$		0		V_{CC}	V
High-level input voltage, V_{IH}	V_{CC} = 2 V	1.5		V_{CC}	V
	V_{CC} = 4.5 V	3.15		V_{CC}	
	V_{CC} = 9 V	6.3		V_{CC}	
	V_{CC} = 12 V	8.4		V_{CC}	
Low-level input voltage, V_{IL}	V_{CC} = 2 V	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	
	V_{CC} = 9 V	0		1.8	
	V_{CC} = 12 V	0		2.4	
Input rise time, t_r	V_{CC} = 2 V			1000	ns
	V_{CC} = 4.5 V			500	
	V_{CC} = 9 V			400	
Input fall time, t_f	V_{CC} = 2 V			1000	ns
	V_{CC} = 4.5 V			500	
	V_{CC} = 9 V			400	
Operating free-air temperature, T_A	TLC4066M	−55		125	°C
	TLC4066I	−40		85	

†With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	TLC4066M			TLC4066I			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
r_{Son}	On-state switch resistance		I_S = 1 mA, V_A = 0 to V_{CC}, See Figure 1	4.5 V		100	220		100	200	Ω
				9 V		50	110		50	105	
				12 V		30	90		30	85	
			I_S = 1 mA, V_A = 0 or V_{CC}, See Figure 1	2 V		120	240		120	215	
				4.5 V		50	120		50	100	
				9 V		35	80		35	75	
				12 V		20	70		20	60	
	On-state switch resistance matching		V_A = 0 to V_{CC}, See Figure 1	4.5 V		10	20		10	20	Ω
				9 V		5	15		5	15	
				12 V		5	15		5	15	
I_I	Control input current		V_I = 0 or V_{CC}	2 V or 6 V			±1			±1	μA
I_{Soff}	Off-state switch leakage current		V_S = ±V_{CC}, See Figure 2	5.5 V		±10	±600		±10	±600	nA
				9 V		±15	±800		±15	±800	
				12 V		±20	±1000		±20	±1000	
I_{Son}	On-state switch leakage current		V_A = 0 or V_{CC}, See Figure 3	5.5 V		±10	±150		±10	±150	nA
				9 V		±15	±200		±15	±200	
				12 V		±20	±300		±20	±300	
I_{CC}	Supply current		V_I = 0 or V_{CC}, I_O = 0	5.5 V		2	40		2	20	μA
				9 V		8	160		8	80	
				12 V		16	320		16	160	
C_i	Input capacitance	A or B		2 V to 12 V		15			15		pF
		C				5	10		5	10	
C_f	Feedthrough capacitance	A to B	V_I = 0	2 V to 12 V		5			5		pF

†All typical values are at T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	TLC4066M			TLC4066I			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	Propagation delay time, A to B or B to A	See Figure 4	2 V		25	75		15	30	ns
			4.5 V		5	15		5	13	
			9 V		4	12		4	10	
			12 V		3	13		3	11	
t_{on}	Switch turn-on time	R_L = 1 kΩ, See Figures 5 and 6	2 V		32	150		32	125	ns
			4.5 V		8	30		8	25	
			9 V		6	18		6	15	
			12 V		5	15		5	13	
t_{off}	Switch turn-off time	R_L = 1 kΩ, See Figures 5 and 6	2 V		45	252		45	210	ns
			4.5 V		15	54		15	45	
			9 V		10	48		10	40	
			12 V		8	45		8	38	
f_{co}	Switch cutoff frequency (channel loss = 3 dB)		4.5 V		100			100		MHz
			9 V		120			120		
$V_{OCF(PP)}$	Control feedthrough voltage to any switch, peak to peak	See Figure 7	4.5 V			350			350	mV
	Frequency at which crosstalk attenuation between any two switches equals 50 dB	See Figure 8	4.5 V		1			1		MHz

†All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

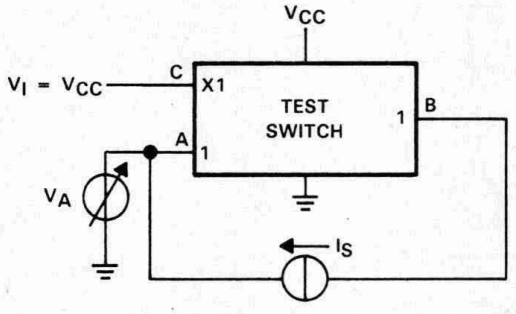
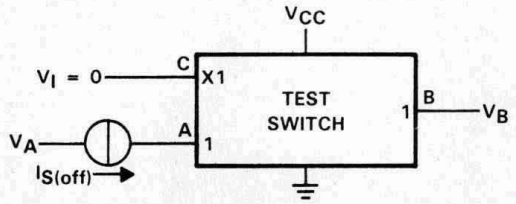


FIGURE 1. TEST CIRCUIT FOR ON-STATE RESISTANCE



$V_S = V_A - V_B$

CONDITION 1: V_A = 0, $V_B = V_{CC}$

CONDITION 2: $V_A = V_{CC}$, V_B = 0

FIGURE 2. TEST CIRCUIT FOR OFF-STATE SWITCH LEAKAGE CURRENT

PARAMETER MEASUREMENT INFORMATION

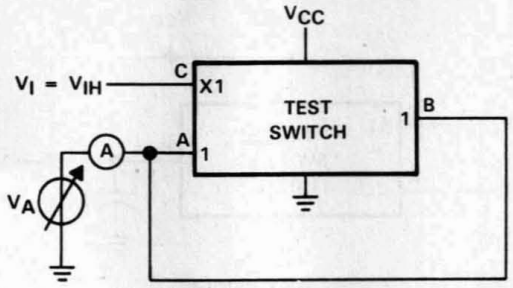
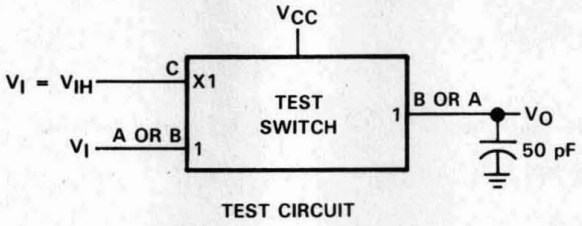
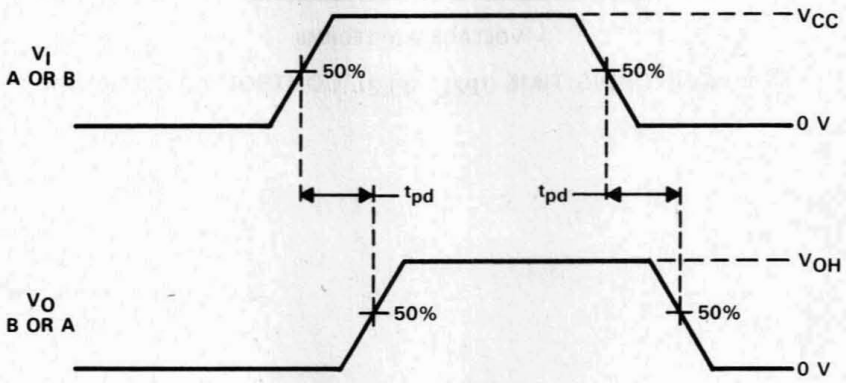


FIGURE 3. TEST CIRCUIT FOR ON-STATE SWITCH LEAKAGE CURRENT



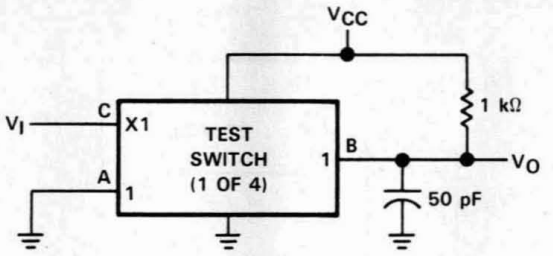
TEST CIRCUIT



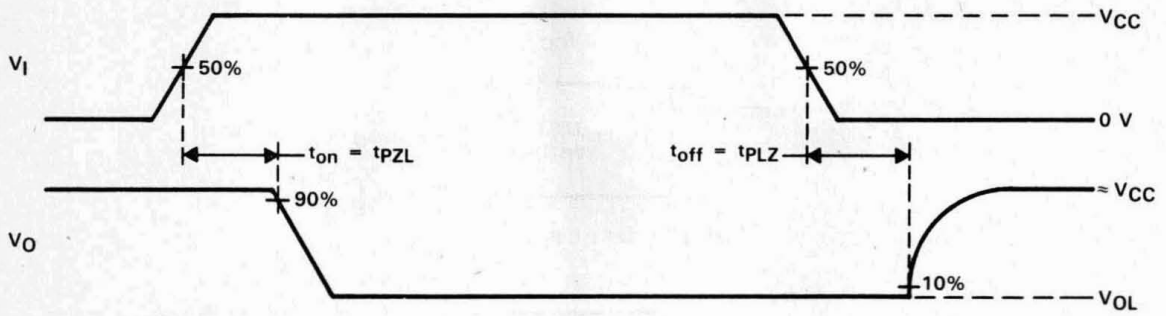
VOLTAGE WAVEFORMS

FIGURE 4. PROPAGATION DELAY TIME, SIGNAL INPUT TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION



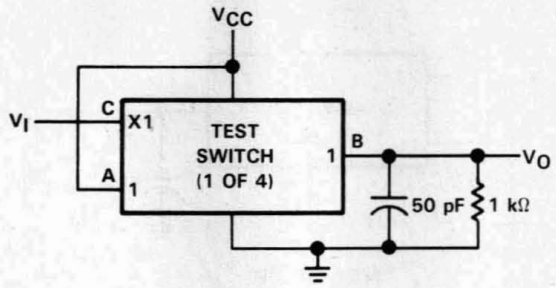
TEST CIRCUIT



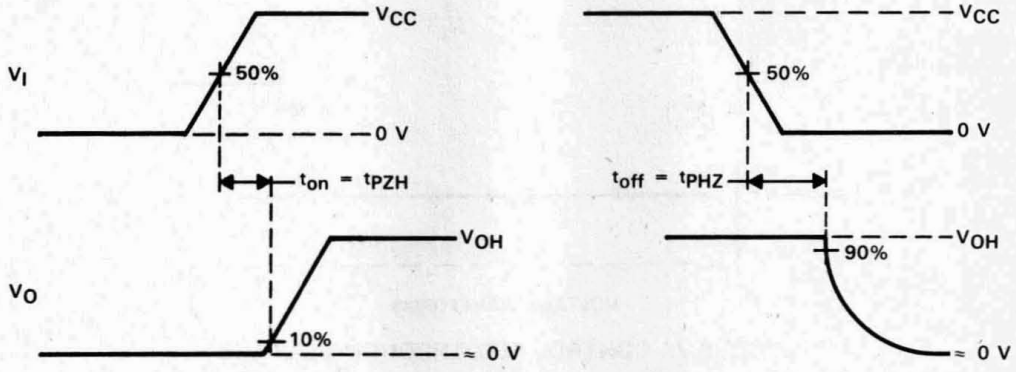
VOLTAGE WAVEFORMS

FIGURE 5. SWITCHING TIME (t_{PZL}, t_{PLZ}), CONTROL TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 6. SWITCHING TIME (t_{PZH}, t_{PHZ}), CONTROL TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION

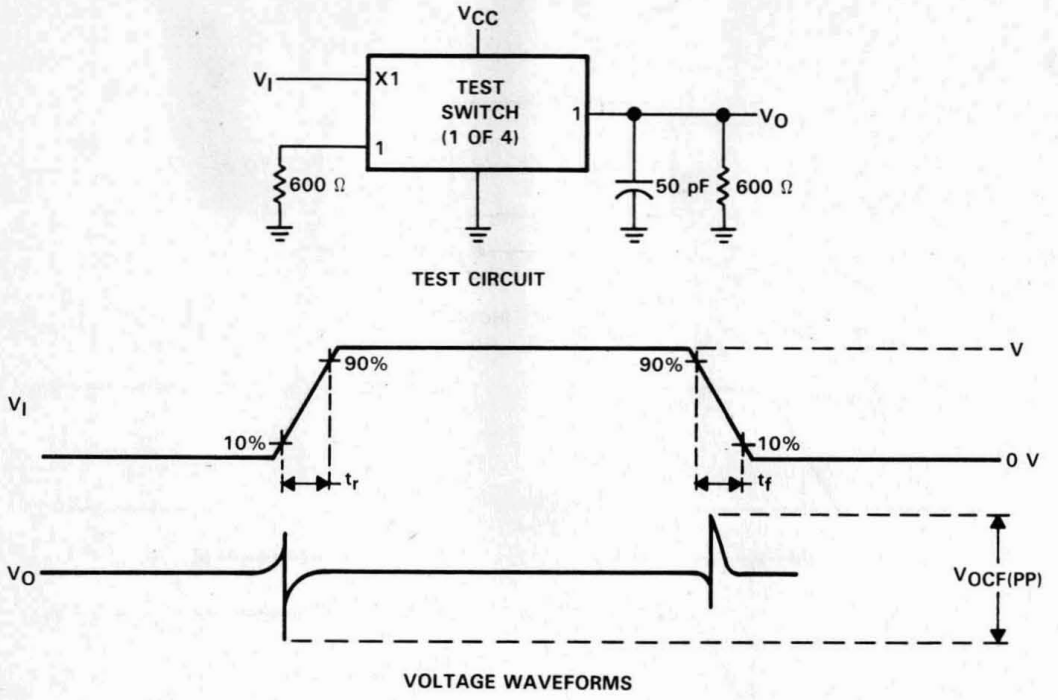
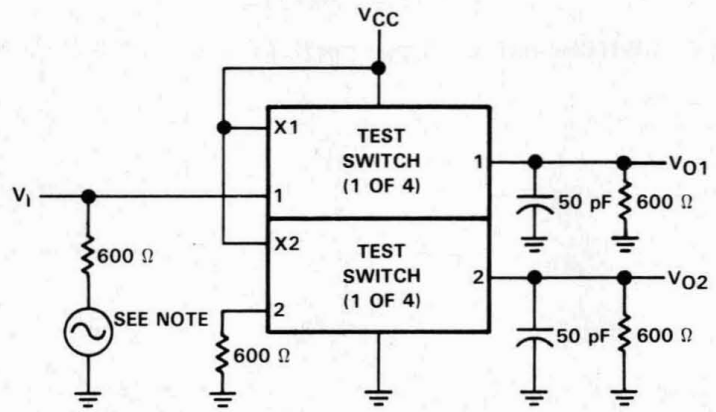


FIGURE 7. CONTROL FEEDTHROUGH VOLTAGE



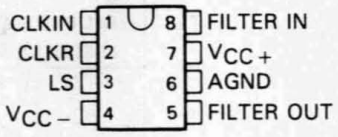
NOTE: ADJUST f for $a_X = \frac{V_{O2}}{V_{O1}} = 50$ dB.

FIGURE 8. CROSSTALK BETWEEN ANY TWO SWITCHES, TEST CIRCUIT

General Information 1
General Purpose ADCs 2
General Purpose DACs 3
Video and High-Speed ADCs and DACs 4
DSP Analog Interface and Conversion 5
Video Interface Palettes 6
Analog Switches 7
Filters 8
Data Manuals 9
Application Reports 10
Mechanical Data 11

- **Low Clock-to-Cutoff-Frequency Ratio Error**
  TLC04/MF4A-50 . . . ±0.8%
  TLC14/MF4A-100 . . . ±1%
- **Filter Cutoff Frequency Dependent Only on External-Clock Frequency Stability**
- **Minimum Filter Response Deviation Due to External Component Variations Over Time and Temperature**
- **Cutoff Frequency Range from 0.1 Hz to 30 kHz, $V_{CC\pm}$ = ±2.5 V**
- **5-V to 12-V Operation**
- **Self Clocking or TTL-Compatible and CMOS-Compatible Clock Inputs**
- **Low Supply Voltage Sensitivity**
- **Designed to be Interchangeable with National MF4-50 and MF4-100**

D OR P PACKAGE
(TOP VIEW)



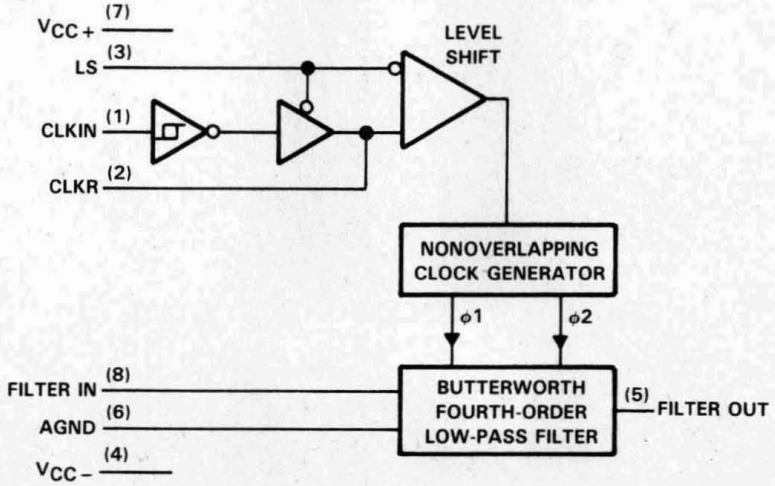
description

The TLC04/MF4A-50 and TLC14/MF4A-100 are monolithic Butterworth low-pass switched-capacitor filters. Each is designed as a low-cost, easy-to-use device providing accurate fourth-order low-pass filter functions in circuit design configurations.

Each filter features cutoff frequency stability that is dependent only on the external-clock frequency stability. The cutoff frequency is clock tunable and has a clock-to-cutoff frequency ratio of 50:1 with less than ±0.8% error for the TLC04/MF4A-50 and a clock-to-cutoff frequency ratio of 100:1 with less than ±1% error for the TLC14/MF4A-100. The input clock features self-clocking or TTL- or CMOS-compatible options in conjunction with the level shift (LS) pin.

The TLC04M/MF4A-50M and TLC14M/MF4A-100M are characterized over the full military temperature range of −55°C to 125°C. The TLC04I/MF4A-50I and TLC14I/MF4A-100I are characterized for operation from −40°C to 85°C. The TLC04C/MF4A-50C and TLC14C/MF4A-100C are characterized for operation from 0°C to 70°C.

functional block diagram



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AVAILABLE OPTIONS

T_A	CLOCK-TO-CUTOFF FREQUENCY RATIO	PACKAGE	
		SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	50:1	TLC04CD/MF4A-50CD	TLC04CP/MF4A-50CP
	100:1	TLC14CD/MF4A-100CD	TLC14CP/MF4A-100CP
−40°C to 85°C	50:1	TLC04ID/MF4A-50ID	TLC04IP/MF4A-50IP
	100:1	TLC14ID/MF4A-100ID	TLC14IP/MF4A-100IP
−55°C to 125°C	50:1		TLC04MP/MF4A-50MP
	100:1		TLC14MP/MF4A-100MP

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC04CDR/MF4A-50CDR).

pin description

PIN NAME	PIN NO.	I/O	DESCRIPTION
AGND	6	I	Analog Ground — The noninverting input to the operational amplifiers of the Butterworth fourth-order low-pass filter.
CLKIN	1	I	Clock In — The clock input terminal for CMOS-compatible clock or self-clocking options. For either option, the Level Shift (LS) terminal is at V_{CC-}. For self-clocking, a resistor is connected between the CLKIN and CLKR terminal pins and a capacitor is connected from the CLKIN terminal pin to ground.
CLKR	2	I	Clock R — The clock input for a TTL-compatible clock. For a TTL clock, the level shift pin is connected to mid-supply and the CLKIN pin may be left open, but it is recommended that it be connected to either V_{CC+} or V_{CC-}.
FILTER IN	8	I	Filter Input
FILTER OUT	5	O	Butterworth fourth-order low-pass Filter Output
LS	3	I	Level Shift — This terminal accommodates the various input clocking options. For CMOS-compatible clocks or self-clocking, the level-shift terminal is at V_{CC-} and for TTL-compatible clocks, the level-shift terminal is at mid-supply.
V_{CC+}	7	I	Positive supply voltage terminal
V_{CC-}	4	I	Negative supply voltage terminal

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC\pm}$ (see Note 1) . . . . . ±7 V
Operating free-air temperature range: TLC04M/MF4A-50M, TLC14M/MF4A-100M −55°C to 125°C
TLC04I/MF4A-50I, TLC14I/MF4A-100I . . . . . −40°C to 85°C
TLC04C/MF4A-50C, TLC14C/MF4A-100C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to the AGND terminal.

recommended operating conditions

			TLC04/MF4A-50		TLC14/MF4A-100		UNIT
			MIN	MAX	MIN	MAX	
V_{CC+}	Positive supply voltage		2.25	6	2.25	6	V
V_{CC-}	Negative supply voltage		−2.25	−6	−2.25	−6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
f_{clock}	Clock frequency (see Note 2)	$V_{CC\pm}$ = ±2.5 V	5	1.5×10^6	5	1.5×10^6	Hz
		$V_{CC\pm}$ = ±5 V	5	2×10^6	5	2×10^6	
f_{co}	Cutoff frequency (see Note 3)		0.1	40×10^3	0.05	20×10^3	Hz
T_A	Operating free-air temperature	TLC04M/MF4A-50M, TLC14M/MF4A-100M	−55	125	−55	125	°C
		TLC04I/MF4A-50I, TLC14I/MF4A-100I	−40	85	−40	85	
		TLC04C/MF4A-50C, TLC14C/MF4A-100C	0	70	0	70	

NOTES: 2. Above 250 kHz, the input clock duty cycle should be 50% to allow the operational amplifiers the maximum time to settle while processing analog samples.
3. The cutoff frequency is defined as the frequency where the response is 3.01 dB less than the dc gain of the filter.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 2.5 V, V_{CC-} = −2.5 V, $f_{clock} \leq$ 250 kHz (unless otherwise noted)

filter section

PARAMETER			TEST CONDITIONS	TLC04/MF4A-50			TLC14/MF4A-100			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OO}	Output voltage offset				25			50		mV
V_{OM}	Peak output voltages	V_{OM+}	R_L = 10 kΩ	1.8	2		1.8	2		V
		V_{OM-}		−1.25	−1.7		−1.25	−1.7		
I_{OS}	Short-circuit output current	Source	T_A = 25°C, See Note 4		−0.5			−0.5		mA
		Sink			4			4		
I_{CC}	Supply current		f_{clock} = 250 kHz		1.2	2.25		1.2	2.25	mA

NOTE 4: I_{OS} (source current) is measured by forcing the output to its maximum positive voltage and then shorting the output to the negative supply (V_{CC-}) terminal. I_{OS} (sink current) is measured by forcing the output to its maximum negative voltage and then shorting the output to the positive supply (V_{CC+}) terminal.

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 2.5 V, V_{CC-} = −2.5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TLC04/MF4A-50			TLC14/MF4A-100			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Maximum clock frequency, f_{max}	See Note 2		1.5	3		1.5	3		MHz
Clock-to-cutoff-frequency ratio (f_{clock}/f_{co})	$f_{clock} \leq$ 250 kHz, T_A = 25°C		49.27	50.07	50.87	99	100	101	
Temperature coefficient of clock-to-cutoff frequency ratio	$f_{clock} \leq$ 250 kHz			±25			±25		ppm/°C
Frequency response above and below cutoff frequency (see Note 5)	f_{co} = 5 kHz, f_{clk} = 250 kHz, T_A = 25°C	f = 6 kHz	−7.9	−7.57	−7.1				dB
		f = 4.5 kHz	−1.7	−1.46	−1.3				
	f_{co} = 2.5 kHz, f_{clk} = 250 kHz, T_A = 25°C	f = 3 kHz				−7.9	−7.42	−7.1	dB
		f = 2.25 kHz				−1.7	−1.51	−1.3	
Dynamic range (see Note 6)	T_A = 25°C			80			78		dB
Stop-band frequency attentuation at 2 f_{co}	$f_{clock} \leq$ 250 kHz		24	25		24	25		dB
DC voltage amplification	$f_{clock} \leq$ 250 kHz, RS ≤ 2 kΩ		−0.15	0	0.15	−0.15	0	0.15	dB
Peak-to-peak clock feedthrough voltage	T_A = 25°C			5			5		mV

† All typical values are at T_A = 25°C.

NOTES: 2. Above 250 kHz, the input clock duty cycle should be 50% to allow the operational amplifiers the maximum time to settle while processing analog samples.

5. The frequency responses at f are referenced to a dc gain of 0 dB.

6. The dynamic range is referenced to 1.06 V rms (1.5 V peak) where the wideband noise over a 30-kHz bandwidth is typically 106 μV rms for the TLC04/MF4A-50 and 135 μV rms for the TLC14/MF4A-100.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, $f_{clock} \leq$ 250 kHz, (unless otherwise noted)

filter section

PARAMETER		TEST CONDITIONS	TLC04/MF4A-50			TLC14/MF4A-100			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OO} Output voltage offset				150			200		mV
V_{OM} Peak output voltages	V_{OM+}	R_L = 10 kΩ	3.75	4.3		3.75	4.5		V
	V_{OM-}		−3.75	−4.1		−3.75	−4.1		
I_{OS} Short-circuit output current	Source	T_A = 25°C, See Note 4		−2			−2		mA
	Sink			5			5		
I_{CC} Supply current		f_{clock} = 250 kHz		1.8	3		1.8	3	mA
k_{SVS} Supply voltage sensitivity (see Figures 1 and 2)				−30			−30		dB

NOTE 4: I_{OS} (source current) is measured by forcing the output to its maximum positive voltage and then shorting the output to the negative supply (V_{CC-}) terminal. I_{OS} (sink current) is measured by forcing the output to its maximum negative voltage and then shorting the output to the positive supply (V_{CC+}) terminal.

clocking section

PARAMETER		TEST CONDITIONS‡		MIN	TYP†	MAX	UNIT
V_{T+} Positive-going input threshold voltage	CLKIN	V_{CC+} = 10 V, V_{CC-} = 0		6.1	7	8.9	V
		V_{CC+} = 5 V, V_{CC-} = 0		3.1	3.5	4.4	
V_{T-} Negative-going input threshold voltage	CLKIN	V_{CC+} = 10 V, V_{CC-} = 0		1.3	3	3.8	V
		V_{CC+} = 5 V, V_{CC-} = 0		0.6	1.5	1.9	
V_{hys} Hysteresis ($V_{T+} - V_{T-}$)	CLKIN	V_{CC+} = 10 V, V_{CC-} = 0		2.3	4	7.6	V
		V_{CC+} = 5 V, V_{CC-} = 0		1.2	2	3.8	
V_{OH} High-level output voltage	CLKR	V_{CC} = 10 V	I_O = −10 μA	9			V
		V_{CC} = 5 V		4.5			
V_{OL} Low-level output voltage	CLKR	V_{CC} = 10 V	I_O = 10 μA			1	V
		V_{CC} = 5 V				0.5	
Input leakage current	CLKR	V_{CC} = 10 V	Level Shift pin at mid-supply,			2	μA
		V_{CC} = 5 V	T_A = 25°C			2	
Output current	CLKR	V_{CC} = 10 V	CLKR and CLKIN	−3	−7		mA
		V_{CC} = 5 V	shorted to V_{CC-}	−0.75	−2		
Output current	CLKR	V_{CC} = 10 V	CLKR and CLKIN	3	7		mA
		V_{CC} = 5 V	shorted to V_{CC+}	0.75	2		

†All typical values are at T_A = 25°C.
‡$V_{CC} = V_{CC+} - V_{CC-}$.

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TLC04/MF4A-50			TLC14/MF4A-100			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Maximum clock frequency, f_{max} (see Note 2)			2	4		2	4		MHz
Clock-to-cutoff-frequency ratio (f_{clock}/f_{co})	$f_{clock} \le 250$ kHz, T_A = 25°C		49.58	49.98	50.38	99	100	101	
Temperature coefficient of clock-to-cutoff frequency ratio	$f_{clock} \le 250$ kHz			±15			±15		ppm/°C
Frequency response above and below cutoff frequency (see Note 5)	f_{co} = 5 kHz, f_{clk} = 250 kHz, T_A = 25°C	f = 6 kHz	−7.9	−7.57	−7.1				dB
		f = 4.5 kHz	−1.7	−1.44	−1.3				
	f_{co} = 2.5 kHz, f_{clk} = 250 kHz, T_A = 25°C	f = 3 kHz				−7.9	−7.42	−7.1	dB
		f = 2.25 kHz				−1.7	−1.51	−1.3	
Dynamic range (see Note 7)	T_A = 25°C			86			84		dB
Stop-band frequency attentuation at 2 f_{co}	$f_{clock} \le 250$ kHz		24	25		24	25		dB
DC voltage amplification	$f_{clock} \le 250$ kHz, RS ≤ 2 kΩ		−0.15	0	0.15	−0.15	0	0.15	dB
Peak-to-peak clock feedthrough voltage	T_A = 25°C			7			7		mV

† All typical values are at T_A = 25°C.

NOTES: 2. Above 250 kHz, the input clock duty cycle should be 50% to allow the operational amplifiers the maximum time to settle while processing analog samples.

5. The frequency responses at f are referenced to a dc gain of 0 dB.

7. The dynamic range is referenced to 2.82 V rms (4 V peak) where the wideband noise over a 30-kHz bandwidth is typically 142 μV rms for the TLC04/MF4A-50 and 178 μV rms for the TLC14/MF4A-100.

TYPICAL CHARACTERISTICS

FILTER OUTPUT
vs
SUPPLY VOLTAGE V_{CC+} RIPPLE FREQUENCY

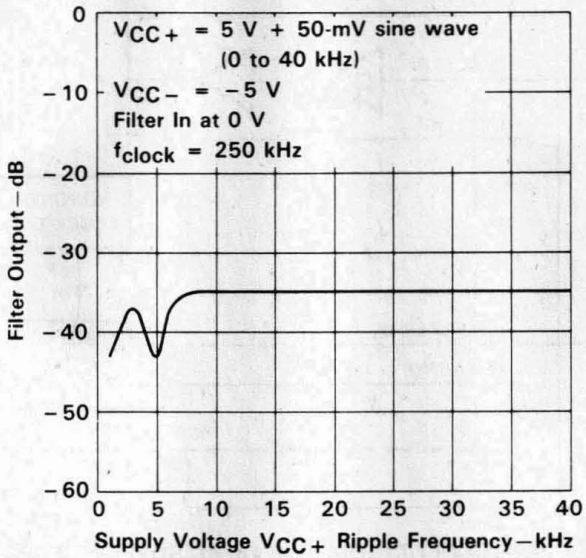


FIGURE 1

FILTER OUTPUT
vs
SUPPLY VOLTAGE V_{CC-} RIPPLE FREQUENCY

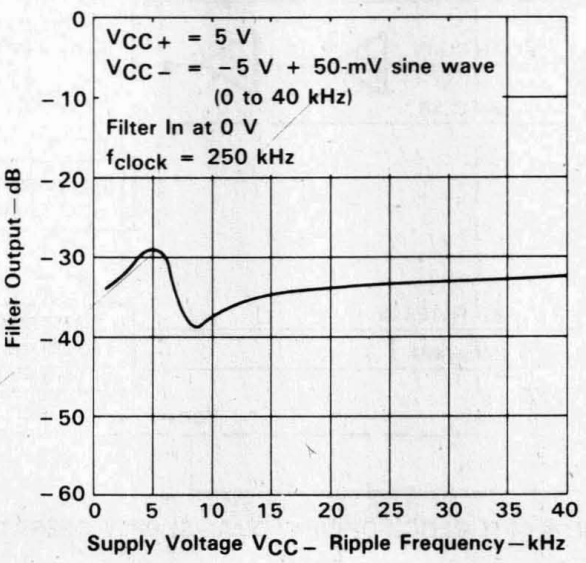


FIGURE 2

TYPICAL APPLICATION DATA

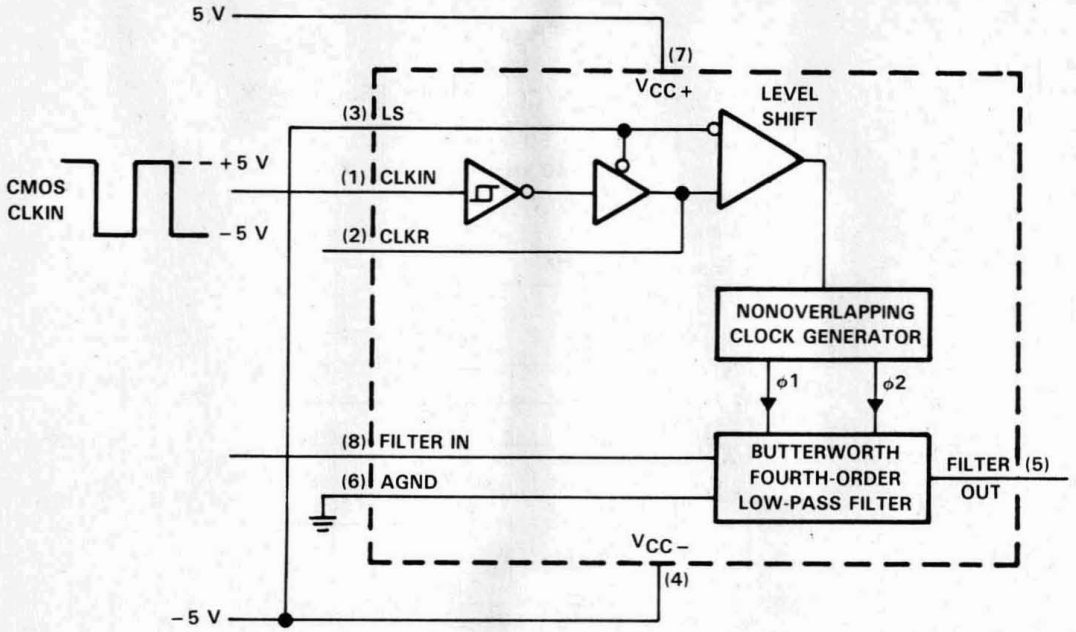


FIGURE 3. CMOS-CLOCK-DRIVEN, DUAL-SUPPLY OPERATION

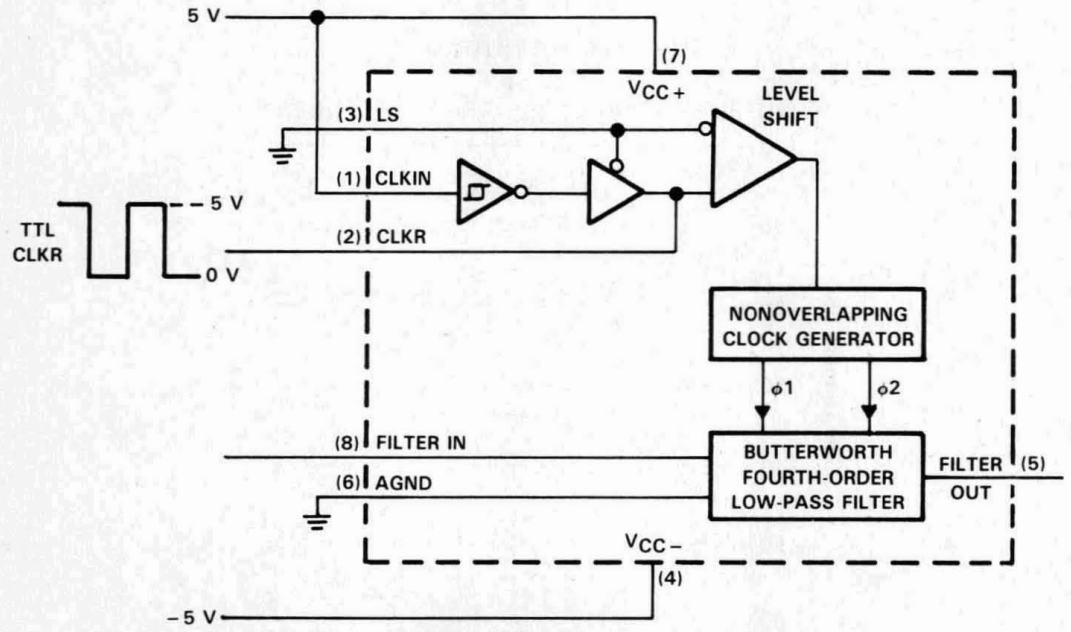
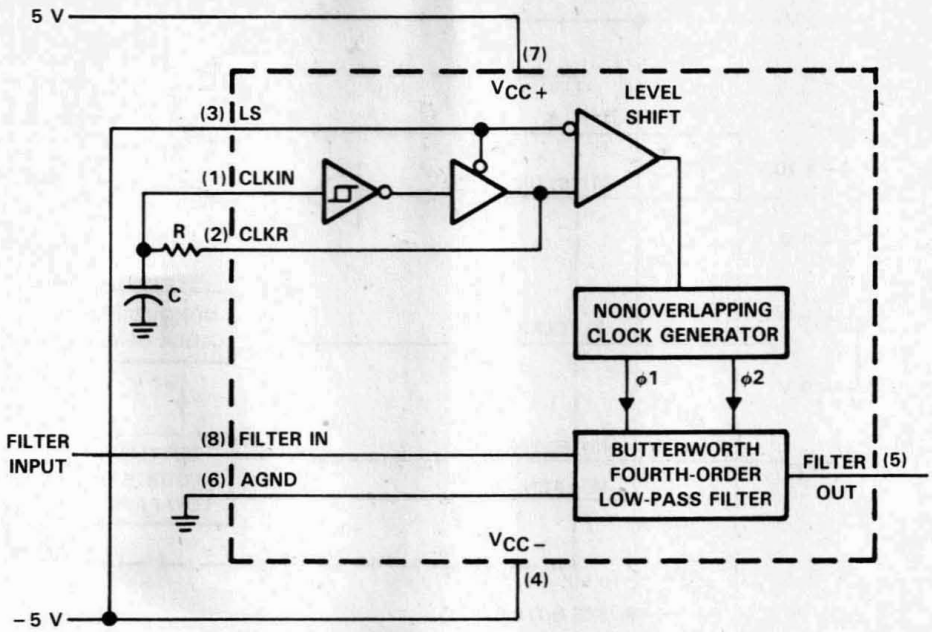


FIGURE 4. TTL-CLOCK-DRIVEN, DUAL-SUPPLY OPERATION

TYPICAL APPLICATION DATA



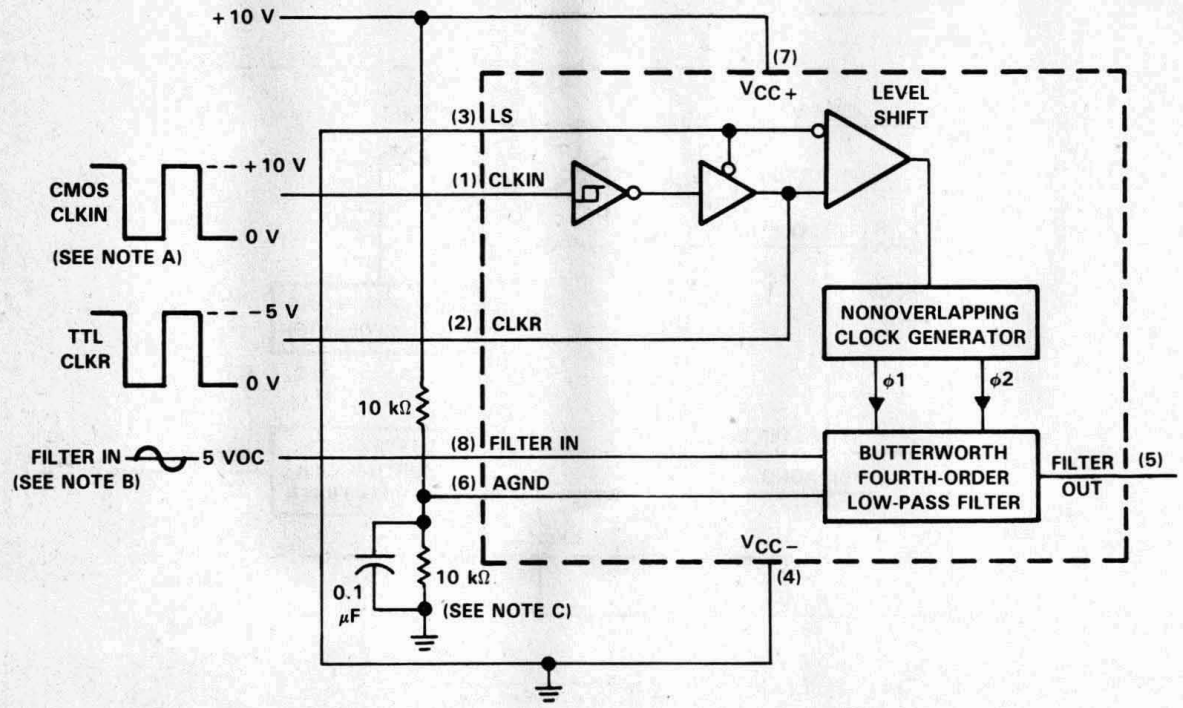
$$f_{clock} = \frac{1}{RC \times \ln\left[\left(\frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}\right)\left(\frac{V_{T+}}{V_{T-}}\right)\right]}$$

For $V_{CC} = 10$ V,

$$f_{clock} = \frac{1}{1.69\ RC}$$

FIGURE 5. SELF-CLOCKING THROUGH SCHMITT-TRIGGER OSCILLATOR, DUAL-SUPPLY OPERATION

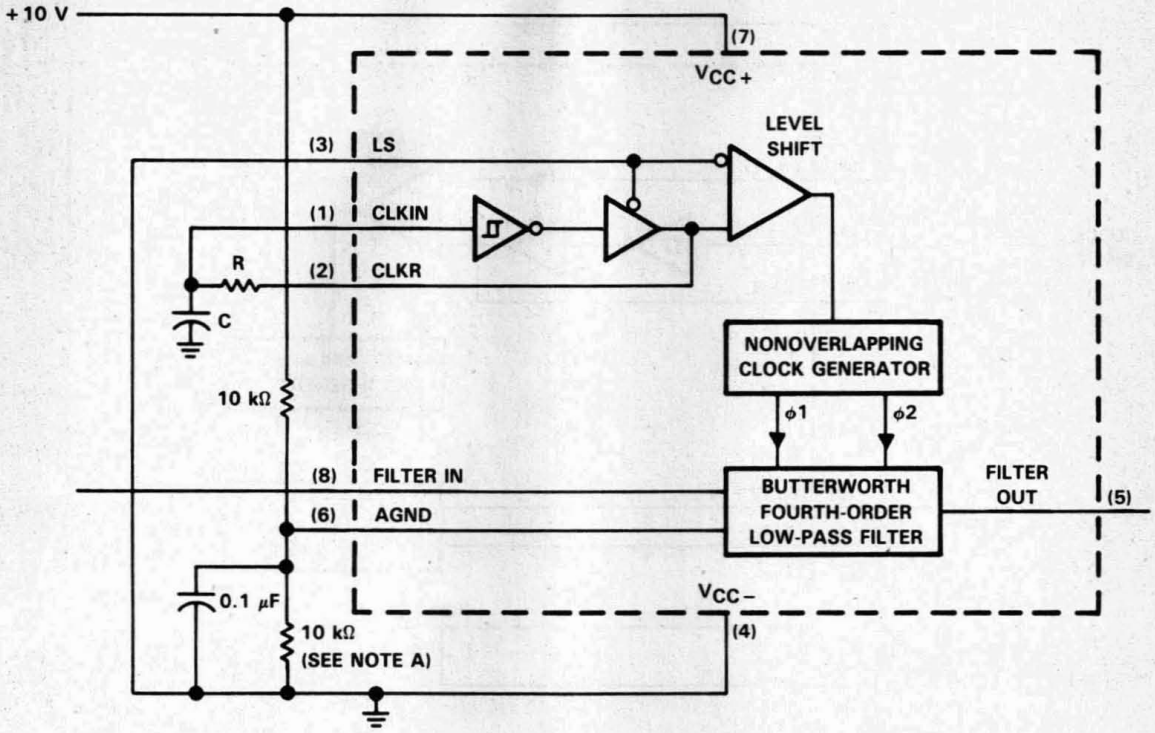
TYPICAL APPLICATION DATA



NOTES: A. The external clock used must be of CMOS level because the clock is input to a CMOS Schmitt trigger.
B. The Filter input signal should be dc-biased to mid-supply or ac-coupled to the terminal.
C. The AGND terminal must be biased to mid-supply.

FIGURE 6. EXTERNAL-CLOCK-DRIVEN SINGLE-SUPPLY OPERATION

TYPICAL APPLICATION DATA



$$f_{clock} = \frac{1}{RC \times \ln\left[\left(\frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}\right)\left(\frac{V_{T+}}{V_{T-}}\right)\right]}$$

For $V_{CC} = 10$ V,

$$f_{clock} = \frac{1}{1.69\ RC}$$

NOTE A: The AGND terminal must be biased to mid-supply.

FIGURE 7. SELF-CLOCKING THROUGH SCHMITT-TRIGGER OSCILLATOR, SINGLE-SUPPLY OPERATION

TYPICAL APPLICATION DATA

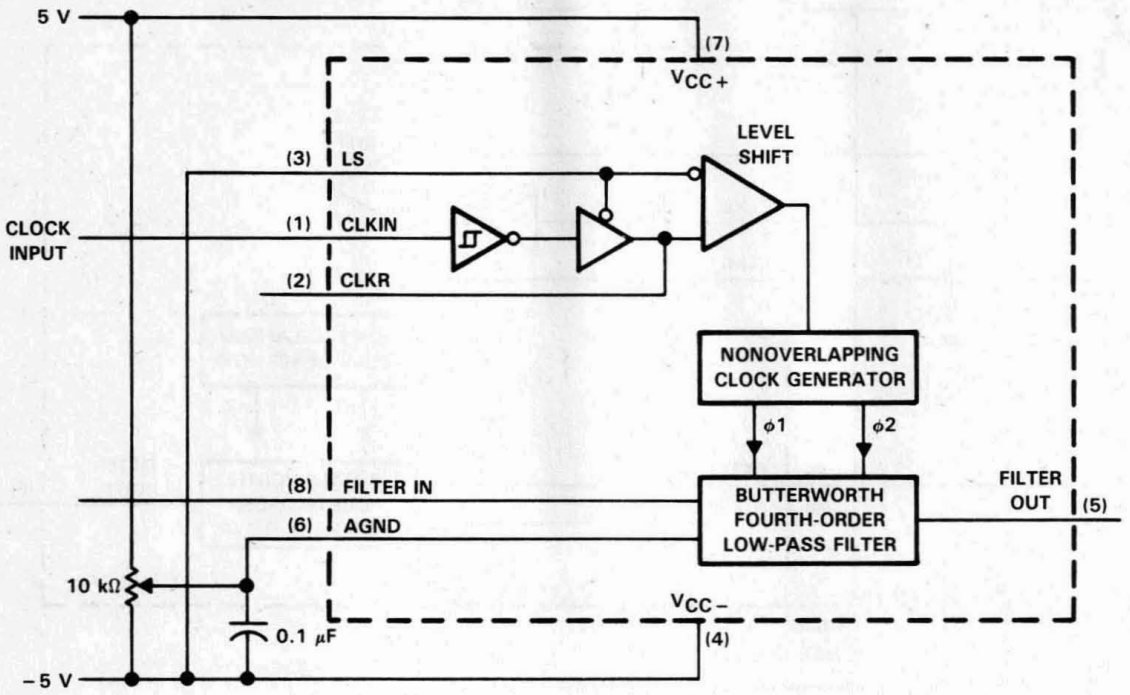


FIGURE 8. DC OFFSET ADJUSTMENT

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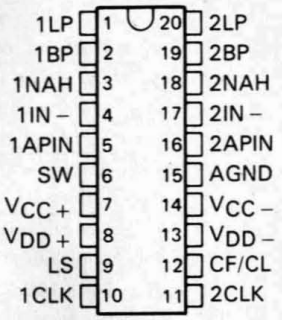
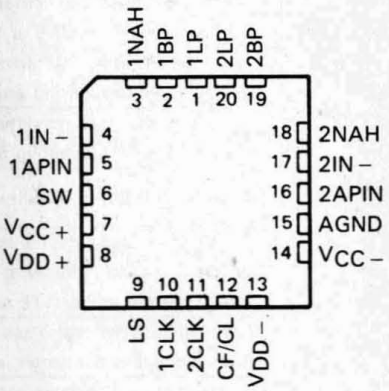
D2952, AUGUST 1986—REVISED NOVEMBER 1988

- **Maximum Clock to Center-Frequency Ratio Error**
  TLC10 . . . ±0.6%
  TLC20 . . . ±1.5%
- **Filter Cutoff Frequency Stability Dependent Only on External-Clock Frequency Stability**
- **Minimum Filter Response Deviation Due to External Component Variations over Time and Temperature**
- **Critical-Frequency Times Q Factor Range Up to 200 kHz**
- **Critical-Frequency Operation Up to 30 kHz**
- **Designed to be Interchangeable with:**
  National MF10
  Maxim MF10
  Linear Technology LTC1060

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



FN CHIP CARRIER PACKAGE
(TOP VIEW)



description

The TLC10/MF10A and TLC20/MF10C are monolithic general-purpose switched-capacitor CMOS filters each containing two independent active-filter sections. Each device facilitates configuration of Butterworth, Bessel, Cauer, or Chebyshev filter design.

Filter features include cutoff frequency stability that is dependent only on the external clock frequency stability and minimal response deviation over time and temperature. Features also include a critical-frequency times filter quality (Q) factor range of up to 200 kHz.

With external clock and resistors, each filter section can be used independently to produce various second-order functions or both sections can be cascaded to produce fourth-order functions. For functions greater than fourth-order, ICs can be cascaded.

The TLC10/MF10A and TLC20/MF10C are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	MAX f_{clock}/fc ERROR	PACKAGE	
		CHIP CARRIER (FN)	PLASTIC DIP (N)
0°C to 70°C	±0.6%	TLC10CFN or MF10ACFN	TLC10CN or MF10ACN
	±1.5%	TLC20CFN or MF10CCFN	TLC20CN or MF10CCN

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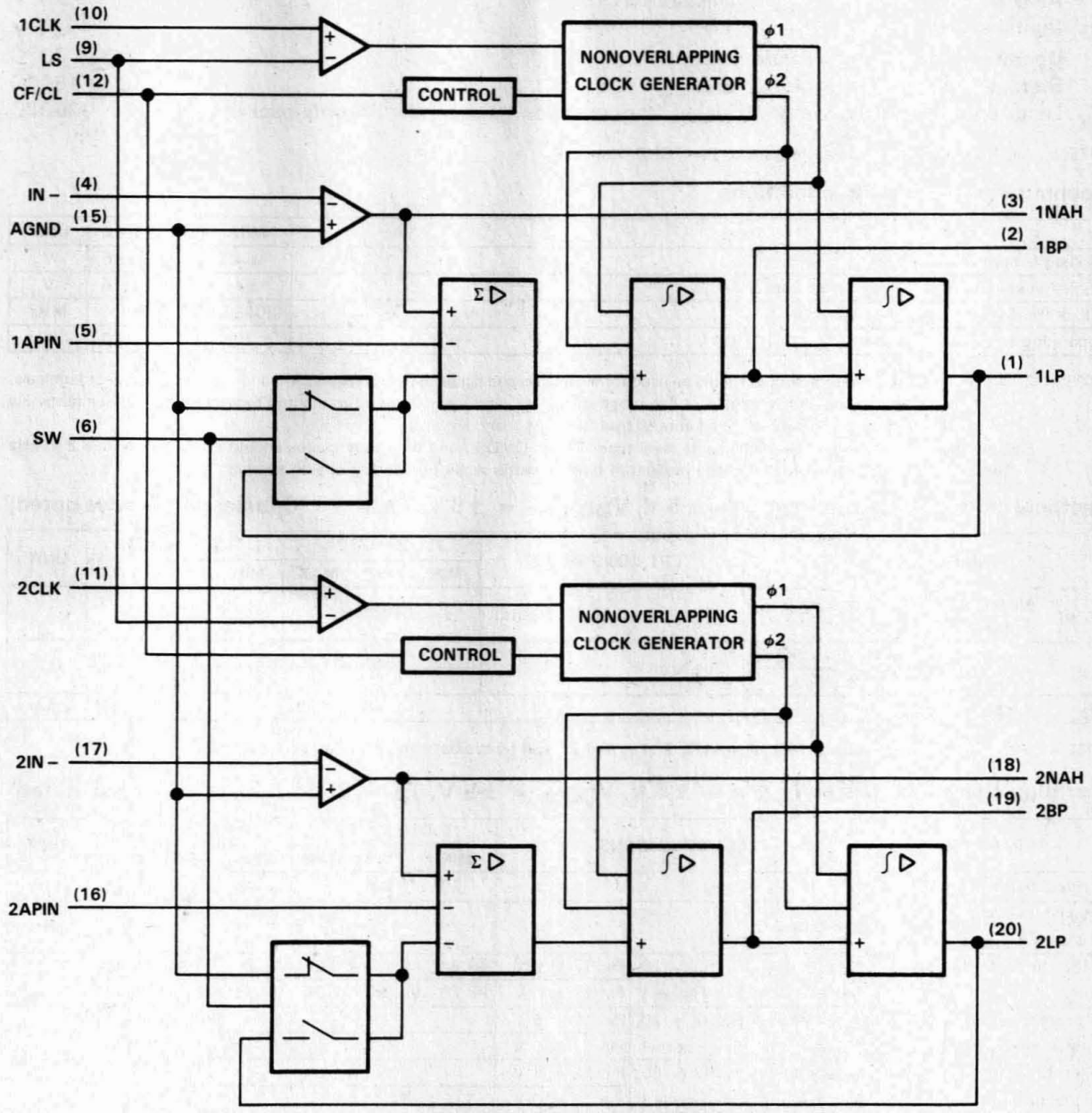
PIN NAME	PIN NO.	I/O	DESCRIPTION
AGND	15	I	Analog Ground — The noninverting inputs to the input operational amplifiers of both filter sections. This terminal should be at ground for dual supplies or at mid-supply level for single-supply operation.
1APIN 2APIN	5 16	I	All-Pass Inputs — The all-pass input to the summing amplifier of each respective filter section used for all-pass filter applications in configuration modes 1a, 4, 5, and 6. This terminal should be driven from a source having an impedance of less than 1 kΩ. In all other modes, this terminal is grounded. See Typical Application Data.
1BP 2BP	2 19	O	Band-Pass Outputs — The band-pass output of each respective filter section provides the second-order band-pass filter functions.
CF/CL	12	I	Center Frequency/Current Limit — This input terminal provides the option to select the input-clock-to-center-frequency ratio of 50:1 or 100:1 or to limit the current of the IC. For a 50:1 ratio, the CF/CL terminal is set to V_{DD+}. For a 100:1 ratio, the CF/CL terminal is set to ground for dual supplies or to mid-supply level for single-supply operation. For current limiting, the CF/CL terminal is set to V_{DD-}. This aborts filtering and limits the IC current to 0.5 milliamperes.
1CLK 2CLK	10 11	I	Clock Inputs — The clock input to the two-phase nonoverlapping generator of each respective filter section is used to generate the center frequency of the complex pole pair second-order function. Both clocks should be of the same level (TTL or CMOS) and have duty cycles close to 50%, especially when clock frequencies (f_{clock}) greater than 200 kHz are used. At this duty cycle, the operational amplifiers have the maximum time to settle while processing analog samples.
1IN− 2IN−	4 17	I	Inverting Inputs — The inverting input side of the input operational amplifier whose output drives the summing amplifier of each respective filter section.
1LP 2LP	1 20	O	Low-Pass Outputs — The low-pass outputs of the second-order filters.
LS	9	I	Level Shift — This terminal accommodates various input clock levels of bipolar (CMOS) or unipolar (TTL or other clocks) to function with single or dual supplies. For CMOS (±5-volt) clocks, V_{DD-} or ground is applied to the LS terminal. For TTL and other clocks, ground is applied to the LS terminal.
1NAH 2NAH	3 18	O	Notch, All-Pass, or High-Pass Outputs — The output of each respective filter section can be used to provide either a second-order notch, all-pass, or high-pass output filter function, depending on circuit configuration.
SW	6	I	Switch Input — This input terminal is used to control internal switches to connect either the AGND input or the LP output to one of the inputs of the summing amplifier. The terminal controls both independent filter sections and places them in the same configuration simultaneously. If V_{CC-} is applied to the SW terminal, the AGND input terminal will be connected to one of the inputs of each summing amplifier. If V_{CC+} is applied to the SW terminal, the LP output will be connected to one of the inputs of the summing amplifier.
V_{CC+}	7		Analog positive supply voltage terminal
V_{CC-}	14		Analog negative supply voltage terminal
V_{DD+}	8		Digital positive supply voltage terminal
V_{DD-}	13		Digital negative supply voltage terminal

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Analog supply voltage, $V_{CC\pm}$ (see Note 1) . . . . . ±7 V
Digital supply voltage, $V_{DD\pm}$ . . . . . ±7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: FN or N package . . . . . 260°C

NOTE 1: All voltage values are with respect to the AGND terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Analog supply voltage, $V_{CC\pm}$, (see Note 2)	±4	±5	±6	V
Digital supply voltage, $V_{DD\pm}$, (see Note 2)	±4	±5	±6	V
Clock frequency, f_{clock}, (see Note 3)	0.008		1.0	MHz
Operating free-air temperature, T_A	0		70	°C

NOTES: 2. A common supply voltage source should be used for the analog and digital supply voltages. Although each has separate terminals, they are connected together internally at the substrate. V_{CC+} and V_{DD+} can be connected together at the device terminals or at the supply voltage source. The same is true for V_{CC-} and V_{DD-}.
3. Both input clocks should be of the same level type (TTL or CMOS), and their duty cycles should be at 50% above 200 kHz to allow the operational amplifiers the maximum time to settle while processing analog samples.

electrical characteristics at $V_{CC\pm}$ = ±5 V, $V_{DD\pm}$ + = ±5 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	TLC10/MF10A			TLC20/MF10C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OPP}	Maximum peak-to-peak output voltage swing		R_L = 3.5 kΩ at all outputs	±4	±4.1		±3.8	±3.9		V
I_{OS}	Short-circuit output current, Pins 3 and 18	Source	See Note 4		2			2		mA
		Sink			50			50		
I_{CC}	Supply current				8	10		8	10	mA

NOTE 4: The short-circuit output current for pins 1, 2, 19, and 20 will be typically the same as pins 3 and 18.

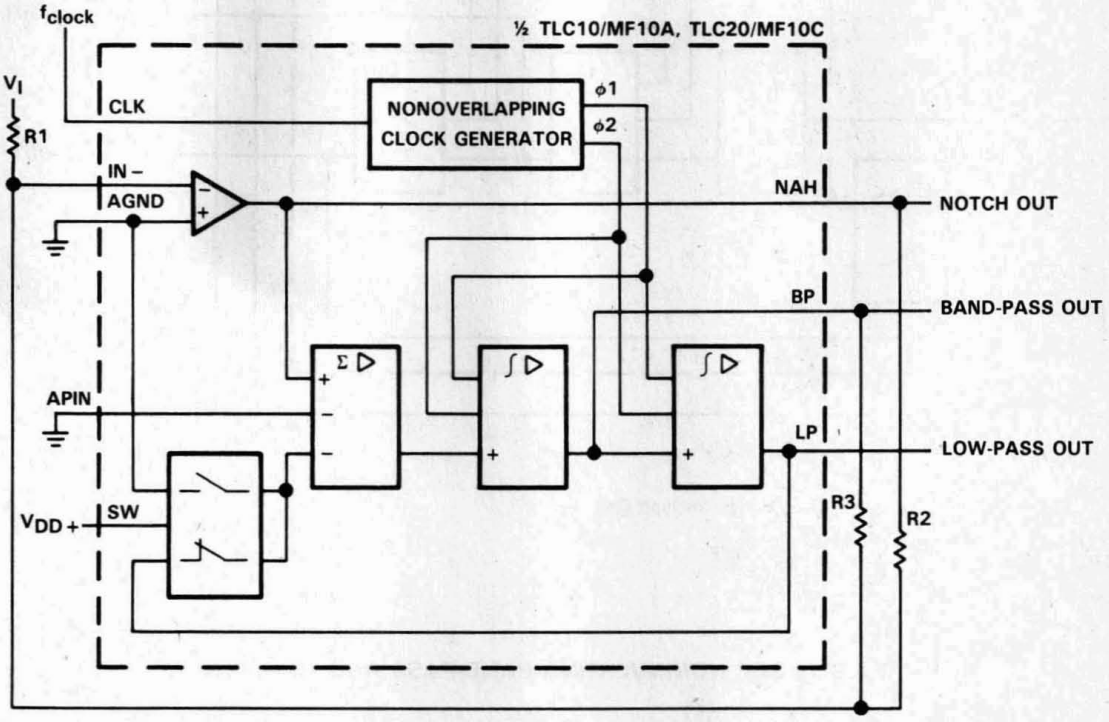
operating characteristics at $V_{CC\pm}$ = ±5 V, $V_{DD\pm}$ = ±5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS			TLC10/MF10A			TLC20/MF10C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Critical-frequency range	$f_o \times Q \leq 200$ kHz			20	30		20	30		kHz
Maximum clock frequency, f_{clock}	See Note 3			1	1.5		1	1.5		MHz
Clock to center-frequency ratio	$f_o \leq 5$ kHz, Mode 1,	R3/R2 = 10, See Figure 1	Pin 12 at 5 V	49.64	49.94	50.24	49.24	49.94	50.64	
			Pin 12 at 0 V	98.75	99.35	99.95	97.86	99.35	100.84	
Temperature coefficient of center frequency	$f_o \leq 5$ kHz, Mode 1,	R3/R2 = 20, See Figure 1	Pin 12 at 5 V		±10			±10		ppm/°C
			Pin 12 at 0 V		±100			±100		
Filter Q (quality factor) deviation from 20	$f_o \leq 5$ kHz, Mode 1,	R3/R2 = 20, See Figure 1	Pin 12 at 5 V		±2%	±4%		±2%	±6%	
			Pin 12 at 0 V		±2%	±3%		±2%	±6%	
Temperature coefficient of measured filter Q	$f_o \leq 5$ kHz, Mode 1	R3/R2 = 20,			±500			±500		ppm/°C
Low-pass output deviation from unity gain	R1 = R2 = 10 kΩ Mode 1,	See Figure 1				±2%			±2%	
Crosstalk attenuation					60			60		dB
Clock feedthrough voltage					10			10		mV
Operational amplifier gain-bandwidth product					2.5			2.5		MHz
Operational amplifier slew rate					7			7		V/μs

TYPICAL APPLICATION DATA

modes of operation

The TLC10/MF10A and TLC20/MF10C are switched-capacitor (sampled-data) filters that closely approximate continuous filters. Each filter section is designed to approximate the response of a second-order variable filter. When the sampling frequency is much larger than the frequency band of interest, the sampled-data filter is a good approximation to its continuous time equivalent. In the case of the TLC10/MF10A and TLC20/MF10C, the ratio is about 50:1 or 100:1. To fully describe their transfer function, a time domain approach would be appropriate. Since this may appear cumbersome, the following application examples are based on the well known frequency domain. It should be noted that in order to obtain the actual filter response, the filter's response must be examined in the z-domain.



$f_o = f_{clock}/100$ or $f_{clock}/50$
$f_{notch} = f_o$
$H_{OLP} = -R2/R1$ (as $f \rightarrow 0$)
$H_{OBP} = -R3/R1$ (at $f = f_o$)
H_{ON} = notch gain { as f approaches 0 $-R2/R1$; as f approaches 0.5 f_{clock}
$Q = f_o/BW = R3/R2$

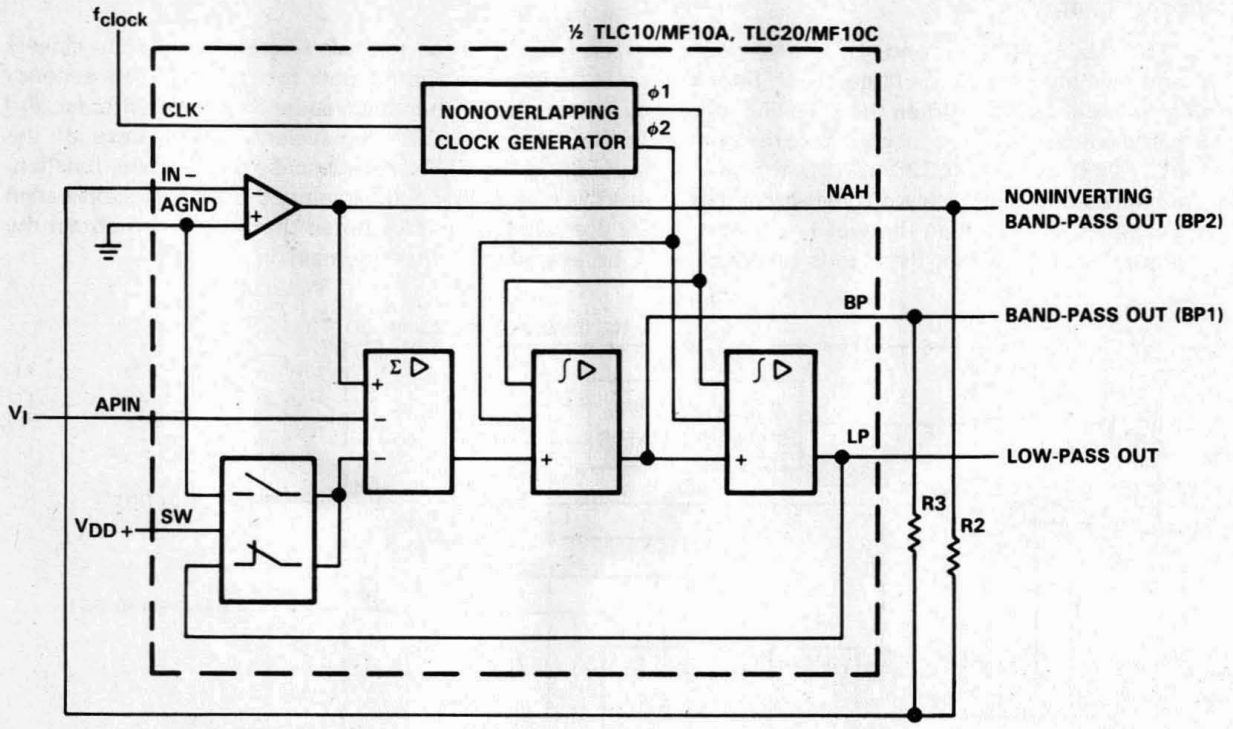
Circuit dynamics:

The following expressions determine the swing at each output as a function of the desired Q of the second-order function.

$H_{OLP} = H_{OBP}/Q$ or $H_{OLP} \times Q = H_{ON} \times Q$
H_{OLP} (peak) $= Q \times H_{OLP}$ (for high Qs)

FIGURE 1. MODE 1 FOR NOTCH, BAND-PASS, AND LOW-PASS OUTPUTS: $f_{notch} = f_o$

TYPICAL APPLICATION DATA

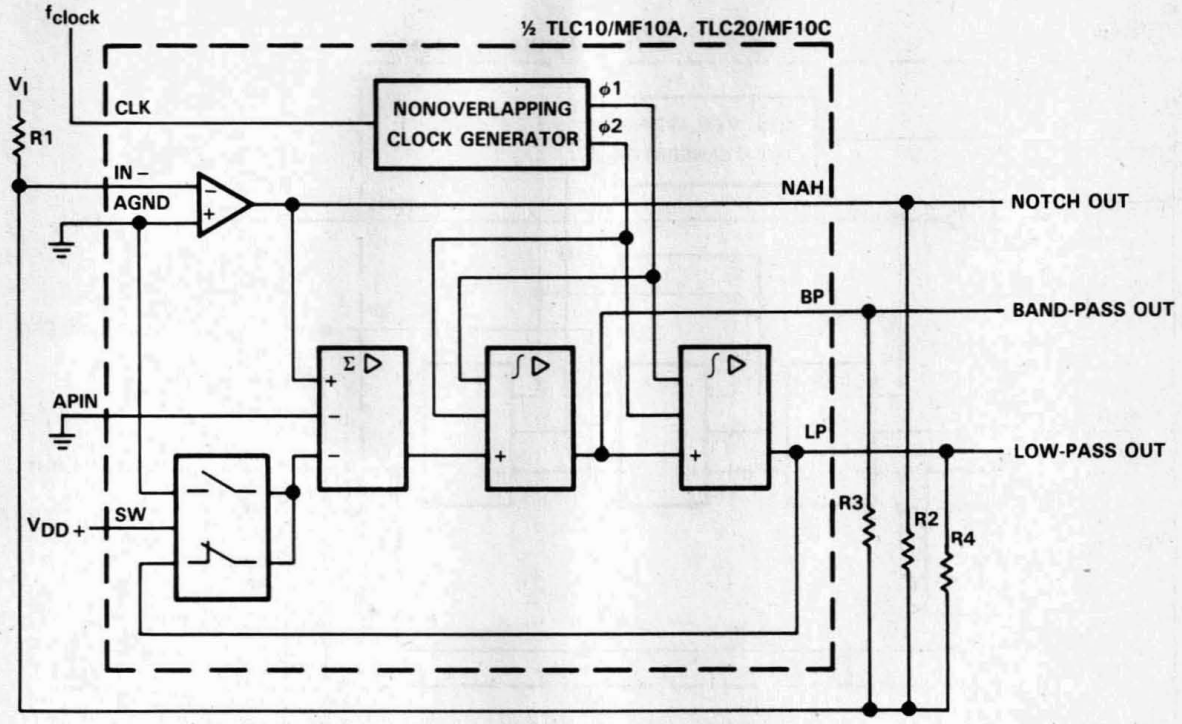


$f_o = f_{clock}/100$ or $f_{clock}/50$
$Q = R3/R2$
$H_{OLP} = -1$ H_{OLP} (peak) = $Q \times H_{OLP}$ (for high Qs)
$H_{OBP1} = -R3/R2$
$H_{OBP2} = 1$ (noninverting)

Circuit dynamics:
$H_{OBP1} = Q$

FIGURE 2. MODE 1a FOR NONINVERTING BAND-PASS AND LOW-PASS OUTPUTS

TYPICAL APPLICATION DATA



$f_o = f_{notch} \times \sqrt{R2/R4 + 1}$

$f_{notch} = f_{clock}/100$ or $f_{clock}/50$

$$Q = \frac{\sqrt{R2/R4 + 1}}{R2/R3}$$

$$H_{OLP} \text{ (as f approaches 0)} = \frac{-R2/R1}{R2/R4 + 1}$$

H_{OBP} (at $f = f_o$) $= -R3/R1$

$$H_{ON1} \text{ (as f approaches 0)} = \frac{-R2/R1}{R2/R4 + 1}$$

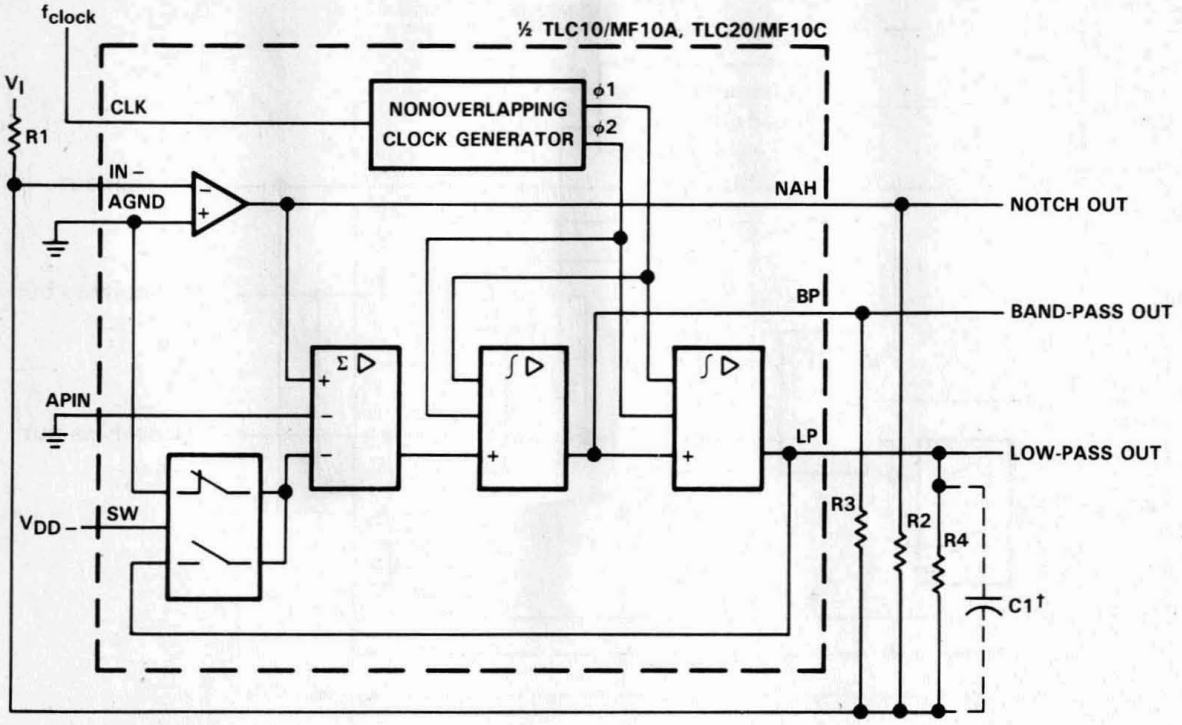
H_{ON2} (as f approaches 0.5 f_{clock}) $= -R2/R1$

Circuit dynamics:

$$H_{OBP} = Q\sqrt{H_{OLP} \times H_{ON2}} = Q\sqrt{H_{ON1} \times H_{ON2}}$$

FIGURE 3. MODE 2 FOR NOTCH 2, BAND-PASS, AND LOW-PASS OUTPUTS: $f_{notch} < f_o$

TYPICAL APPLICATION DATA



f_o = (f_{clock}/100 or f_{clock}/50) $\sqrt{R2/R4}$

Q = $\sqrt{R2/R4}$ × R3/R2

H_{OHP} (as f approaches 0.5 f_{clock}) = −R2/R1

H_{OLP} (as f approaches 0) = −R4/R1

H_{OBP} (at f = f_o) = −R3/R1

Circuit dynamics:

R2/R4 = H_{OHP}/H_{OLP}: H_{OBP} = $\sqrt{H_{OHP} \times H_{OLP}}$ × Q

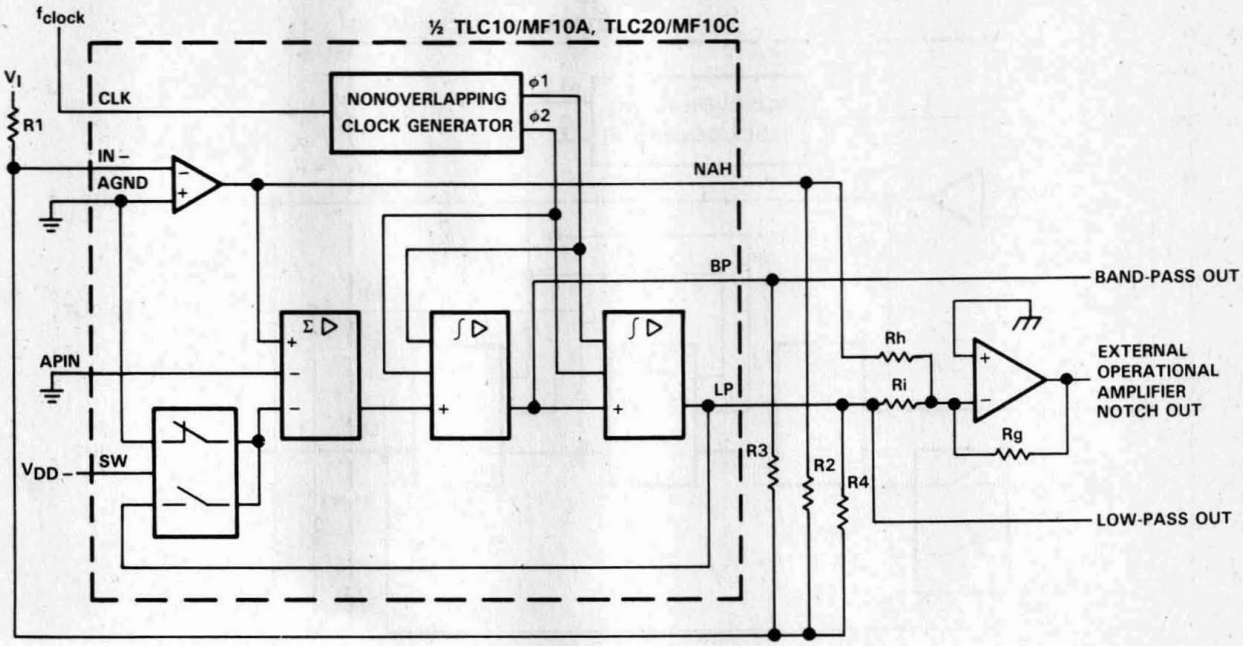
H_{OLP} (peak) = Q × H_{OLP} (for high Qs)

H_{OHP} (peak) = Q × H_{OHP} (for high Qs)

†In this mode, the feedback loop is closed around the input summing amplifier; the finite GBW product of this operational amplifier will cause a slight Q enhancement. If this is a problem, connect a low-value capacitor (10 pF to 100 pF) across R4 to provide some phase lead.

FIGURE 4. MODE 3 FOR HIGH-PASS, BAND-PASS, AND LOW-PASS OUTPUTS

TYPICAL APPLICATION DATA



$f_o = (f_{clock}/100 \text{ or } f_{clock}/50)\sqrt{R2/R4}$

$Q = \sqrt{R2/R4} \times R3/R2$

$H_{OHP} = -R2/R1$

$H_{OBP} = -R3/R1$

$H_{OLP} = -R4/R1$

$f_{notch} = (f_{clock}/100 \text{ or } f_{clock}/50)\sqrt{Rh/Ri}$

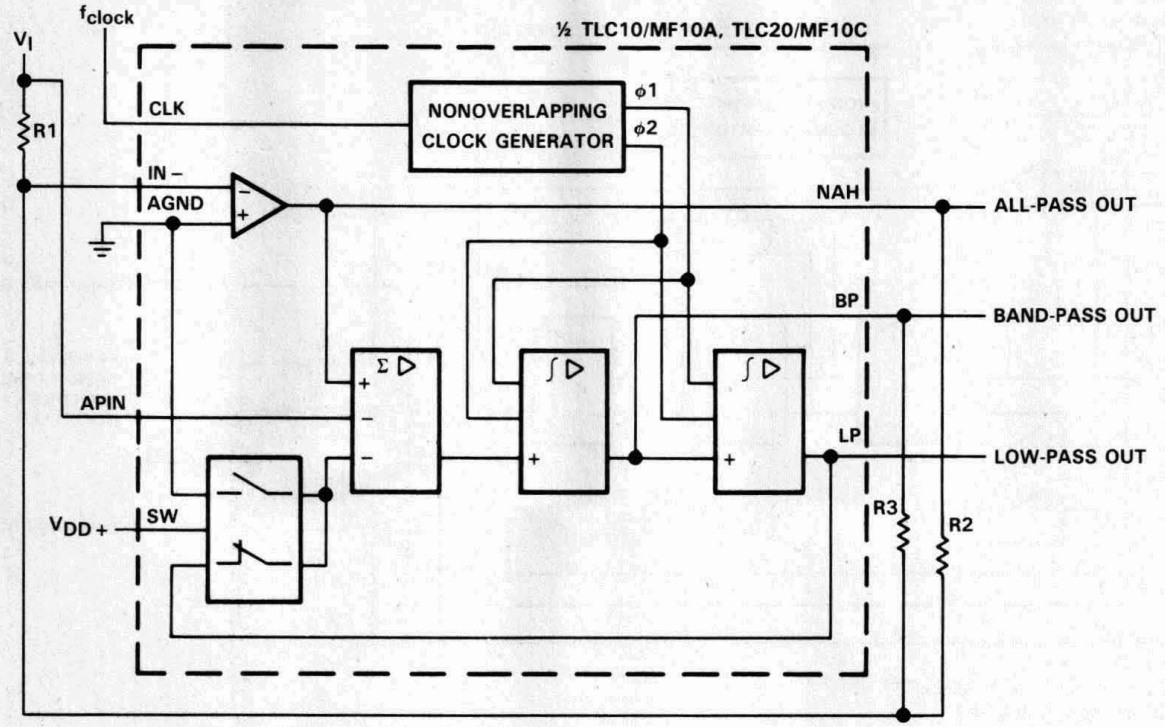
H_{ON} (at $f = f_o$) = $| Q (Rg/Ri \times H_{OLP} - Rg/Rh \times HOHP) |$

H_{ON1} (as f approaches 0) = $Rg/Ri \times H_{OLP}$

H_{ON2} (as f approaches 0.5 f_{clock}) = $-Rg/Rh \times H_{OHP}$

FIGURE 5. MODE 3a FOR HIGH-PASS, BAND-PASS, LOW-PASS, AND NOTCH OUTPUTS WITH EXTERNAL OPERATIONAL AMPLIFIER

TYPICAL APPLICATION DATA



$f_o = f_{clock}/100$ or $f_{clock}/50$

$f_z = f_o$†

$Q = f_o/BW = R3/R2$

$Q_z = R3/R1$

H_{OAP} (at $0 \le f \le 0.5\ f_{clock}$) $= -R2/R1 = -1$
(for AP output R1 = R2)

H_{OLP} (as f approaches 0) $= -(R2/R1 + 1) = -2$

H_{OBP} (at $f = f_o$) $= -R3/R2\ (R2/R1 + 1) = -2\ (R3/R2)$

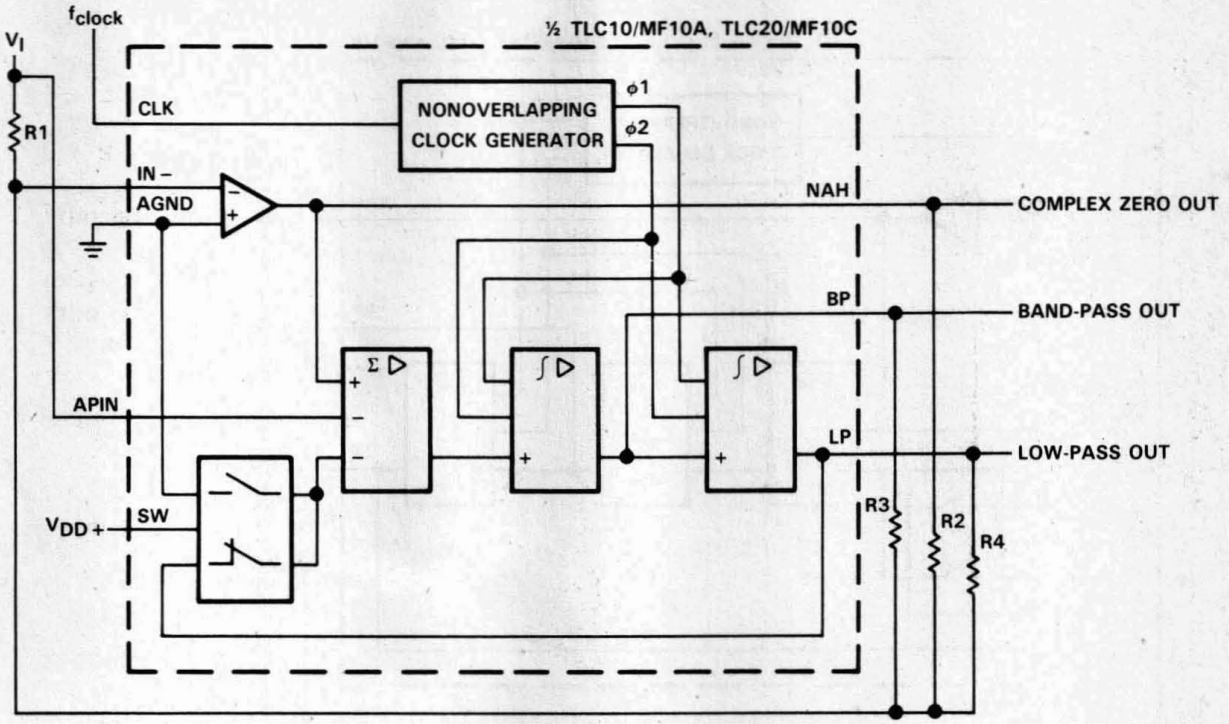
Circuit dynamics:

$$H_{OBP} = H_{OLP} \times Q = (H_{OAP} + 1)\ Q$$

†Due to the sampled-data nature of the filter, a slight mismatch of f_z and f_o occurs causing a 0.4-dB peaking around f_o of the all-pass filter amplitude response (which theoretically should be a straight line). If this is unacceptable, Mode 5 is recommended.

FIGURE 6. MODE 4 FOR ALL-PASS, BAND-PASS, AND LOW-PASS OUTPUTS

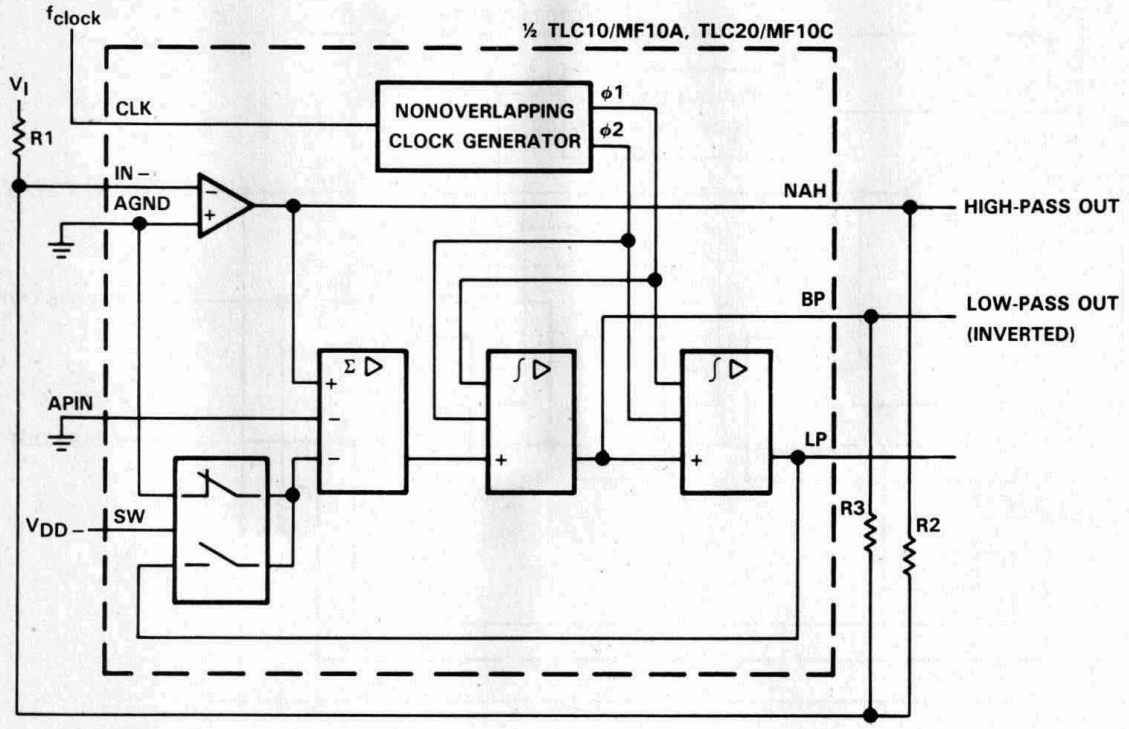
TYPICAL APPLICATION DATA



$f_o = \sqrt{R2/R4 + 1} \times (f_{clock}/100 \text{ or } f_{clock}/50)$
$f_z = \sqrt{1 - R1/R4} \times (f_{clock}/100 \text{ or } f_{clock}/50)$
$Q = \sqrt{R2/R4 + 1} \times R3/R2$
$Q_z = \sqrt{1 - R1/R4} \times R3/R1$
H_{OZ1} (as f approaches 0) = R2 (R4 – R1)/R1 (R2 + R4)
H_{OZ2} (as f approaches 0.5 f_{clock}) = R2/R1
$H_{OBP} = (R2/R1 + 1) \times R3/R2$
$H_{OLP} = (R2 + R1)/(R2 + R4) \times R4/R1$

FIGURE 7. MODE 5 FOR NUMERATOR COMPLEX ZEROS, BAND-PASS, AND LOW-PASS OUTPUTS

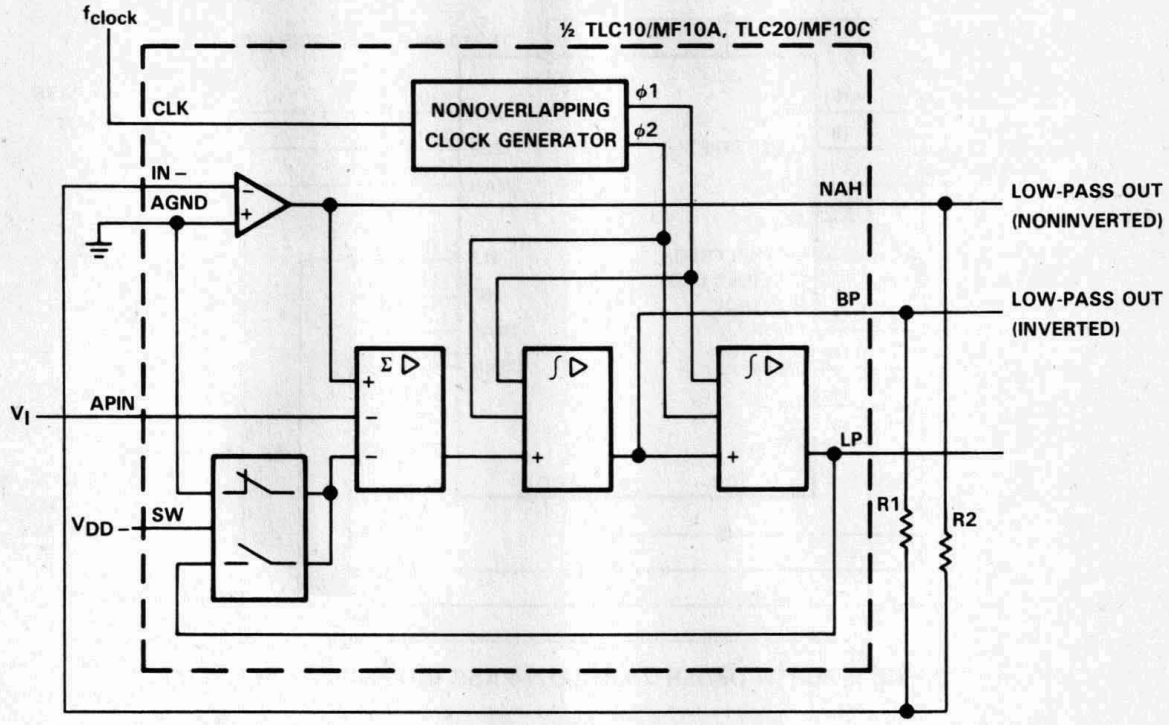
TYPICAL APPLICATION DATA



f_c = R2/R3 (f_{clock}/100 or f_{clock}/50)
H_{OLP} = –R3/R1
H_{OHP} = –R2/R1

FIGURE 8. MODE 6 FOR SINGLE-POLE HIGH-PASS AND LOW-PASS OUTPUT

TYPICAL APPLICATION DATA



f_c = R2/R3 × (f_{clock}/100 or f_{clock}/50)
H_{OLP1} = 1 (noninverting)
H_{OLP2} = –R3/R2

FIGURE 9. MODE 6a FOR SINGLE-POLE LOW-PASS OUTPUT (INVERTED AND NONINVERTED)

TYPICAL APPLICATION DATA

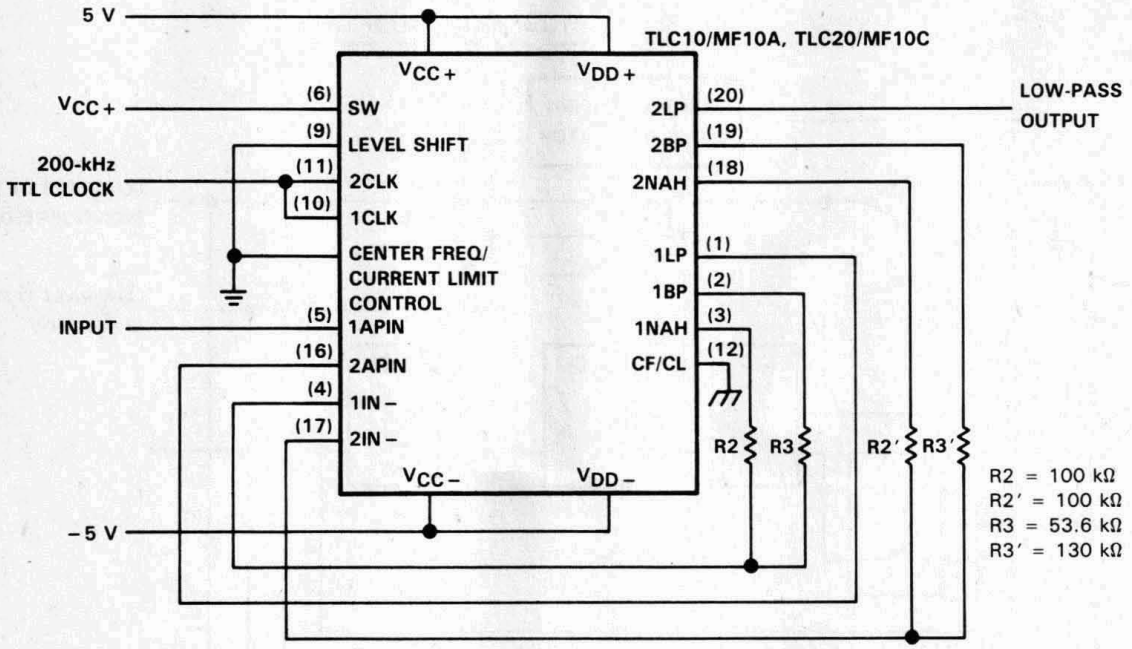
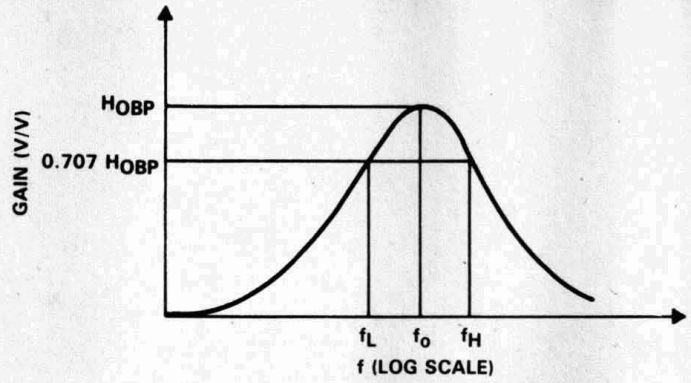


FIGURE 10. FOURTH-ORDER 2-kHz LOW-PASS BUTTERWORTH FILTER

filter terminology

f_c	The cutoff frequency of the low-pass or high-pass filter output
f_{clock}	The input clock frequency to the device
f_{notch}	The notch frequency of the notch output
f_o	The center frequency of the complex pole pair second-order function
f_z	The center frequency of the complex zero pair
H_{OBP}	The band-pass output voltage gain (V/V) at the band-pass center frequency
H_{OHP}	The high-pass output voltage gain (V/V) as the frequency approaches 0.5 f_{clock}
H_{OLP}	The low-pass output voltage gain (V/V) as the frequency approaches 0
H_{ON}	The notch output voltage gain (V/V) at the notch frequency
H_{ON1}	The low-side notch output voltage gain as the frequency approaches 0
H_{ON2}	The high-side notch output voltage gain as the frequency approaches 0.5 f_{clock}
H_{OZ1}	Gain at complex zero output (as $f \rightarrow 0$ Hz)
H_{OZ2}	Gain at complex zero output (as f approaches 0.5 f_{clock})
Q	The quality factor of the complex pole pair second-order function. Q is the ratio of f_o to the 3-dB bandwidth of the band-pass output. The value of Q also affects the possible peaking of the low-pass and high-pass outputs.
Q_z	The quality factor of the complex zero pair, if such a complex pair exists. This parameter is used when an all-pass filter output is desired.

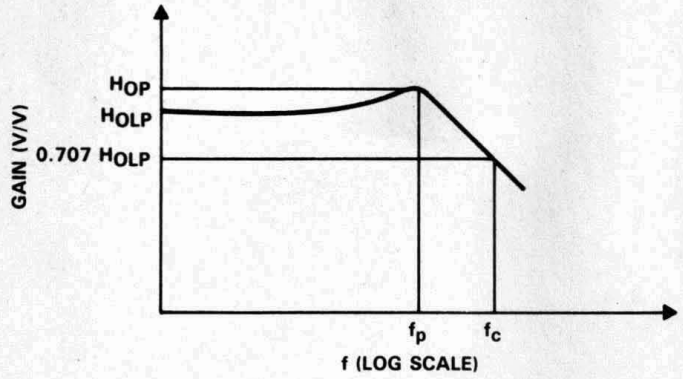


$$Q = \frac{f_o}{f_H - f_L} \; ; \; f_o = \sqrt{f_L f_H}$$

$$f_L = f_o \left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1} \right)$$

$$f_H = f_o \left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1} \right)$$

FIGURE 11. BAND-PASS OUTPUT

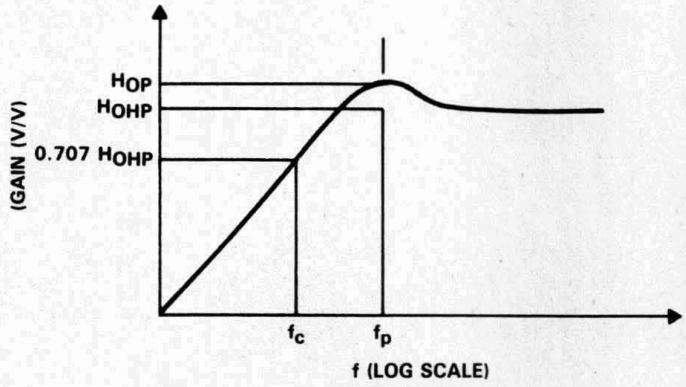


$$f_c = f_o \times \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}$$

$$f_p = f_o \sqrt{1 - \frac{1}{2Q^2}}$$

$$H_{OP} = H_{OLP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

FIGURE 12. LOW-PASS OUTPUT



$$f_c = f_o \times \left[\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}} \right]^{-1}$$

$$f_p = f_o \times \left[\sqrt{1 - \frac{1}{2Q^2}} \right]^{-1}$$

$$H_{OP} = H_{OHP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

FIGURE 13. HIGH-PASS OUTPUT

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TLC32046

Wide-Band Analog Interface Circuit

Data Manual

TEXAS INSTRUMENTS

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Introduction

The TLC32046 wide-band analog interface circuit (AIC) is a complete analog-to-digital and digital-to-analog interface system for advanced digital signal processors (DSPs) similar to the TMS32020, TMS320C25, and TMS320C30. The TLC32046 offers a powerful combination of options under DSP control: three operating modes (dual-word [telephone interface], word, and byte) combined with two word formats (8 bits and 16 bits) and synchronous or asynchronous operation. It provides a high level of flexibility in that conversion and sampling rates, filter bandwidths, input circuitry, receive and transmit gains, and multiplexed analog inputs are under processor control.

This AIC features a

- band-pass switched-capacitor antialiasing input filter
- 14-bit-resolution A/D converter
- 14-bit-resolution D/A converter
- low-pass switched-capacitor output-reconstruction filter.

The antialiasing input filter comprises eighth-order and fourth-order CC-type (Chebyshev/elliptic transitional) low-pass and high-pass filters, respectively. The input filter is implemented in switched-capacitor technology and is preceded by a continuous time filter to eliminate any possibility of aliasing caused by sampled data filtering. When low-pass filtering is desired, the high-pass filter can be switched out of the signal path. A selectable auxiliary differential analog input is provided for applications where more than one analog input is required.

The output-reconstruction filter is an eighth-order CC-type (Chebyshev/elliptic transitional low-pass filter) followed by a second-order (sin x)/x correction filter and is implemented in switched-capacitor technology. This filter is followed by a continuous-time filter to eliminate images of the sample data signal. The on-board (sin x)/x correction filter can be switched out of the signal path using digital signal processor control.

The A/D and D/A architectures ensure no missing codes and monotonic operation. An internal voltage reference is provided to ease the design task and to provide complete control over the performance of the IC. The internal voltage reference is brought out to pin 8. Separate analog and digital voltage supplies and ground are provided to minimize noise and ensure a wide dynamic range. The analog circuit path contains only differential circuitry to keep noise to a minimum. The exception is the DAC sample-and-hold, which utilizes pseudo-differential circuitry.

The TLC32046C is characterized for operation from 0°C to 70°C, and the TLC32046I is characterized for operation from −40°C to 85°C.

Features

- **Advanced LinCMOS™ Silicon-Gate Process Technology**
- **14-Bit Dynamic Range ADC and DAC**
- **16-Bit Dynamic Range Input With Programmable Gain**
- **Synchronous or Asynchronous ADC and DAC Sampling Rates Up to 25,000 Samples Per Second**
- **Programmable Incremental ADC and DAC Conversion Timing Adjustments**
- **Typical Applications**
  - **Speech Encryption for Digital Transmission**
  - **Speech Recognition and Storage Systems**
  - **Speech Synthesis**
  - **Modems at 8-kHz, 9.6-kHz, and 16-kHz Sampling Rates**
  - **Industrial Process Control**
  - **Biomedical Instrumentation**
  - **Acoustical Signal Processing**
  - **Spectral Analysis**
  - **Instrumentation Recorders**
  - **Data Acquisition**
- **Switched-Capacitor Antialiasing Input Filter and Output-Reconstruction Filter**
- **Three Fundamental Modes of Operation: Dual-Word (Telephone Interface), Word, and Byte**
- **600-mil Wide N Package**
- **Digital Output in Twos Complement Format**

FUNCTION TABLE

DATA COMMUNICATIONS FORMAT	SYNCHRONOUS (CONTROL REGISTER BIT D5 = 1)	ASYNCHRONOUS (CONTROL REGISTER BIT D5 = 0)	FORCING CONDITION	DIRECT INTERFACE
16-bit format	Dual-word (telephone interface) mode	Dual-word (telephone interface) mode	Pin 13 = 0 to 5 V Pin 1 = 0 to 5 V	TMS32020, TMS320C25, TMS320C30
16-bit format	Word mode	Word mode	Pin 13 = V_{CC-} (–5 V nom) Pin 1 = V_{CC+} (+5 V nom)	TMS32020, TMS320C25, TMS320C30, indirect interface to TMS320C10.
8-bit format (2 bytes required)	Byte mode	Byte mode	Pin 13 = V_{CC-} (–5 V nom) Pin 1 = V_{CC-} (–5 V nom)	TMS320C17

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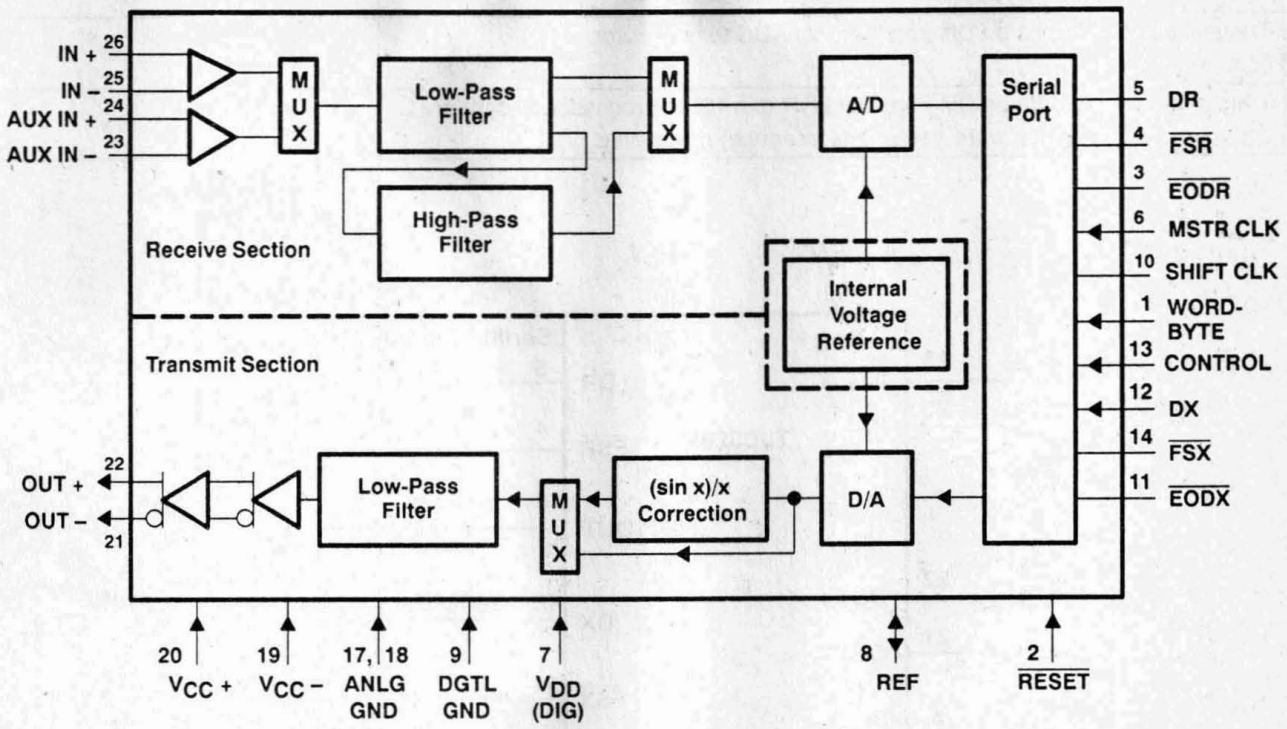
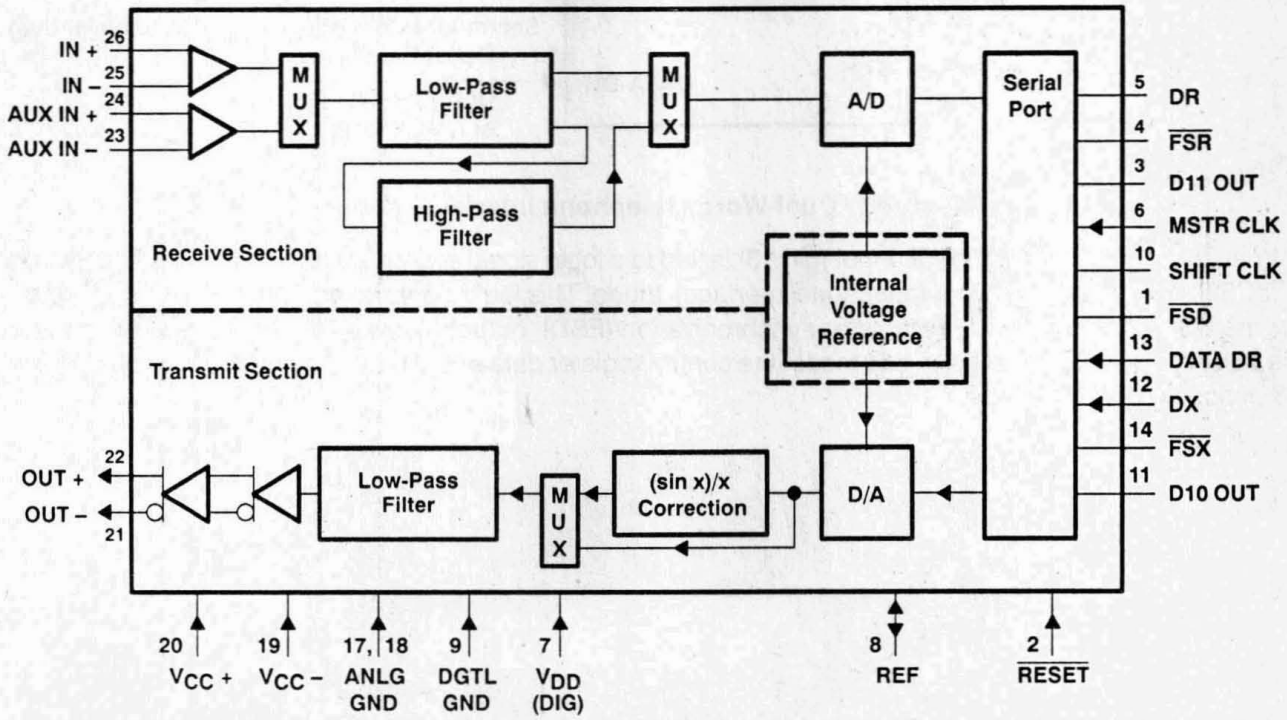
Functional Block Diagrams

WORD OR BYTE MODE



DUAL-WORD (TELEPHONE INTERFACE) MODE



FRAME SYNCHRONIZATION FUNCTIONS

TLC32046 Function	Frame Sync Output
Receiving serial data on DX from processor to internal DAC	$\overline{FSX}$ low
Transmitting serial data on DR from internal ADC to processor, primary communications	$\overline{FSR}$ low
Transmitting serial data on DR from Data DR (pin 13) to processor, secondary communications in dual-word (telephone interface) mode only	$\overline{FSD}$ (pin 1) low

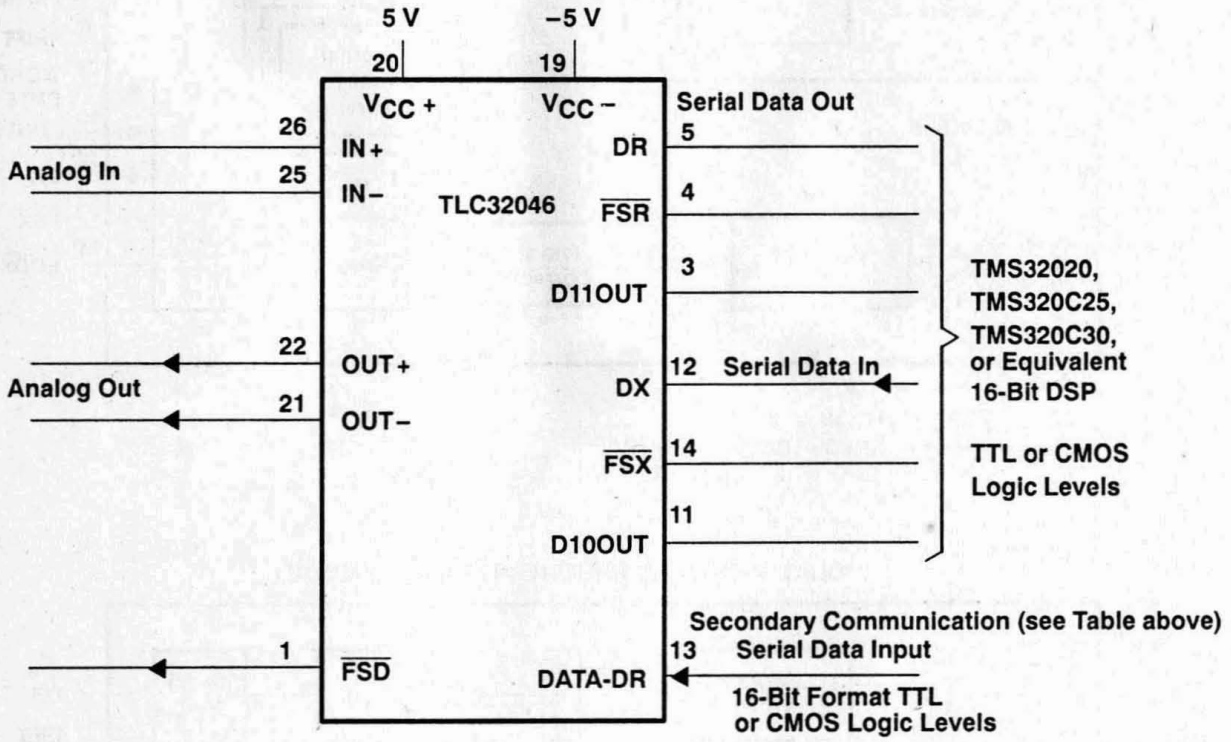


Figure 1. Dual-Word (Telephone Interface) Mode

When the DATA-DR/CONTROL input (pin 13) is tied to a logic signal source varying between 0 and 5 V, the TLC32046 is in the dual-word (telephone interface) mode. This logic signal is routed to the DR line for input to the DSP only when pin 1, data frame synchronization ($\overline{FSD}$), outputs a low level. The $\overline{FSD}$ pulse duration is 16 shift clock pulses. Also, in this mode, the control register data bits D10 and D11 appear on pins 11 and 3, respectively, as outputs.

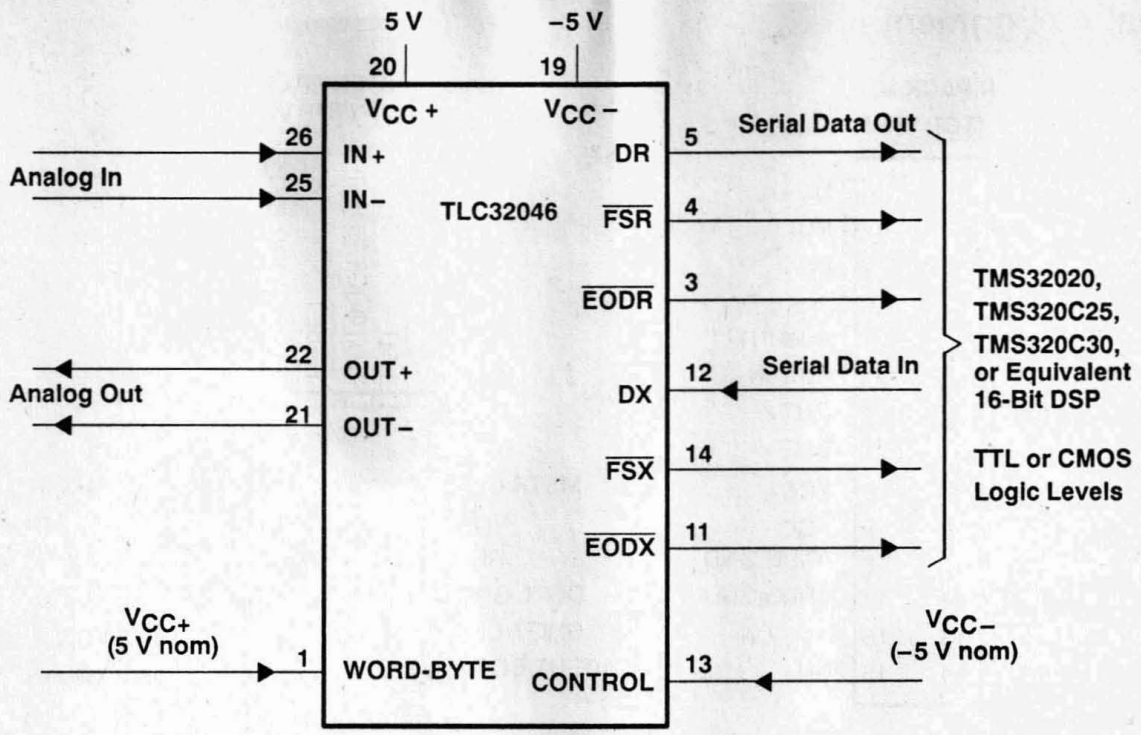


Figure 2. Word Mode

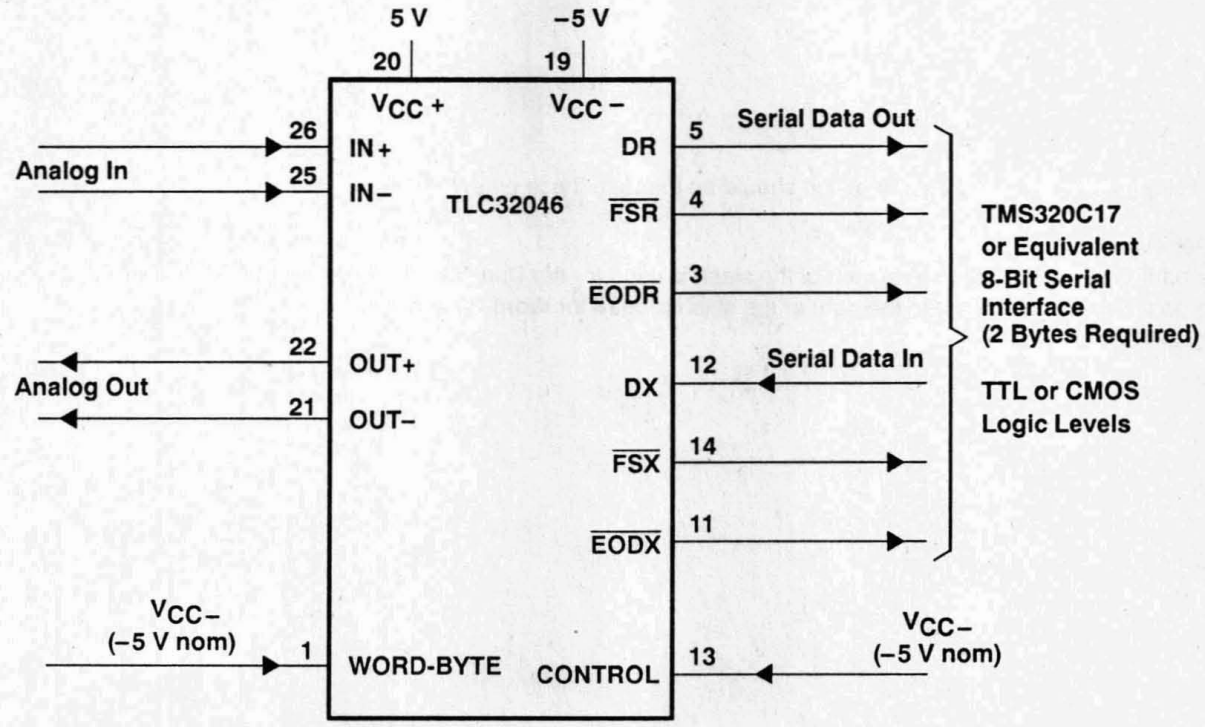
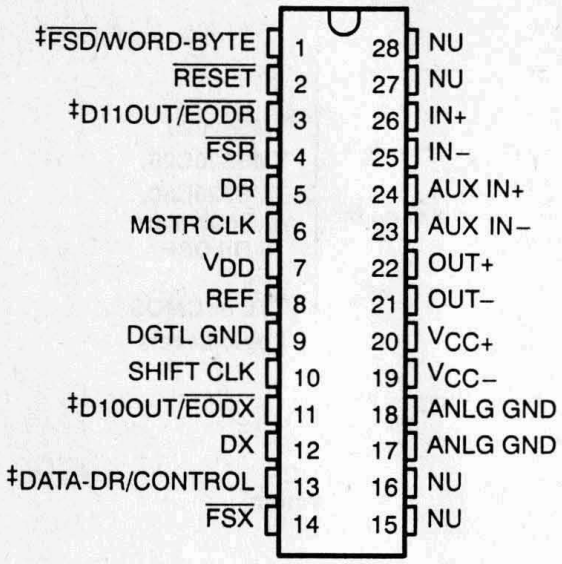


Figure 3. Byte Mode

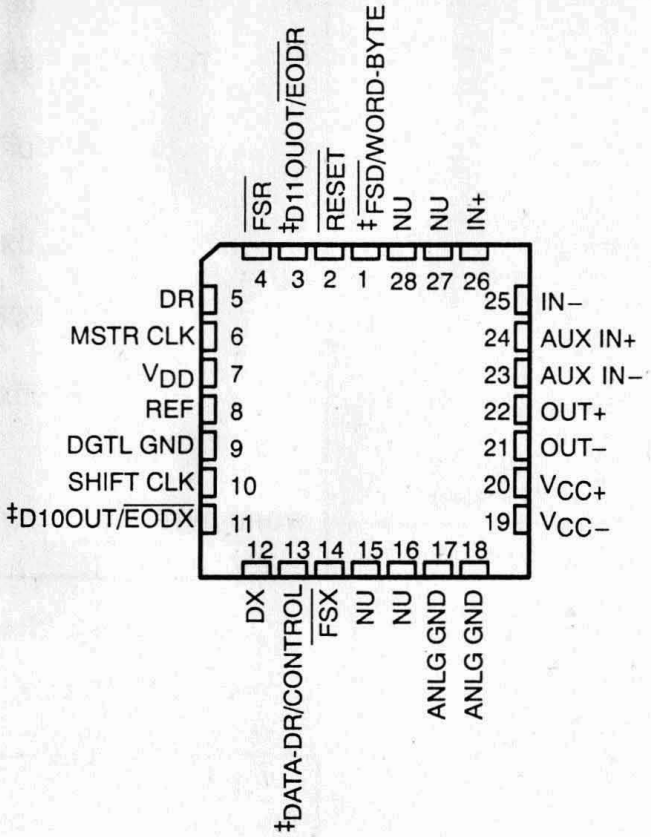
The word or byte mode is selected by first connecting the DATA-DR/CONTROL input (pin 13) to V_{CC-}. $\overline{FSD}$/WORD-BYTE (pin 1) becomes an input and can then be used to select either word or byte transmission formats. The end-of-data transmit ($\overline{EODX}$) and the end-of-data receive ($\overline{EODR}$) signals on pins 11 and 3, respectively, are used to signal the end of word or byte communication (see the Terminal Functions section).

Terminal Assignments

N PACKAGE† (TOP VIEW)



FN PACKAGE (TOP VIEW)



NU - Nonusable; no external connection should be made to these pins.

† 600-mil wide

‡ The portion of the pin name to the left of the slash is used for the Dual-Word (Telephone Interface) mode. The portion of the pin name to the right of the slash is used for Word-Byte mode.

Terminal Functions

PIN NAME	NO.	I/O	DESCRIPTION
ANLG GND	17,18		Analog ground return for all internal analog circuits. Not internally connected to DGTL GND.
AUX IN+	24	I	Noninverting auxiliary analog input stage. This input can be switched into the band-pass filter and ADC path via software control. If the appropriate bit in the control register is a 1, the auxiliary inputs replace the IN+ and IN− inputs. If the bit is a 0, the IN+ and IN− inputs are used (see the DX Serial Data Word Format).
AUX IN−	23	I	Inverting auxiliary analog input (see the above AUX IN+ pin description).
DATA-DR	13	I	The dual-word (telephone interface) mode, selected by applying an input logic level between 0 and 5 V to this input, allows this pin to function as a data input. The data is then framed by the $\overline{FSD}$ signal and transmitted as an output to the DR line during secondary communication. The functions $\overline{FSD}$ (pin 1), D11OUT (pin 3), and D10OUT (pin 11) are valid with this mode selection (see Table 1).
CONTROL			When this input is tied to V_{CC}−, the device is in the word or byte mode. The functions WORD-BYTE (pin 1), $\overline{EODR}$ (pin 3), and $\overline{EODX}$ (pin 11) are valid in this mode. Pin 1 is then used to select either the word or byte mode (see Function Table).
DR	5	O	This pin is used to transmit the ADC output bits from the AIC to the TMS320 serial port. This transmission of bits from the AIC to the TMS320 serial port is synchronized with the SHIFT CLK (pin 10) signal.
DX	12	I	This pin is used to receive the DAC input bits and timing and control information from the TMS320. This serial transmission from the TMS320 serial port is synchronized with the SHIFT CLK (pin 10) signal.
D10OUT	11	O	In the dual-word (telephone interface) mode, bit D10 of the Control Register is output to this pin. When the device is reset, bit D10 is initialized to 0 (see DX Serial Data Word Format). The output update is immediate upon changing bit D10.
$\overline{EODX}$			End of Data Transmit. During the word-mode timing, a low-going pulse occurs on this output immediately after the 16 bits of DAC and control or register information have been transmitted from the TMS320 serial port to the AIC.This signal can be used to interrupt a microprocessor upon completion of serial communications. Also, this signal can be used to strobe and enable external serial-to-parallel shift registers, latches, or external FIFO RAM and to facilitate parallel data bus communications between the DSP and the serial-to-parallel shift registers. During the byte-mode timing, this signal goes low after the first byte has been transmitted from the TMS320 serial port to the AIC and is kept low until the second byte has been transmitted. The TMS320C17 can use this low-going signal to differentiate first and second bytes.
D11OUT	3	O	In the dual-word (telephone interface) mode, bit D11 of the control register is output to this pin. When the device is reset, bit D11 is initialized to 0 (see DX Serial Data Word Format). The output update is immediate upon changing bit D11.
$\overline{EODR}$			End of Data Receive. During the word-mode timing, a low-going pulse occurs on this output immediately after the 16 bits of A/D information have been transmitted from the AIC to the TMS320 serial port. This signal can be used to interrupt a microprocessor upon completion of serial communications. Also, this signal can be used to strobe and enable external serial-to-parallel shift registers, latches, or external FIFO RAM, and to facilitate parallel data bus communications between the DSP and the serial-to-parallel shift registers. During the byte-mode timing, this signal goes low after the first byte has been transmitted from the AIC to the TMS320 serial port and is kept low until the second byte has been transmitted. The TMS320C17 can use this low-going signal to differentiate between first and second bytes.

Terminal Functions (continued)

PIN NAME	NO.	I/O	DESCRIPTION
DGTL	9		Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
$\overline{FSD}$	1	O	Frame Sync Data. The $\overline{FSD}$ output remains high during primary communication. In the dual-word (telephone interface) mode, the $\overline{FSD}$ output is identical to the $\overline{FSX}$ output during secondary communication.
WORD-BYTE		I	The WORD-BYTE pin allows differentiation between the word and byte data format (see DATA-DR/CONTROL (pin 13) and Table 1 for details).
$\overline{FSR}$	4	O	Frame Sync Receive. The $\overline{FSR}$ pin is held low during bit transmission. When the $\overline{FSR}$ pin goes low, the TMS320 serial port begins receiving bits from the AIC via the DR pin of the AIC. The most significant DR bit is present on the DR pin before $\overline{FSR}$ goes low. See Serial Port Sections and Internal Timing Configuration Diagrams.
$\overline{FSX}$	14	O	Frame Sync Transmit. When this pin goes low, the TMS320 serial port begins transmitting bits to the AIC via the DX pin of the AIC. The $\overline{FSX}$ pin is held low during bit transmission (see Serial Port Sections and Internal Timing Configuration Diagrams).
IN+	26	I	Noninverting input to analog input amplifier stage
IN–	25	I	Inverting input to analog input amplifier stage
MSTR CLK	6	I	The master clock signal is used to derive all the key logic signals of the AIC, such as the shift clock, the switched-capacitor filter clocks, and the A/D and D/A timing signals. The Internal Timing Configuration diagram shows how these key signals are derived. The frequencies of these signals are synchronous submultiples of the master clock frequency to eliminate unwanted aliasing when the sampled analog signals are transferred between the switched-capacitor filters and the ADC and DAC converters (see the Internal Timing Configuration).
OUT+	22	O	Noninverting output of analog output power amplifier. Drives transformer hybrids or high-impedance loads directly in a differential or a single-ended configuration.
OUT–	21	O	Inverting output of analog output power amplifier. Functionally identical with and complementary to OUT+.
REF	8	I/O	The internal voltage reference is brought out on this pin. An external voltage reference can be applied to this pin to override the internal voltage reference.
$\overline{RESET}$	2	I	A reset function is provided to initialize TA, TA', TB, RA, RA', RB (see Figure 2-1), and the control registers. This reset function initiates serial communications between the AIC and DSP. The reset function initializes all AIC registers, including the control register. After a negative-going pulse on the $\overline{RESET}$ pin, the AIC registers are initialized to provide a 16-kHz data conversion rate for a 10.368-MHz master clock input signal. The conversion rate adjust registers, TA' and RA', are reset to 1. The CONTROL register bits are reset as follows (see AIC DX Data Word Format section): D11 = 0, D10 = 0, D9 = 1, D7 = 1, D6 = 1, D5 = 1, D4 = 0, D3 = 0, D2 = 1 The shift clock (SCLK) is held high during $\overline{RESET}$. This initialization allows normal serial-port communication to occur between the AIC and the DSP.
SHIFT CLK	10	O	The shift clock signal is obtained by dividing the master clock signal frequency by four. This signal is used to clock the serial data transfers of the AIC.
V_{DD}	7		Digital supply voltage, 5 V ±5%
$V_{CC}+$	20		Positive analog supply voltage, 5 V ±5%
$V_{CC}-$	19		Negative analog supply voltage, –5 V ±5%

Detailed Description

Table 1. Mode-Selection Function Table

DATA-DR/ CONTROL (Pin 13)	$\overline{\text{FSD}}$/ WORD-BYTE (Pin 1)	CONTROL REGISTER BIT (D5)	OPERATING MODE	SERIAL CONFIGURATION	DESCRIPTION
Data in (0 to 5 V)	$\overline{\text{FSD}}$ out (0 to 5 V)	1	Dual-Word (Telephone Interface)	Synchronous, One 16-Bit Word	Pin functions DATA-DR (pin 13†), $\overline{\text{FSD}}$ (pin 1†), D11OUT (pin 3), and D10OUT (pin 11) are applicable in this configuration. $\overline{\text{FSD}}$ is asserted during secondary communication, but the $\overline{\text{FSR}}$ is not asserted. However, $\overline{\text{FSD}}$ remains high during primary communication.
Data in (0 to 5 V)	$\overline{\text{FSD}}$ out (0 to 5 V)	0	Dual-Word (Telephone Interface)	Asynchronous, One 16-Bit Word	Pin functions DATA-DR (pin 13†), $\overline{\text{FSD}}$ (pin 1†), D11OUT (pin 3), and D10OUT (pin 11) are applicable in this configuration. $\overline{\text{FSD}}$ is asserted during secondary communication, but the $\overline{\text{FSR}}$ is not asserted. However, $\overline{\text{FSD}}$ remains high during primary communication. If secondary communications occur while the A/D conversion is being transmitted from the DR (pin 5), $\overline{\text{FSD}}$ cannot go low, and data from the DATA-DR pin cannot go onto the DR pin (pin 5).
V_{CC-}	V_{CC+}	1	WORD	Synchronous, One 16-Bit Word	Pin functions CONTROL (pin 13†), WORD-BYTE (pin 1†), $\overline{\text{EODR}}$ (pin 3), and $\overline{\text{EODX}}$ (pin 11) are applicable in this configuration.
		0		Asynchronous, One 16-bit Word	Pin functions CONTROL (pin 13†), WORD-BYTE (pin 1†), $\overline{\text{EODR}}$ (pin 3), and $\overline{\text{EODX}}$ (pin 11) are applicable in this configuration.
	V_{CC-}	1	BYTE	Synchronous, Two 8-Bit Bytes	Pin functions CONTROL (pin 13†), WORD-BYTE (pin 1†), $\overline{\text{EODR}}$ (pin 3), and $\overline{\text{EODX}}$ (pin 11) are applicable in this configuration.
		0		Asynchronous, Two 8-Bit Bytes	Pin functions CONTROL (pin 13†), WORD-BYTE (pin 1†), $\overline{\text{EODR}}$ (pin 3), and $\overline{\text{EODX}}$ (pin 11) are applicable in this configuration.

† Pin 13 has an internal pulldown resistor to −5 V, and pin 1 has an internal pullup resistor to 5 V.

Internal Timing Configuration (see Figure 4)

All the internal timing of the AIC is derived from the high-frequency clock signal that drives the master clock input pin. The shift clock signal, which strobes the serial port data between the AIC and DSP, is derived by dividing the master clock input signal frequency by four.

The TX(A) counter and the TX(B) counter, which are driven by the master clock signal, determine the D/A conversion timing. Similarly, the RX(A) counter and the RX(B) counter determine the A/D conversion timing. In order for the low-pass switched-capacitor filter in the D/A path (see Functional Block Diagram) to meet its transfer function specifications, the frequency of its clock input must be 288 kHz. If the clock frequency is not 288 kHz, the filter transfer function frequencies are frequency-scaled by the ratios of the clock frequency to 288 kHz:

$$\text{Absolute Frequency (kHz)} = \frac{\text{Normalized Frequency} \times \text{SCF } f_{clock} \text{ (kHz)}}{288} \quad (1)$$

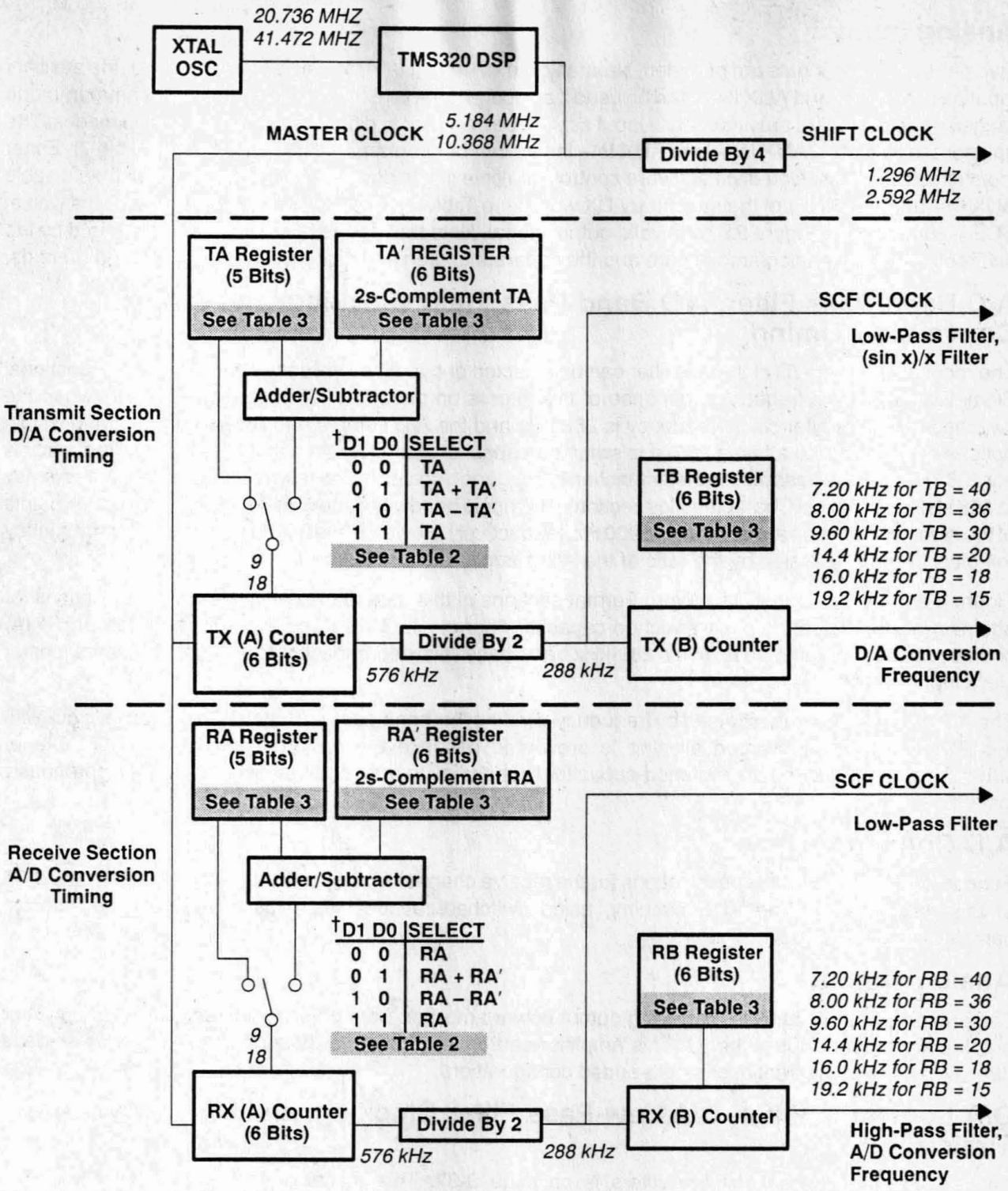
To obtain the specified filter response, the combination of master clock frequency and the TX(A) counter and the RX(A) counter values must yield a 288-kHz switched-capacitor clock signal. This 288-kHz clock signal can then be divided by the TX(B) counter to establish the D/A conversion timing.

The transfer function of the band-pass switched-capacitor filter in the A/D path (see Functional Block Diagram) is a composite of its high-pass and low-pass transfer functions. When the Shift Clock Frequency (SCF) is 288 kHz, the high-frequency roll-off of the low-pass section will meet the band-pass filter transfer function specification. Otherwise, the high-frequency roll-off will be frequency-scaled by the ratio of the high-pass section's SCF clock to 288 kHz (see Figure 23). The low-frequency roll-off of the high-pass section meets the band-pass filter transfer function specification when the A/D conversion rate is 16 kHz. If not, the low-frequency roll-off of the high-pass section is frequency-scaled by the ratio of the A/D conversion rate to 16 kHz.

The TX(A) counter and the TX(B) counter are reloaded each D/A conversion period, while the RX(A) counter and the RX(B) counter are reloaded every A/D conversion period. The TX(B) counter and the RX(B) counter are loaded with the values in the TB and RB registers, respectively. Via software control, the TX(A) counter can be loaded with the TA register, the TA register less the TA′ register, or the TA register plus the TA′ register. By selecting the TA register less the TA′ register option, the upcoming conversion timing occurs earlier by an amount of time that equals TA′ times the signal period of the master clock. If the TA register plus the TA′ register option is executed, the upcoming conversion timing occurs later by an amount of time that equals TA′ times the signal period of the master clock. Thus, the D/A conversion timing can be advanced or retarded. An identical ability to alter the A/D conversion timing is provided. However, the RX(A) counter can be programmed via software control with the RA register, the RA register less the RA′ register, or the RA register plus the RA′ register.

The ability to advance or retard conversion timing is particularly useful for modem applications. This feature allows controlled changes in the A/D and D/A conversion timing and can be used to enhance signal-to-noise performance, to perform frequency-tracking functions, and to generate nonstandard modem frequencies.

If the transmit and receive sections are configured to be synchronous, then the low-pass and band-pass switched-capacitor filter clocks are derived from the TX(A) counter. Also, both the D/A and A/D conversion timings are derived from the TX(A) counter and the TX(B) counter. When the transmit and receive sections are configured to be synchronous, the RX(A) counter, RX(B) counter, RA register, RA′ register, and RB registers are not used.



† These control bits are described in the DX Serial Data Word Format section.

NOTES: A. Tables 2 and 3 (pages 9–25 and 9–26) are primary and secondary communication protocols, respectively.

B. In synchronous operation, RA, RA', RB, RX(A), and RX(B) are not used. TA, TA', TB, TX(A), and TX(B) are used instead.

C. Items in italics refer only to frequencies and register contents, which are variable. A crystal oscillator driving 20.736 MHz into the TMS320-series DSP will provide a master clock frequency of 5.184 MHz. The TLC32046 will produce a shift clock frequency of 1.296 MHz. If the TX(A) register contents equal 9, the SCF clock frequency will then be 288 kHz, and the D/A conversion frequency will be 288 kHz ÷ T(B).

Figure 4. Asynchronous Internal Timing Configuration

Analog Input

Two pairs of analog inputs are provided. Normally, the IN+ and IN– input pair is used; however, the auxiliary input pair, AUX IN+ and AUX IN–, can be used if a second input is required. Since sufficient common-mode range and rejection are provided, each input set can be operated in differential or single-ended modes. The gain for the IN+, IN–, AUX IN+, and AUX IN– inputs can be programmed to 1, 2, or 4 (see Table 7). Either input circuit can be selected via software control. Multiplexing is controlled with the D4 bit (enable/disable AUX IN+ and AUX IN–) of the secondary DX word (see Table 3). The multiplexing requires a 2-ms wait at SCF = 288 kHz (see Figure 21) for a valid output signal. Note that a wide dynamic range is assured by the differential internal analog architecture and the separate analog and digital voltage supplies and grounds.

A/D Band-Pass Filter, A/D Band-Pass Filter Clocking, and A/D Conversion Timing

The receive-channel A/D high-pass filter can be selected or bypassed via software control (see Functional Block Diagram). The frequency response of this filter is on page 9-37. This response results when the switched-capacitor filter clock frequency is 288 kHz and the A/D sample rate is 16 kHz. Several possible options can be used to attain a 288-kHz switched-capacitor filter clock. When the filter clock frequency is not 288 kHz, the low-pass filter transfer function is frequency-scaled by the ratio of the actual clock frequency to 288 kHz (see Typical Characteristics section). The ripple bandwidth and 3-dB low-frequency roll-off points of the high-pass section are 300 Hz and 200 Hz, respectively. However, the high-pass section low-frequency roll-off is frequency-scaled by the ratio of the A/D sample rate to 16 kHz.

Figure 4 and the DX Serial Data Word Format sections of this data manual indicate the many options for attaining a 288-kHz band-pass switched-capacitor filter clock. These sections indicate that the RX(A) counter can be programmed to give a 288-kHz band-pass switched-capacitor filter clock for several master clock input frequencies.

The A/D conversion rate is attained by frequency-dividing the band-pass switched-capacitor filter clock with the RX(B) counter. Unwanted aliasing is prevented because the A/D conversion rate is an integer submultiple of the band-pass switched-capacitor filter sampling rate, and the two rates are synchronously locked.

A/D Converter

Fundamental performance specifications for the receive channel ADC circuitry are on pages 9-34 and 9-35 of this data manual. The ADC circuitry, using switched-capacitor techniques, provides an inherent sample-and-hold function.

Analog Output

The analog output circuitry is an analog output power amplifier. Both noninverting and inverting amplifier outputs are brought out of the IC. This amplifier can drive transformer hybrids or low-impedance loads directly in either a differential or single-ended configuration.

D/A Low-Pass Filter, D/A Low-Pass Filter Clocking, and D/A Conversion Timing

The frequency response of these filters is on page 9-37. This response results when the low-pass switched-capacitor filter clock frequency is 288 kHz (see Equation 1). Like the A/D filter, the transfer function of this filter is frequency-scaled when the clock frequency is not 288 kHz (see Typical Characteristics section). A continuous-time filter is provided on the output of the low-pass filter to eliminate the periodic sample data signal information, which occurs at multiples of the 288-kHz switched-capacitor clock feedthrough.

The D/A conversion rate is attained by frequency-dividing the 288-kHz switched-capacitor filter clock with the T(B) counter. Unwanted aliasing is prevented because the D/A conversion rate is an integer submultiple of the switched-capacitor low-pass filter sampling rate, and the two rates are synchronously locked.

D/A Converter

Fundamental performance specifications for the transmit channel DAC circuitry are on pages 9-35 and 9-36. The DAC has a sample-and-hold function that is realized with a switched-capacitor ladder.

Serial Port

The serial port has four possible configurations summarized in the Function Table on page 9-10. These configurations are briefly described below.

1. The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS320C17. The communications protocol is two 8-bit bytes.
2. The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS32020, TMS320C25, and TMS320C30. The communications protocol is one 16-bit word.
3. The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS320C17. The communications protocol is two 8-bit bytes.
4. The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS32020, TMS320C25, TMS320C30, or two SN74299 serial-to-parallel shift registers, which can interface in parallel to the TMS32010, TMS320C15, to any other digital signal processor, or to external FIFO circuitry. The communications protocol is one 16-bit word.

Synchronous Operation

When the transmit and receive sections are operated synchronously, the low-pass filter clock drives both low-pass and band-pass filters (see Functional Block Diagram). The A/D conversion timing is derived from and equal to the D/A conversion timing. When data bit D5 in the control register is a logic 1, transmit and receive sections are synchronous. The band-pass switched-capacitor filter and the A/D converter timing are derived from the TX(A) counter, the TX(B) counter, and the TA and TA' registers. In synchronous operation, both the A/D and the D/A channels operate from the same frequencies. The $\overline{\text{FSX}}$ and the $\overline{\text{FSR}}$ timing is identical during primary communication, but $\overline{\text{FSR}}$ is not asserted during secondary communication because there is no new A/D conversion result.

One 16-Bit Word (Dual-Word [Telephone Interface] or Word Mode)

The serial port interfaces directly with the serial ports of the TMS32020, TMS320C25, and the TMS320C30, and communicates in one 16-bit word. The operation sequence is as follows:

1. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought low by the TLC32046 AIC.
2. One 16-bit word is transmitted and one 16-bit word is received.
3. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought high.
4. The $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ pins emit low-going pulses one shift clock wide. $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ are valid in the word or byte mode only.

If the device is in the dual-word (telephone interface) mode, $\overline{\text{FSD}}$ goes low during the secondary communication period and enables the data word received at the DATA-DR/CONTROL input pin to be routed to the DR line. The secondary communication period occurs four shift clocks after completion of primary communications.

Two 8-Bit Bytes (Byte Mode)

The serial port interfaces directly with the serial port of the TMS320C17 and communicates in two 8-bit bytes. The operation sequence is as follows:

1. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought low.
2. One 8-bit word is transmitted and one 8-bit word is received.
3. The $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ pins are brought low.
4. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins emit positive frame-sync pulses that are four shift clock cycles wide.

5. One 8-bit byte is transmitted and one 8-bit byte is received.
6. The $\overline{FSX}$ and $\overline{FSR}$ pins are brought high.
7. The $\overline{EODX}$ and $\overline{EODR}$ pins are brought high.

Synchronous Operating Frequencies

The synchronous operating frequencies are determined by the following equations.

Switched capacitor filter (SCF) frequencies (see Figure 4):

$$\text{Low-pass SCF clock frequency} \quad \text{(D/A and A/D channels)} = \frac{\text{master clock frequency}}{\text{T(A)} \times 2}$$

$$\text{High-pass SCF clock frequency (A/D channel)} = \text{A/D conversion frequency}$$

$$\text{Conversion frequency (A/D and D/A channels)} = \frac{\text{Low pass SCF clock frequency}}{\text{T(B)}}$$

$$= \frac{\text{master clock frequency}}{\text{T(A)} \times 2 \times \text{T(B)}}$$

NOTE: T(A), T(B), R(A), and R(B) are the contents of the TA, TB, RA, and RB registers, respectively.

Asynchronous Operation

When the transmit and the receive sections are operated asynchronously, the low-pass and band-pass filter clocks are independently generated from the master clock. The D/A and the A/D conversion timing is also determined independently.

D/A timing is set by the counters and registers described in synchronous operation, but the RA and RB registers are substituted for the TA and TB registers to determine the A/D channel sample rate and the A/D path switched-capacitor filter frequencies. Asynchronous operation is selected by control register bit D5 being zero.

One 16-Bit Word (Word Mode)

The serial port interfaces directly with the serial ports of the TMS32020, TMS320C25, and TMS320C30 and communicates with 16-bit word formats. The operation sequence is as follows:

1. The $\overline{FSX}$ or $\overline{FSR}$ pins are brought low by the TLC32046 AIC.
2. One 16-bit word is transmitted or one 16-bit word is received.
3. The $\overline{FSX}$ or $\overline{FSR}$ pins are brought high.
4. The $\overline{EODX}$ or $\overline{EODR}$ pins emit low-going pulses one shift clock wide. $\overline{EODX}$ and $\overline{EODR}$ are valid in either the word or byte mode only.

Two 8-Bit Bytes (Byte Mode)

The serial port interfaces directly with the serial port of the TMS320C17 and communicates in two 8-bit bytes. The operating sequence is as follows:

1. The $\overline{FSX}$ or $\overline{FSR}$ pins are brought low by the TLC32046 AIC.
2. One byte is transmitted or received.
3. The $\overline{EODX}$ or $\overline{EODR}$ pins are brought low.
4. The $\overline{FSX}$ or $\overline{FSR}$ pins are brought high for four shift clock periods and then brought low.
5. The second byte is transmitted or received.
6. The $\overline{FSX}$ or $\overline{FSR}$ pins are brought high.
7. The $\overline{EODX}$ or $\overline{EODR}$ pins are brought high.

Asynchronous Operating Frequencies

The asynchronous operating frequencies are determined by the following equations.

Switched-capacitor filter frequencies (see Figure 4):

$$\text{Low-pass D/A SCF clock frequency} = \frac{\text{master clock frequency}}{\text{T(A)} \times 2}$$

$$\text{Low-pass A/D SCF clock frequency} = \frac{\text{master clock frequency}}{\text{R(A)} \times 2}$$

$$\text{High-pass SCF clock frequency (A/D channel)} = \text{A/D conversion frequency} \quad (2)$$

Conversion frequency:

$$\text{D/A conversion frequency} = \frac{\text{Low-pass D/A SCF clock frequency}}{\text{T(B)}}$$

$$\text{A/D conversion frequency} = \frac{\text{Low-pass A/D SCF clock frequency (for low pass receive filter)}}{\text{R(B)}} \quad (3)$$

NOTE: T(A), T(B), R(A), and R(B) are the contents of the TA, TB, RA, and RB registers, respectively.

Operation of TLC32046 With Internal Voltage Reference

The internal reference of the TLC32046 eliminates the need for an external voltage reference and provides overall circuit cost reduction. The internal reference eases the design task and provides complete control of the IC performance. The internal reference is brought out to pin 8. To keep the amount of noise on the reference signal to a minimum, an external capacitor can be connected between REF and ANLG GND.

Operation of TLC32046 With External Voltage Reference

The REF pin can be driven from an external reference circuit. This external circuit must be capable of supplying 250 μA and must be protected adequately from noise and crosstalk from the analog input.

Reset

A reset function is provided to initiate serial communications between the AIC and DSP and to allow fast, cost-effective testing during manufacturing. The reset function initializes all AIC registers, including the control register. After a negative-going pulse on the $\overline{\text{RESET}}$ pin, the AIC is initialized. This initialization allows normal serial port communications activity to occur between AIC and DSP (see AIC DX Data Word Format section). After RESET, TA=TB=RA=RB=18 (or 12 hexadecimal), TA′=RA′=01 (hexadecimal), the A/D high-pass filter is inserted, the loop-back function is deleted, AUX IN+ and AUX IN− pins are disabled, transmit and receive sections are in synchronous operation, programmable gain is set to 1, the on-board (sin x)/x correction filter is not selected, D10 OUT is set to 0, and D11 OUT is set to 0.

Loopback

This feature allows the circuit to be tested remotely. In loopback, the OUT+ and OUT− pins are internally connected to the IN+ and IN− pins. The DAC bits (D15 to D2), which are transmitted to the DX pin, can be compared with the ADC bits (D15 to D2), received from the DR pin. The bits on the DR pin equal the bits on the DX pin. However, there is some difference in these bits due to the ADC and DAC output offsets.

The loopback feature is implemented with digital signal processor control by transmitting a logic '1' for data bit D3 in the DX secondary communication to the control register (see Table 3).

Communications Word Sequence

In the Dual-Word (Telephone Interface) mode, there are two data words that are presented to the DSP or μP from the DR terminal. The first data word is the ADC conversion result occurring during the FSR time, and the second is the serial data applied to the DATA-DR pin during the FSD time. FSR is not asserted during secondary communications and FSD is not asserted during primary communications.

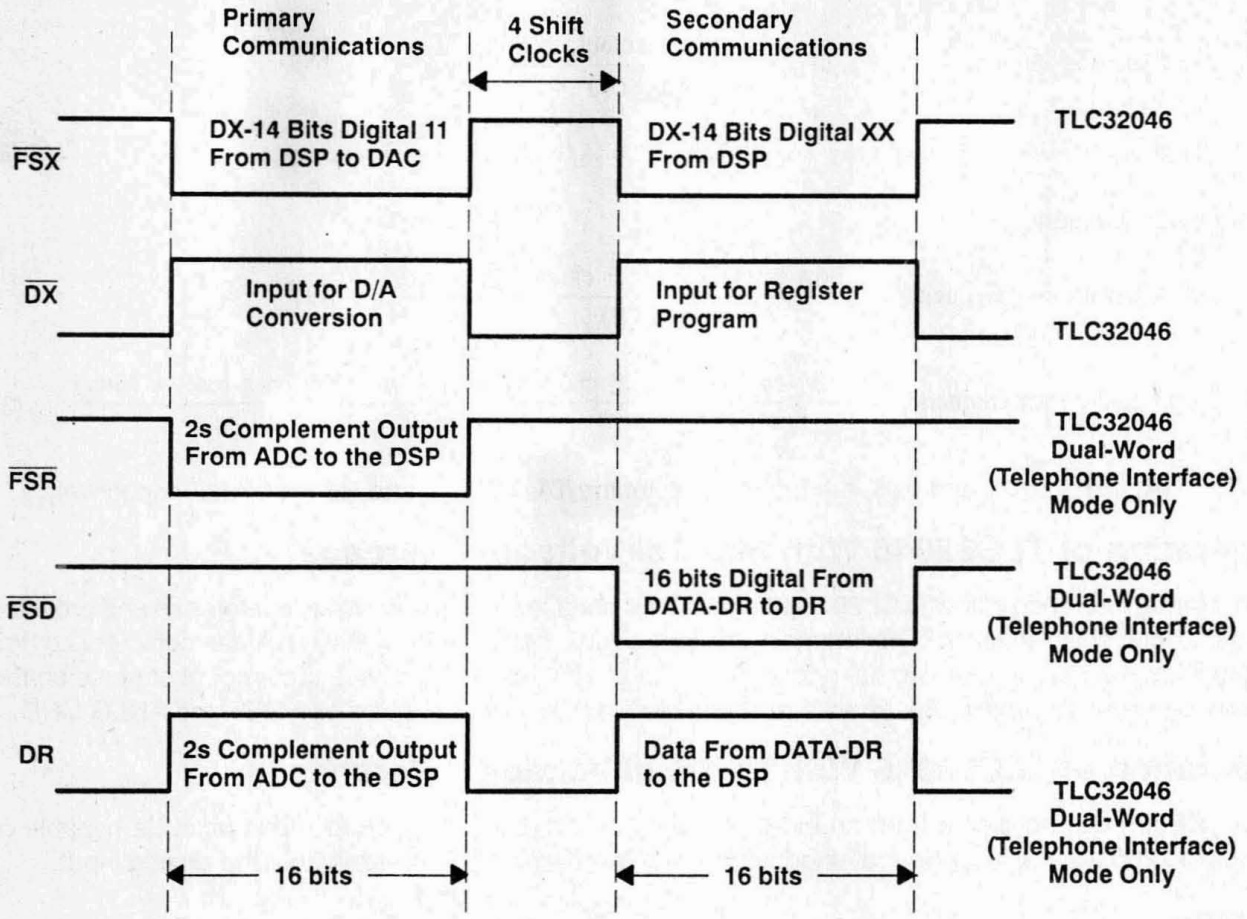


Figure 5. Primary and Secondary Communications Word Sequence

DR SERIAL DATA WORD FORMAT

DR Word Bit Pattern

A/D MSB
1st bit sent ↓

A/D LSB ↓

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

The data word is the 14-bit conversion result of the receive channel to the processor in 2s complement format. With 16-bit processors, the data is 16 bits long with the two LSBs at zero. Using 8-bit processors, the data word is transmitted in the same order as one 16-bit word, but as two bytes with the two LSBs of the second byte set to zero.

DX SERIAL DATA WORD FORMAT

Primary DX Word Bit Pattern

A/D OR D/A MSB
1st bit sent ↓ — 1st bit sent of 2nd byte ↓ — A/D or D/A LSB ↓

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 2. Primary DX Serial Communication Protocol

FUNCTIONS	D1	D0
D15 (MSB)-D2 → DAC Register. TA → TX(A), RA → RX(A). See Figure 4. TB → TX(B), RB → RX(B). See Figure 4.	0	0
D15 (MSB)-D2 → DAC Register. TA+TA′ → TX(A), RA+RA′ → RX(A). See Figure 4. TB → TX(B), RB → RX(B). See Figure 4. The next D/A and A/D conversion period will be changed by the addition of TA′ and RA′ master clock cycles, in which TA′ and RA′ can be positive, negative, or zero. Refer to Table 4, AIC Responses to Improper Conditions.	0	1
D15 (MSB)-D2 → DAC Register. TA–TA′ → TX(A), RA–RA′ → RX(A). See Figure 4. TB → TX(B), RB → RX(B). See Figure 4. The next D/A and A/D conversion period will be changed by the subtraction of TA′ and RA′ master clock cycles, in which TA′ and RA′ can be positive, negative, or zero. Refer to Table 4, AIC Responses to Improper Conditions.	1	0
D15 (MSB)-D2 → DAC Register. TA → TX(A), RA → RX(A). See Figure 4. TB → TX(B), RB → RX(B). See Figure 4. After a delay of four shift cycles, a secondary transmission follows to program the AIC to operate in the desired configuration. In the telephone interface mode, data on DATA DR (pin 13) is routed to DR (Serial Data Output) during secondary transmission.	1	1

NOTE: Setting the two least significant bits to 1 in the normal transmission of DAC information (primary communications) to the AIC initiates secondary communications upon completion of the primary communications. When the primary communication is complete, $\overline{FSX}$ remains high for four SHIFT CLOCK cycles and then goes low and initiates the secondary communication. The timing specifications for the primary and secondary communications are identical. In this manner, the secondary communication, if initiated, is interleaved between successive primary communications. This interleaving prevents the secondary communication from interfering with the primary communications and DAC timing. This prevents the AIC from skipping a DAC output. It is important to note that $\overline{FSR}$ is not asserted during secondary communications activity. However, in the dual-word (telephone interface) mode, $\overline{FSD}$ is asserted during secondary communications but not during primary communications.

Secondary DX Word Bit Pattern

D/A MSB
1st bit sent ↓ | 1st bit sent of 2nd byte ↓ | D/A LSB ↓

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 3. Secondary DX Serial Communication Protocol

FUNCTIONS	D1	D0
D13 (MSB)-D9 → TA , 5 bits unsigned binary. See Figure 4. D6 (MSB)-D2 → RA, 5 bits unsigned binary. See Figure 4. D15, D14, D8, and D7 are unassigned.	0	0
D14 (sign bit)-D9 → TA′, 6 bits 2s complement. See Figure 4. D7 (sign bit)-D2 → RA′, 6 bits 2s complement. See Figure 4. D15 and D8 are unassigned.	0	1
D14 (MSB)-D9 → TB, 6 bits unsigned binary. See Figure 4. D7 (MSB)-D2 → RB, 6 bits unsigned binary. See Figure 4. D15 and D8 are unassigned.	1	0
D2 = 0/1 deletes/inserts the A/D high-pass filter. D3 = 0/1 deletes/inserts the loopback function. D4 = 0/1 disables/enables the AUX IN+ and AUX IN– pins. D5 = 0/1 asynchronous/synchronous transmit and receive sections. D6 = 0/1 gain control bits (see Table 7). D7 = 0/1 gain control bits (see Table 7). D9 = 0/1 delete/insert on-board second-order (sinx)/x correction filter D10 = 0/1 output to D10OUT (dual-word (telephone interface) mode) D11 = 0/1 output to D11OUT (dual-word (telephone interface) mode) D8, D12–D15 are unassigned.	1	1

Reset Function

A reset function is provided to initiate serial communications between the AIC and DSP. The reset function initializes all AIC registers, including the control register. After power has been applied to the AIC, a negative-going pulse on the $\overline{\text{RESET}}$ pin initializes the AIC registers to provide a 16-kHz A/D and D/A conversion rate for a 10.368-MHz master clock input signal. Also, the pass-bands of the A/D and D/A filters are 300 Hz to 7200 Hz and 0 Hz to 7200 Hz, respectively. Therefore, the filter bandwidths are half those shown in the filter transfer function specification section. The AIC, excepting the CONTROL register, is initialized as follows (see AIC DX Data Word Format section):

REGISTER	TA	TA′	TB	RA	RA′	RB
INITIALIZED VALUE (HEX)	12	01	12	12	01	12

The CONTROL register bits are reset as follows (see Table 3):

D11 = 0, D10 = 0, D9 = 1, D7 = 1, D6 = 1, D5 = 1, D4 = 0, D3 = 0, D2 = 1

This initialization allows normal serial port communications to occur between the AIC and the DSP. If the transmit and receive sections are configured to operate synchronously and the user wishes to program different conversion rates, only the TA, TA′, and TB register need to be programmed. Both transmit and receive timing are synchronously derived from these registers (see the Terminal Functions and DX Serial Data Word Format sections).

Figure 2–3 shows a circuit that provides a reset on power-up when power is applied in the sequence given in the Power-Up Sequence section. The circuit depends on the power supplies reaching their recommended values a minimum of 800 ns before the capacitor charges to 0.8 V above DGTL GND.

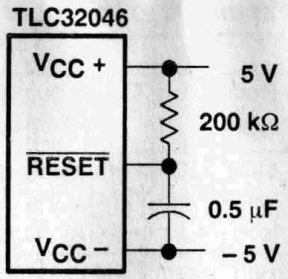


Figure 6. Reset on Power-Up Circuit

Power-Up Sequence

To ensure proper operation of the AIC and as a safeguard against latch-up, it is recommended that Schottky diodes with forward voltages less than or equal to 0.4 V be connected from V_{CC-} to ANLG GND and from V_{CC-} to DGTL GND. In the absence of such diodes, power is applied in the following sequence: ANLG GND and DGTL GND, V_{CC-}, then V_{CC+} and V_{DD}. Also, no input signal is applied until after power-up.

AIC Register Constraints

The following constraints are placed on the contents of the AIC registers:

1. TA register must be ≥ 4 in word mode (WORD/BYTE= High).
2. TA register must be ≥ 5 in byte mode (WORD/BYTE= Low).
3. TA′ register can be either positive, negative, or zero.
4. RA register must be ≥ 4 in word mode (WORD/BYTE = High).
5. RA register must be ≥ 5 in byte mode (WORD/BYTE = Low).
6. RA′ register can be either positive, negative, or zero.
7. (TA register ± TA′ register) must be > 1.
8. (RA register ± RA′ register) must be > 1.
9. TB register must be ≥ 15.
10. RB register must be ≥ 15.

AIC Responses to Improper Conditions

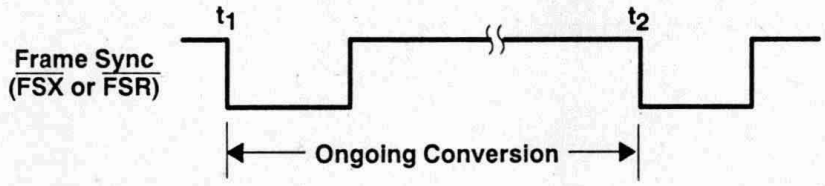
The AIC has provisions for responding to improper conditions. These improper conditions and the response of the AIC to these conditions are presented in Table 4.

Table 4. AIC Responses to Improper Conditions

IMPROPER CONDITION	AIC RESPONSE
TA register + TA′ register = 0 or 1 TA register – TA′ register = 0 or 1	Reprogram TX(A) counter with TA register value
TA register + TA′ register < 0	MODULO 64 arithmetic is used to ensure that a positive value is loaded into TX(A) counter, i.e., TA register + TA′ register + 40 HEX is loaded into TX(A) counter.
RA register + RA′ register = 0 or 1 RA register – RA′ register = 0 or 1	Reprogram RX(A) counter with RA register value
RA register + RA′ register = 0 or 1	MODULO 64 arithmetic is used to ensure that a positive value is loaded into RX(A) counter, i.e., RA register + RA′ register + 40 HEX is loaded into RX(A) counter.
TA register = 0 or 1 RA register = 0 or 1	AIC is shut down. Reprogram TA or RA registers after a reset.
TA register < 4 in word mode TA register < 5 in byte mode RA register < 4 in word mode RA register < 5 in byte mode	The AIC serial port no longer operates. Reprogram TA or RA registers after a reset.
TB register < 15	Reprogram TB register with 12 HEX
RB register < 15	Reprogram RB register with 12 HEX
AIC and DSP cannot communicate	Hold last DAC output

Operation With Conversion Times Too Close Together

If the difference between two successive D/A conversion frame syncs is less than 1/25 kHz, the AIC operates improperly. In this situation, the second D/A conversion frame sync occurs too quickly, and there is not enough time for the ongoing conversion to be completed. This situation can occur if the A and B registers are improperly programmed or if the A + A′ register result is too small. When incrementally adjusting the conversion period via the A + A′ register options, the designer should not violate this requirement. See Figure 4.



$t_2 - t_1 \leq 1/25$ kHz

Figure 7. Conversion Times Too Close Together

More Than One Receive Frame Sync Occurring Between Two Transmit Frame Syncs – Asynchronous Operation

When incrementally adjusting the conversion period via the A + A′ or A – A′ register options, a specific protocol is followed. The command to use the incremental conversion period adjust option is sent to the AIC during an $\overline{\text{FSX}}$ frame sync. The ongoing conversion period is then adjusted; however, either receive conversion period A or conversion period B may be adjusted. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. If there is sufficient time between t_1 and t_2, the receive conversion period adjustment is performed during receive conversion period A. Otherwise, the adjustment is performed during receive conversion period B.

The adjustment command only adjusts one transmit conversion period and one receive conversion period. To adjust another pair of transmit and receive conversion periods, another command must be issued during a subsequent $\overline{FSX}$ frame (see Figure 8).

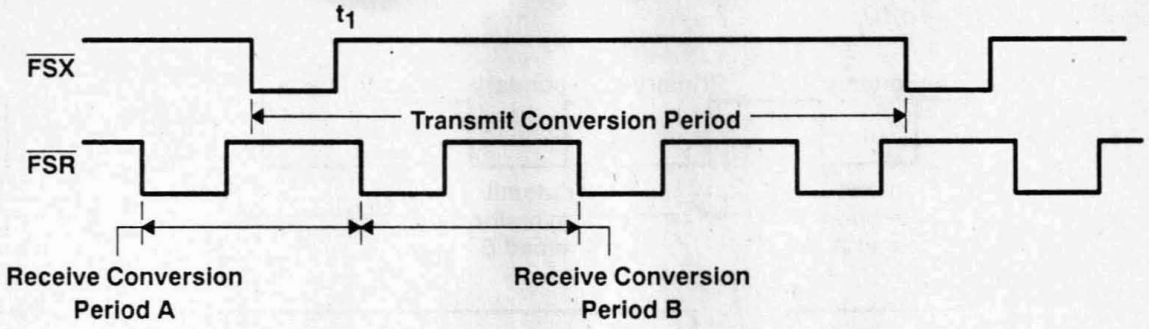


Figure 8. More Than One Receive Frame Sync Between Two Transmit Frame Syncs

More Than One Transmit Frame Sync Occurring Between Two Receive Frame Syncs – Asynchronous Operation

When incrementally adjusting the conversion period via the A + A′ or A – A′ register options, a specific protocol must be followed. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. The command to use the incremental conversion period adjust options is sent to the AIC during an $\overline{FSX}$ frame sync. The ongoing transmit conversion period is then adjusted. However, three possibilities exist for the receive conversion period adjustment as shown in Figure 9. When the adjustment command is issued during transmit conversion period A, receive conversion period A is adjusted if there is sufficient time between t1 and t2. If there is not sufficient time between t1 and t2, receive conversion period B is adjusted. The third option is that the receive portion of an adjustment command can be ignored if the adjustment command is sent during a receive conversion period, which is adjusted due to a prior adjustment command. For example, if adjustment commands are issued during transmit conversion periods A, B, and C, the first two commands may cause receive conversion periods A and B to be adjusted, while the third receive adjustment command is ignored. The third adjustment command is ignored since it was issued during receive conversion period B, which already is adjusted via the transmit conversion period B adjustment command.

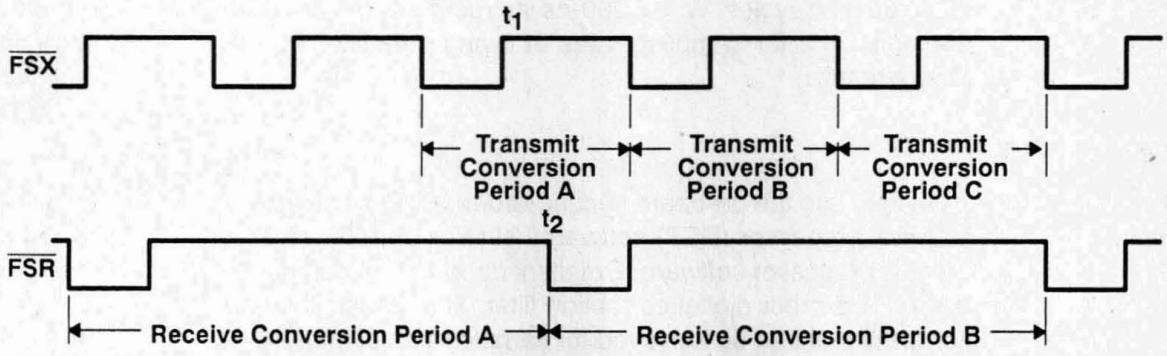


Figure 9. More Than One Transmit Frame Sync Between Two Receive Frame Syncs

More than One Set of Primary and Secondary DX Serial Communications Occurring Between Two Receive Frame Syncs (See DX Serial Data Word Format section) – Asynchronous Operation

The TA, TA′, TB, and control register information that is transmitted in the secondary communication is accepted and applied during the ongoing transmit conversion period. If there is sufficient time between t_1

and t_2, the TA, RA′, and RB register information, sent during transmit conversion period A, is applied to receive conversion period A. Otherwise, this information is applied during receive conversion period B. If RA, RA′, and RB register information has been received and is being applied during an ongoing conversion period, any subsequent RA, RA′, or RB information received during this receive conversion period is disregarded. See Figure 10.

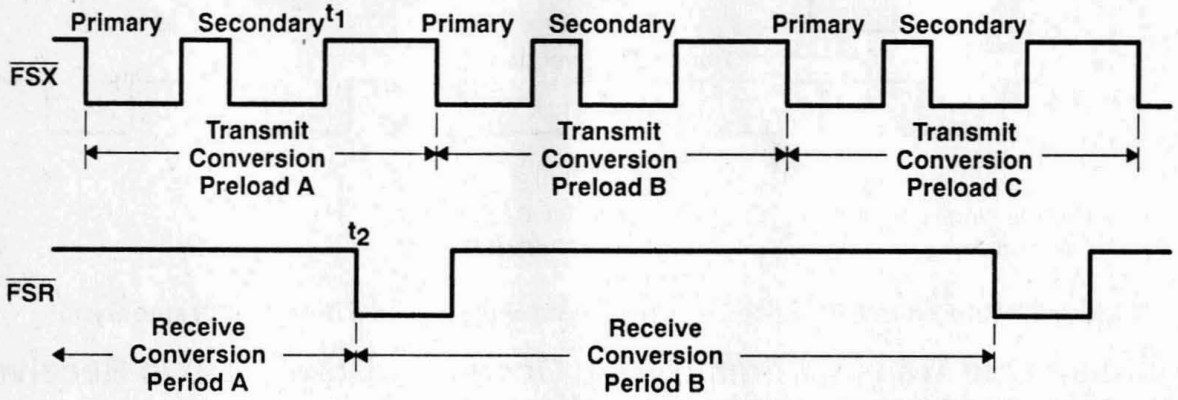


Figure 10. More Than One Set of Primary and Secondary DX Serial Communications Between Two Receive Frame Syncs

System Frequency Response Correction

The (sin x)/x correction for the DAC zero-order sample-and-hold output can be provided by an on-board second-order (sin x)/x correction filter (see Functional Block Diagram). This (sin x)/x correction filter can be inserted into or omitted from the signal path by digital-signal-processor control (data bit D9 in the DX secondary communications). When inserted, the (sin x)/x correction filter precedes the switched-capacitor low-pass filter. When the TB register (see Figure 4) equals 15, the correction results of Figures 26, 27, and 28 can be obtained.

The (sin x)/x correction [see section (sin x)/x] can also be accomplished by disabling the on-board second-order correction filter and performing the (sin x)/x correction in digital signal processor software. The system frequency response can be corrected via DSP software to ± 0.1 dB accuracy to a band edge of 3000 Hz for all sampling rates. This correction is accomplished with a first-order digital correction filter, that requires seven TMS320 instruction cycles. With a 200-ns instruction cycle, seven instructions represent an overhead factor of 1.1% and 1.3% for sampling rates of 8 and 9.6 kHz, respectively (see the (sin x)/x Correction Section for more details).

(sin x)/x Correction

If the designer does not wish to use the on-board second-order (sin x)/x correction filter, correction can be accomplished in digital signal processor (DSP) software. (sin x)/x correction can be accomplished easily and efficiently in digital signal processor software. Excellent correction accuracy can be achieved to a band edge of 3000 Hz by using a first-order digital correction filter. The results shown below are typical of the numerical correction accuracy that can be achieved for sample rates of interest. The filter requires seven instruction cycles per sample on the TMS320 DS. With a 200-ns instruction cycle, nine instructions per sample represents an overhead factor of 1.4% and 1.7% for sampling rates of 8000 Hz and 9600 Hz, respectively. This correction adds a slight amount of group delay at the upper edge of the 300-Hz to 3000-Hz band.

(sin x)/x Roll-Off for a Zero-Order Hold Function

The (sin x)/x roll-off error for the AIC DAC zero-order hold function at a band-edge frequency of 3000 Hz for the various sampling rates is shown in Table 5 (see Figure 27).

Table 5. (sin x)/x Roll-Off Error

f_S (Hz)	Error = 20 log $\frac{\sin \pi f/f_S}{\pi f/f_S}$ f = 3000 Hz (dB)
7200	−2.64
8000	−2.11
9600	−1.44
14400	−0.63
16000	−0.50
19200	−0.35
25000	−0.21

The actual AIC (sin x)/x roll-off is slightly less than the figures above because the AIC has less than 100% duty cycle hold interval.

Correction Filter

To externally compensate for the (sin x)/x roll-off of the AIC, a first-order correction filter can be implemented as shown in Figure 11.

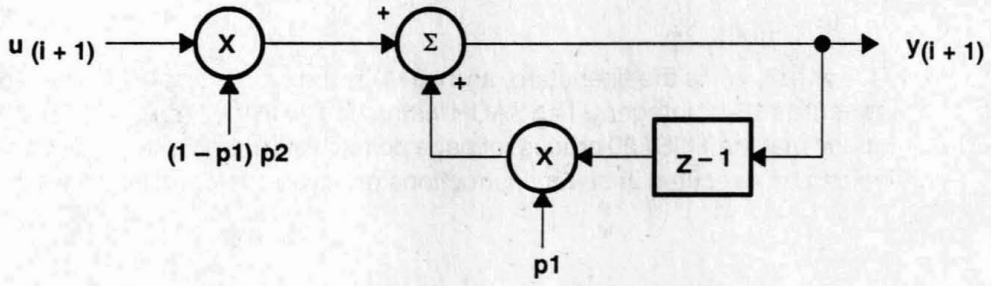


Figure 11. First-Order Correction Filter

The difference equation for this correction filter is:

$$y_{(i+1)} = p2 \cdot (1 - p1) \cdot u_{(i+1)} + p1 \cdot y_{(i)} \quad (4)$$

where the constant p1 determines the pole locations.

The resulting squared magnitude transfer function is:

$$|H(f)|^2 = \frac{(p2)^2 \cdot (1-p1)^2}{1-2 \cdot p1 \cdot \cos(2\pi f/f_S) + (p1)^2} \quad (5)$$

Correction Results

Table 5 shows the optimum p values and the corresponding correction results for 8000-Hz and 9600-Hz sampling rates (see Figures 26, 27, and 28).

Table 6. (sin x)/x Correction Table for f_S = 8000 Hz and f_S = 9600 Hz

f (Hz)	ROLL-OFF ERROR (dB) f_S = 8000 Hz p1 = −0.14813 p2 = 0.9888	ROLL-OFF ERROR (dB) f_S = 9600 Hz p1 = −0.1307 p2 = 0.9951
300	−0.099	−0.043
600	−0.089	−0.043
900	−0.054	0
1200	−0.002	0
1500	0.041	0
1800	0.079	0.043
2100	0.100	0.043
2400	0.091	0.043
2700	−0.043	0
3000	−0.102	−0.043

TMS320 Software Requirements

The digital correction filter equation can be written in state variable form as follows:

$$y_{(i+1)} = y_{(i)} \cdot k1 + u_{(i+1)} \cdot k2$$

where k1 = p1, k2 = (1 − p1)p2, y(i) is the filter state, and u(i+1) is the next I/O sample. The coefficients k1 and k2 must be represented as 16-bit integers. The SACH instruction (with the proper shift) yields the correct result. With the assumption that the TMS320 processor page pointer and memory configuration are properly initialized, the equation can be executed in seven instructions or seven cycles with the following program:

```
ZAC
LT K2
MPY U
LTA K1
MPY Y
APAC
SACH (dma), (shift)
```

Specifications

Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)

Supply voltage range, V_{CC+} (see Note 1) ..... −0.3 V to 15 V
Supply voltage range, V_{DD} ..... −0.3 V to 15 V
Output voltage range, V_O ..... −0.3 V to 15 V
Input voltage range, V_I ..... −0.3 V to 15 V
Digital ground voltage range ..... −0.3 V to 15 V
Operating free-air temperature range: TLC32046C ..... 0°C to 70°C
TLC32046I ..... −40°C to 85°C
Storage temperature range ..... −40°C to 125°C
Case temperature for 10 seconds: FN package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package ... 260°C

NOTE 1: Voltage values for maximum ratings are with respect to V_{CC-}.

Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} (see Note 2)		4.75	5	5.25	V
Supply voltage, V_{CC-} (see Note 2)		−4.75	−5	−5.25	V
Digital supply voltage, V_{DD} (see Note 2)		4.75	5	5.25	V
Digital ground voltage with respect to ANLG GND, DGTL GND			0		V
Reference input voltage, $V_{ref(ext)}$ (see Note 2)		2		4	V
High-level input voltage, V_{IH}		2		V_{DD}+0.3	V
Low-level input voltage, V_{IL} (see Note 3)		−0.3		0.8	V
Load resistance at OUT+ and/or OUT−, R_L		300			Ω
Load capacitance at OUT+ and/or OUT−, C_L				100	pF
MSTR CLK frequency (see Note 4)			5	10.368	MHz
Analog input amplifier common mode input voltage (see Note 5)				±1.5	V
A/D or D/A conversion rate				25	kHz
Operating free-air temperature range, T_A	TLC32046C	0		70	°C
	TLC32046I	−40		85	

NOTES: 2. Voltages at analog inputs and outputs, REF, V_{CC+}, and V_{CC-} are with respect to the ANLG GND terminal. Voltages at digital inputs and outputs and V_{DD} are with respect to the DGTL GND terminal.

3. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data manual for logic voltage levels only.
4. The band-pass switched-capacitor filter (SCF) specifications apply only when the low-pass section SCF clock is 288 kHz and the high-pass section SCF clock is 16 kHz. If the low-pass SCF clock is shifted from 288 kHz, the low-pass roll-off frequency shifts by the ratio of the low-pass SCF clock to 288 kHz. If the high-pass SCF clock is shifted from 16 kHz, the high-pass roll-off frequency shifts by the ratio of the high-pass SCF clock to 16 kHz. Similarly, the low-pass switched-capacitor filter (SCF) specifications apply only when the SCF clock is 288 kHz. If the SCF clock is shifted from 288 kHz, the low-pass roll-off frequency shifts by the ratio of the SCF clock to 288 kHz.
5. This range applies when (IN+ – IN−) or (AUX IN+ – AUX IN−) equals ± 6 V.

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (Unless Otherwise Noted)

total device, MSTR CLK frequency = 5.184 MHz, outputs not loaded

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 4.75 V, I_{OH} = −300 μA	2.4			V
V_{OL}	Low-level output voltage		V_{DD} = 4.75 V, I_{OL} = 2 mA			0.4	V
I_{CC+}	Supply current from V_{CC+}	TLC32046C				35	mA
		TLC32046I				40	
I_{CC-}	Supply current from V_{CC-}	TLC32046C				−35	mA
		TLC32046I				−40	
I_{DD}	Supply current from V_{DD}					7	mA
V_{ref}	Internal reference output voltage			3		3.3	V
α_{Vref}	Temperature coefficient of internal reference voltage				250		ppm/°C
r_o	Output resistance at REF				100		kΩ

power supply rejection and crosstalk attenuation

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{CC+} or V_{CC-} supply voltage rejection ratio, receive channel	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at DR (ADC output)		30		dB
	f = 30 kHz to 50 kHz			45		
V_{CC+} or V_{CC-} supply voltage rejection ratio, transmit channel (single-ended)	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at OUT+		30		dB
	f = 30 kHz to 50 kHz			45		
Crosstalk attenuation, transmit-to-receive (single-ended)				80		dB

serial port

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −300 μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4	V
I_I	Input current				±10	μA
I_I	Input current, DATA-DR/CONTROL				±100	μA
C_i	Input capacitance			15		pF
C_o	Output capacitance			15		pF

† All typical values are at T_A = 25°C.

receive amplifier input

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	A/D converter offset error (filters in)			10	70	mV
CMRR	Common-mode rejection ratio at IN+, IN−, or AUX IN+, AUX IN−	See Note 6		55		dB
r_I	Input resistance at IN+, IN− or AUX IN+, AUX IN−, REF			100		kΩ

NOTE 6: The test condition is a 0-dBm, 1-kHz input signal with a 16-kHz conversion rate.

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (Unless Otherwise Noted) (Continued)

transmit filter output

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OO}	Output offset voltage at OUT+ or OUT− (single-ended relative to ANLG GND)			15	80	mV
V_{OM}	Maximum peak output voltage swing across R_L at OUT+ or OUT− (single-ended)	$R_L \geq 300\ \Omega$, Offset voltage = 0	±3			V
V_{OM}	Maximum peak output voltage swing between OUT+ and OUT− (differential output)	$R_L \geq 600\ \Omega$	±6			V

† All typical values are at T_A = 25°C.

receive and transmit channel system distortion, SCF clock frequency = 288 kHz (see Note 7)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Attenuation of second harmonic of A/D input signal	single-ended	V_{in} = −0.1 dB to −24 dB		70		dB
	differential		62	70		
Attenuation of third and higher harmonics of A/D input signal	single-ended			65		dB
	differential		57	65		
Attenuation of second harmonic of D/A input signal	single-ended	V_{in} = −0 dB to −24 dB		70		dB
	differential		62	70		
Attenuation of third and higher harmonics of D/A input signal	single-ended			65		dB
	differential		57	65		

† All typical values are at T_A = 25°C.

receive channel signal-to-distortion ratio (see Note 7)

PARAMETER	TEST CONDITIONS	A_V = 1‡		A_V = 2‡		A_V = 4‡		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
A/D channel signal-to-distortion ratio	V_{in} = −6 dB to −0.1 dB	58		§		§		dB
	V_{in} = −12 dB to −6 dB	58		58		§		
	V_{in} = −18 dB to −12 dB	56		58		58		
	V_{in} = −24 dB to −18 dB	50		56		58		
	V_{in} = −30 dB to −24 dB	44		50		56		
	V_{in} = −36 dB to −30 dB	38		44		50		
	V_{in} = −42 dB to −36 dB	32		38		44		
	V_{in} = −48 dB to −42 dB	26		32		38		
	V_{in} = −54 dB to −48 dB	20		26		32		

‡ A_V is the programmable gain of the input amplifier.

§ Measurements under these conditions are unreliable due to overrange and signal clipping.

NOTE 7: The test condition is a 1-kHz input signal with a 16-kHz conversion rate. The load impedance for the DAC is 600 Ω. Input and output voltages are referred to V_{ref}.

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (Unless Otherwise Noted) (Continued)

transmit channel signal-to-distortion ratio (see Note 7)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
D/A channel signal-to-distortion ratio	V_{in} = −6 dB to −0.1 dB	58		dB
	V_{in} = −12 dB to −6 dB	58		
	V_{in} = −18 dB to −12 dB	56		
	V_{in} = −24 dB to −18 dB	50		
	V_{in} = −30 dB to −24 dB	44		
	V_{in} = −36 dB to −30 dB	38		
	V_{in} = −42 dB to −36 dB	32		
	V_{in} = −48 dB to −42 dB	26		
	V_{in} = −54 dB to −48 dB	20		

NOTE 7: The test condition is a 1-kHz input signal with a 16-kHz conversion rate. The load impedance for the DAC is 600 Ω. Input and output voltages are referred to V_{ref}.

receive and transmit gain and dynamic range (see Note 8)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit gain tracking error	V_{out} = −48 dB to 0 dB signal range		±0.05	±0.15	dB
Receive gain tracking error	V_{in} = −48 dB to 0 dB signal range		±0.05	±0.15	dB

NOTE 8: Gain tracking is relative to the absolute gain at 1 kHz and 0 dB (0 dB relative to V_{ref}).

receive channel band-pass filter transfer function, SCF f_{clock} = 288 kHz, input (IN+ – IN–) is a ±3-V sine wave‡ (see Note 9)

PARAMETER	TEST CONDITION	FREQUENCY	ADJUSTMENT	MIN	TYP†	MAX	UNIT
Filter gain	Input signal reference is 0 dB	f ≤ 100 Hz	K1 × 0 dB	−33	−29	−25	dB
		f = 200 Hz	K1 × −0.26 dB	−4	−2	−1	
		f = 300 Hz to 6200 Hz	K1 × 0 dB	−0.25	0	0.25	
		f = 6200 Hz to 6600 Hz	K1 × 0 dB	−0.3	0	0.3	
		f = 6600 Hz to 7300 Hz	K1 × 0 dB	−0.5	0	0.5	
		f = 7600 Hz	K1 × 2.3 dB	−5	−2	−0.5	
		f = 8000 Hz	K1 × 2.7 dB		−16	−14	
		f ≥ 8800 Hz	K1 × 3.2 dB			−40	
		f ≥ 10000 Hz	K1 × 0 dB			−65	

† All typical values are at T_A = 25°C.

‡ The MIN, TYP, and MAX specifications are given for a 288-kHz SCF clock frequency. A slight error in the 288-kHz SCF may result from inaccuracies in the MSTR CLK frequency, resulting from crystal frequency tolerances. If this frequency error is less than 0.25%, the ADJUSTMENT ADDEND should be added to the MIN, TYP, and MAX specifications, where K1 = 100 • [(SCF frequency – 288 kHz)/288 kHz]. For errors greater than 0.25%, see Note 9.

NOTE 9: The filter gain outside of the pass band is measured with respect to the gain at 1 kHz. The filter gain within the pass band is measured with respect to the average gain within the pass band. The pass bands are 300 Hz to 7200 Hz and 0 to 7200 Hz for the band-pass and low-pass filters, respectively. For switched-capacitor filter clocks at frequencies other than 288 kHz, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 288 kHz.

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (Unless Otherwise Noted) (Continued)

receive and transmit channel low-pass filter transfer function, SCF f_{clock} = 288 kHz (see Note 9)

PARAMETER	TEST CONDITION	FREQUENCY RANGE	ADJUSTMENT ADDEND‡	MIN	TYP†	MAX	UNIT
Filter gain	Input signal reference is 0 dB	f = 0 Hz to 6200 Hz	K1 × 0 dB	−0.25	0	0.25	dB
		f = 6200 Hz to 6600 Hz	K1 × 0 dB	−0.3	0	0.3	
		f = 6600 Hz to 7300 Hz	K1 × 0 dB	−0.5	0	0.5	
		f = 7600 Hz	K1 × 2.3 dB	−5	−2	−0.5	
		f = 8000 Hz	K1 × 2.7 dB		−16	−14	
		f ≥ 8800 Hz	K1 × 3.2 dB			−40	
		f ≥ 10000 Hz	K1 × 0 dB			−65	

† All typical values are at T_A = 25°C.

‡ The MIN, TYP, and MAX specifications are given for a 288-kHz SCF clock frequency. A slight error in the 288-kHz SCF may result from inaccuracies in the MSTR CLK frequency, resulting from crystal frequency tolerances. If this frequency error is less than 0.25%, the ADJUSTMENT ADDEND should be added to the MIN, TYP, and MAX specifications, where K1 = 100 • [(SCF frequency – 288 kHz)/288 kHz]. For errors greater than 0.25%, see Note 9.

NOTE 9: The filter gain outside of the pass band is measured with respect to the gain at 1 kHz. The filter gain within the pass band is measured with respect to the average gain within the pass band. The pass bands are 300 Hz to 7200 Hz and 0 to 7200 Hz for the band-pass and low-pass filters, respectively. For switched-capacitor filter clocks at frequencies other than 288 kHz, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 288 kHz.

Operating Characteristics Over Recommended Operating Free-Air Temperature Range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V

receive and transmit noise (measurement includes low-pass and band-pass switched-capacitor filters)

PARAMETER		TEST CONDITIONS	TYP†	MAX	UNIT
Transmit noise	broadband with (sin x)/x	DX input = 00000000000000, constant input code	250	500	μV rms
	broadband without (sin x)/x		200	450	
	0 to 30 kHz with (sin x)/x		200	400	
	0 to 30 kHz without (sin x)/x		200	400	
	0 to 3.4 kHz with (sin x)/x		180	300	
	0 to 3.4 kHz without (sin x)/x		160	300	
	0 to 6.8 kHz with (sin x)/x [wide-band operation with 7.2 kHz roll-off]		180	350	
	0 to 6.8 kHz without (sin x)/x [wide-band operation with 7.2 kHz roll-off]		160	350	
Receive noise (see Note 10)		Inputs grounded, gain = 1	300	500	μV rms
			18		dBrnc0

† All typical values are at T_A = 25°C.

NOTE 10: The noise is computed by statistically evaluating the digital output of the A/D converter.

Timing Requirements

serial port recommended input signals

PARAMETER		MIN	MAX	UNIT
$t_{c(MCLK)}$	Master clock cycle time	95		ns
$t_{r(MCLK)}$	Master clock rise time		10	ns
$t_{f(MCLK)}$	Master clock fall time		10	ns
	Master clock duty cycle	25%	75%	
	$\overline{\text{RESET}}$ pulse duration (see Note 11)	800		ns
$t_{su(DX)}$	DX setup time before SCLK↓	20		ns
$t_{h(DX)}$	DX hold time after SCLK↓	$t_{c(SCLK)}/4$		ns

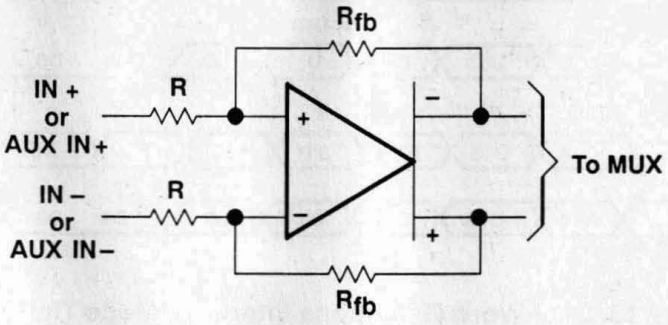
NOTE 11: $\overline{\text{RESET}}$ pulse duration is the amount of time that the reset pin is held below 0.8 V after the power supplies have reached their recommended values.

serial port – AIC output signals, C_L = 30 pF for SHIFT CLK output, C_L = 15 pF for all other outputs

PARAMETER		MIN	TYP†	MAX	UNIT
$t_{c(SCLK)}$	Shift clock (SCLK) cycle time	380			ns
$t_{f(SCLK)}$	Shift clock (SCLK) fall time		3	8	ns
$t_{r(SCLK)}$	Shift clock (SCLK) rise time		3	8	ns
	Shift clock (SCLK) duty cycle	45		55	%
$t_{d(CH-FL)}$	Delay from SCLK↑ to $\overline{\text{FSR}}/\overline{\text{FSX}}/\overline{\text{FSD}}$↓		30		ns
$t_{d(CH-FH)}$	Delay from SCLK↑ to $\overline{\text{FSR}}/\overline{\text{FSX}}/\overline{\text{FSD}}$↑		35	90	ns
$t_{d(CH-DR)}$	DR valid after SCLK↑			90	ns
$t_{d(CH-EL)}$	Delay from SCLK↑ to $\overline{\text{EODX}}/\overline{\text{EODR}}$↓ in word mode			90	ns
$t_{d(CH-EH)}$	Delay from SCLK↑ to $\overline{\text{EODX}}/\overline{\text{EODR}}$↑ in word mode			90	ns
$t_{f(EODX)}$	$\overline{\text{EODX}}$ fall time		2	8	ns
$t_{f(EODR)}$	$\overline{\text{EODR}}$ fall time		2	8	ns
$t_{d(CH-EL)}$	Delay from SCLK↑ to $\overline{\text{EODX}}/\overline{\text{EODR}}$↓ in byte mode			90	ns
$t_{d(CH-EH)}$	Delay from SCLK↑ to $\overline{\text{EODX}}/\overline{\text{EODR}}$↑ in byte mode			90	ns
$t_{d(MH-SL)}$	Delay from MSTR CLK↑ to SCLK↓		65	170	ns
$t_{d(MH-SH)}$	Delay from MSTR CLK↑ to SCLK↑		65	170	ns

† Typical values are at T_A = 25°C.

Parameter Measurement Information



R_{fb} = R for D6 = 1 and D7 = 1
D6 = 0 and D7 = 0
R_{fb} = 2R for D6 = 1 and D7 = 0
R_{fb} = 4R for D6 = 0, and D7 = 1

Figure 12. IN+ and IN– Gain Control Circuitry

Table 7. Gain Control Table (Analog Input Signal Required for Full-Scale Bipolar A/D Conversion Twos Complement)†

INPUT CONFIGURATIONS	CONTROL REGISTER BITS		ANALOG INPUT‡§	A/D CONVERSION RESULT
	D6	D7		
Differential configuration Analog input = IN+ – IN– = AUX IN+ – AUX IN–	1 0	1 0	V_{ID} = ±6 V	±full scale
	1	0	V_{ID} = ±3 V	±full scale
	0	1	V_{ID} = ±1.5 V	±full scale
Single-ended configuration Analog input = IN+ – ANLG GND = AUX IN+ – ANLG GND	1 0	1 0	V_I = ±3 V	±half scale
	1	0	V_I = ±3 V	±full scale
	0	1	V_I = ±1.5 V	±full scale

† V_{CC+} = 5 V, V_{CC-} = –5 V, V_{DD} = 5 V
‡ V_{ID} = Differential Input Voltage, V_I = Input voltage referenced to ground with IN– or AUX IN– connected to ground.
§ In this example, V_{ref} is assumed to be 3 V. In order to minimize distortion, it is recommended that the analog input not exceed 0.1 dB below full scale.

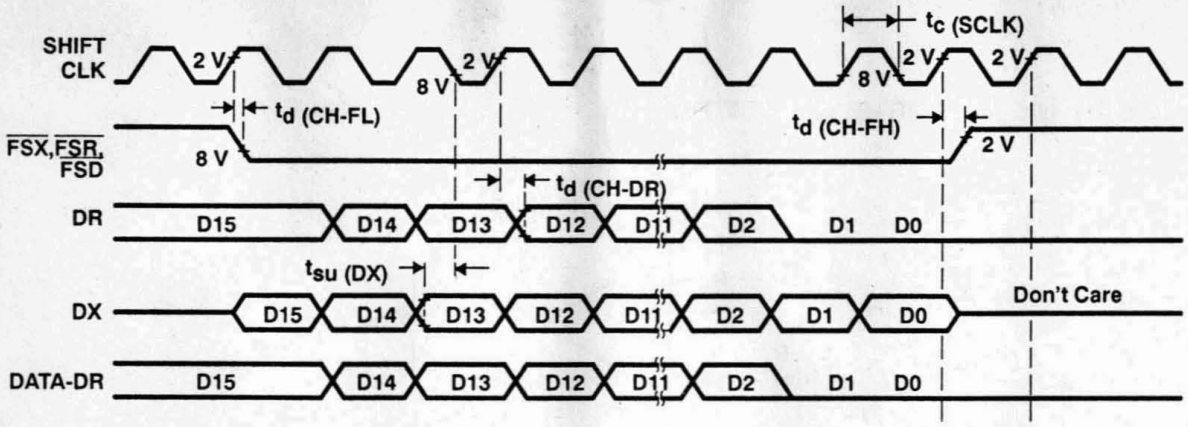


Figure 13. Dual-Word (Telephone Interface) Mode Timing

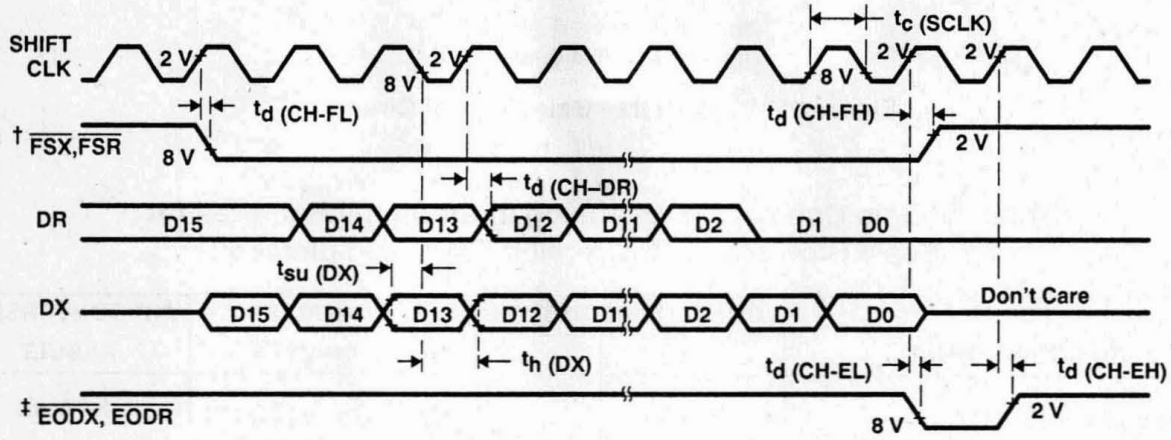


Figure 14. Word Timing

† The time between falling edges of $\overline{FSR}$ is the A/D conversion period and the time between falling edges of $\overline{FSX}$ is the D/A conversion period.

‡ In the word format, $\overline{EODX}$ and $\overline{EODR}$ go low to signal the end of a 16-bit data word to the processor. The word-cycle is 20 shift-clocks wide, giving a four-clock period setup time between data words.

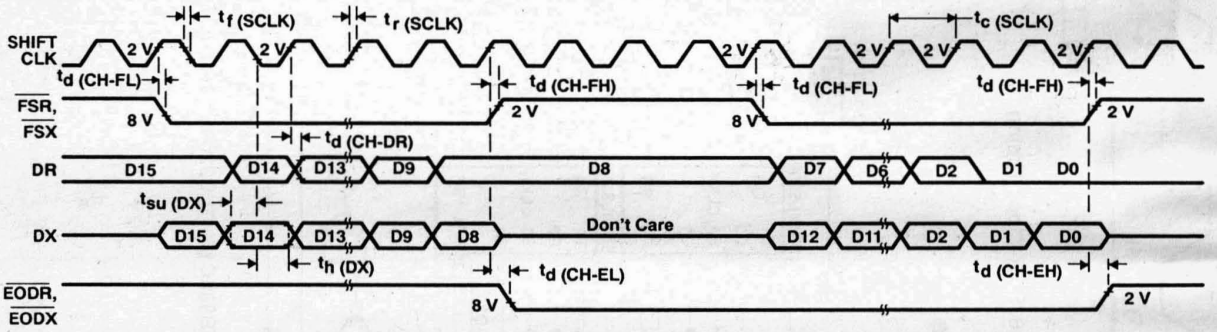


Figure 15. Byte-Mode Timing

†The time between falling edges of FSR is the A/D conversion period, and the time between fallling edges of $\overline{\text{FSX}}$ is the D/A conversion period.

‡In the byte mode, when $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ is high, the first byte is transmitted or received, and when these signals are low, the second byte is transmitted or received. Each byte-cycle is 12 shift-clocks long, allowing for a four-shift-clock setup time between byte transmissions.

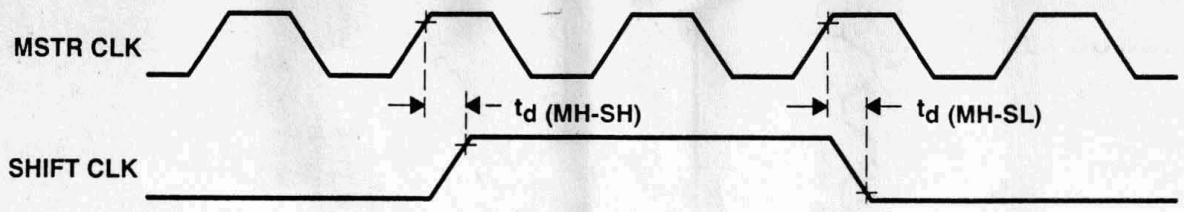


Figure 16. Shift-Clock Timing

TMS32046 – Processor Interface

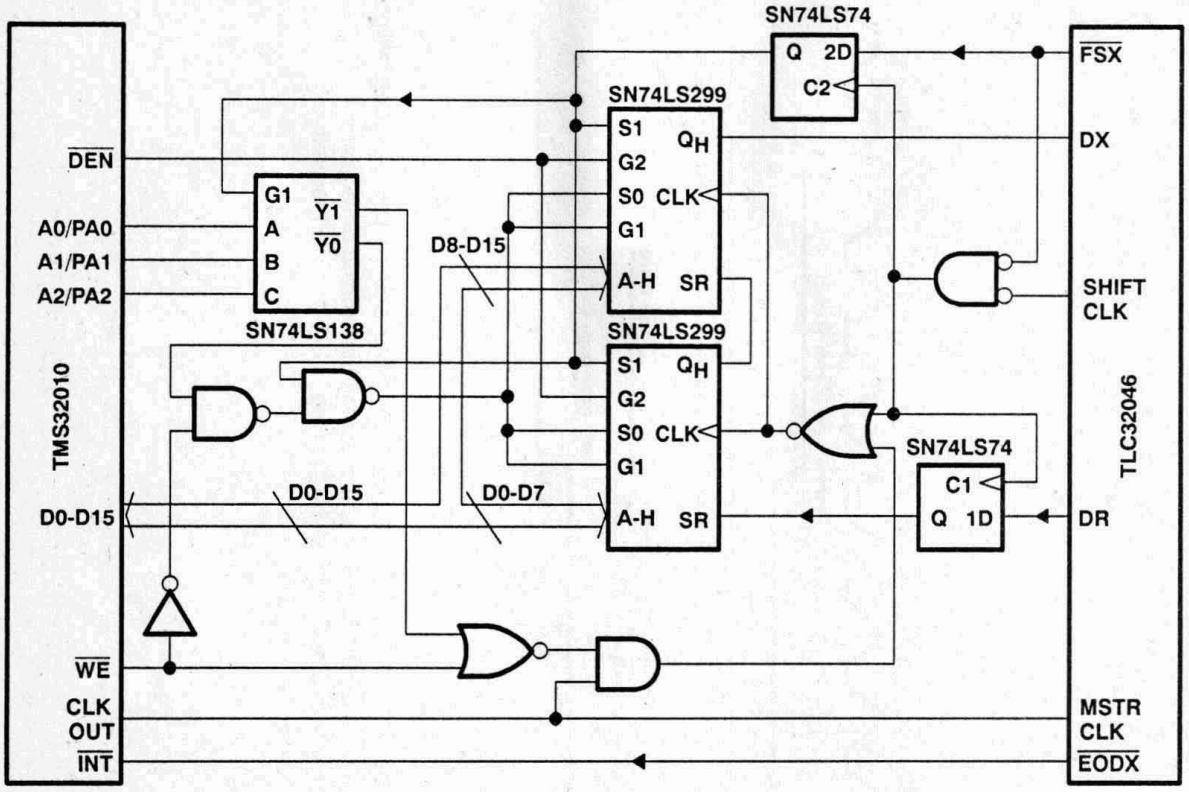
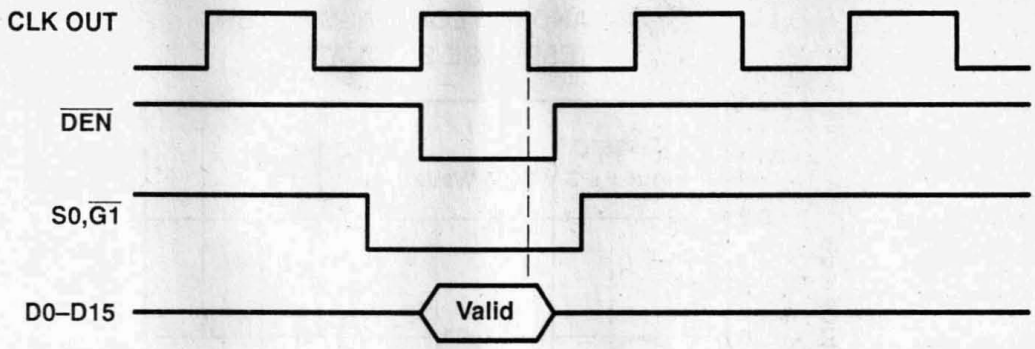


Figure 17. TMS32010/TMS320C15–TLC32046 Interface Circuit

IN instruction timing



OUT instruction timing

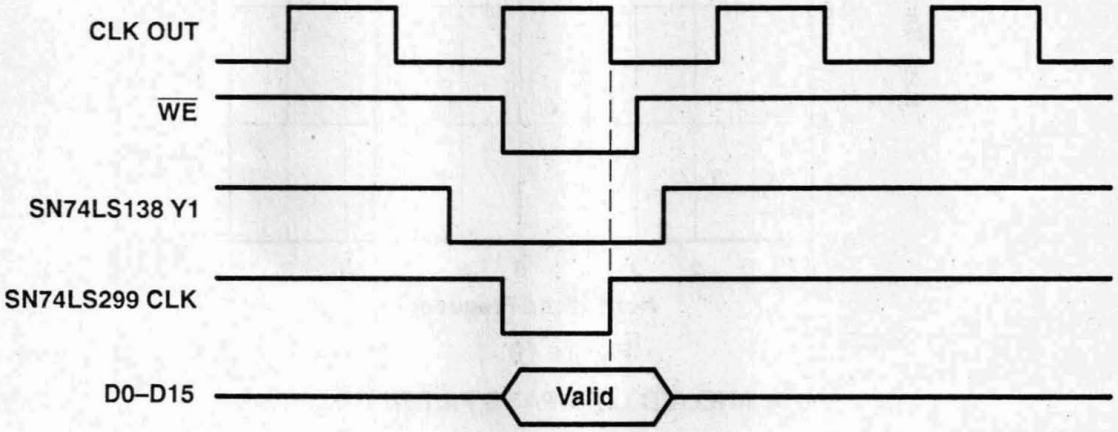


Figure 18. TMS32010/TMS320C15–TLC32046 Interface Timing

Typical Characteristics

D/A AND A/D LOW-PASS FILTER RESPONSE SIMULATION

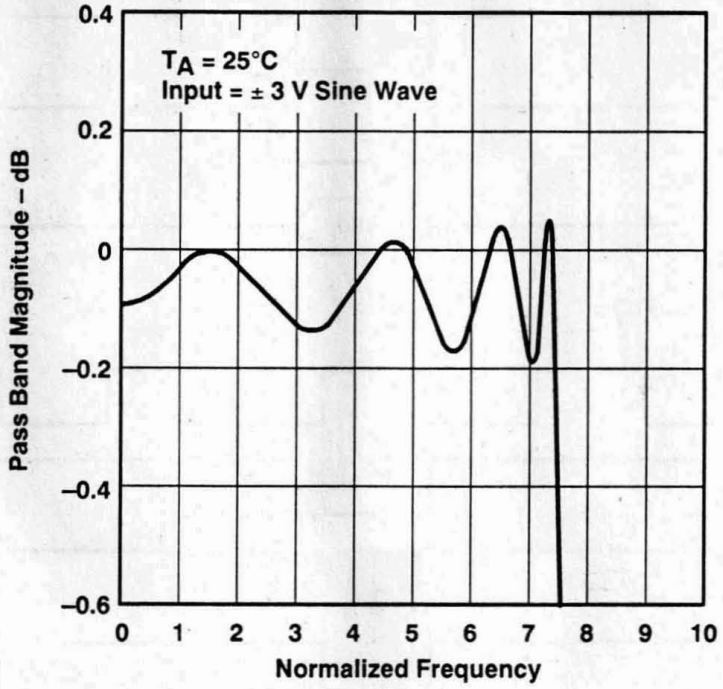


Figure 19

D/A AND A/D LOW-PASS FILTER RESPONSE

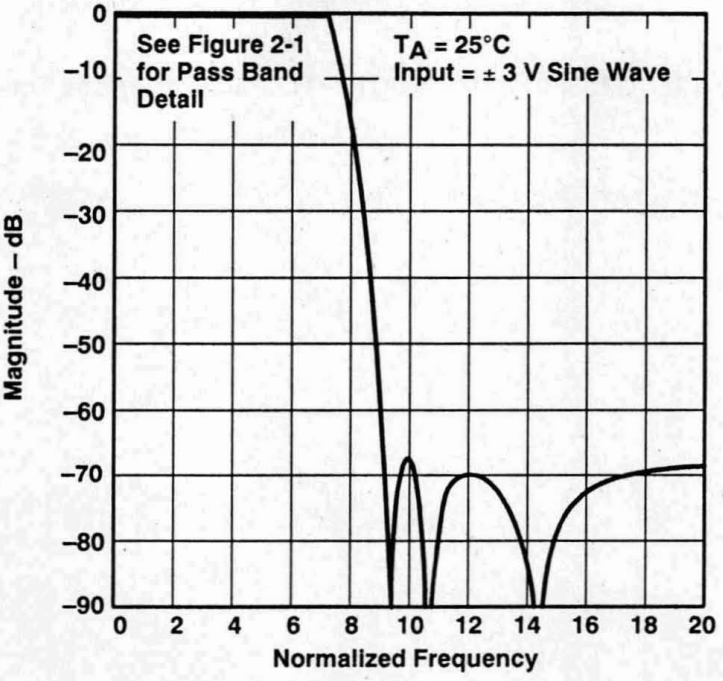


Figure 20

NOTE : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{SCF } f_{clock} \text{ (kHz)}}{288}$

D/A AND A/D LOW-PASS GROUP DELAY

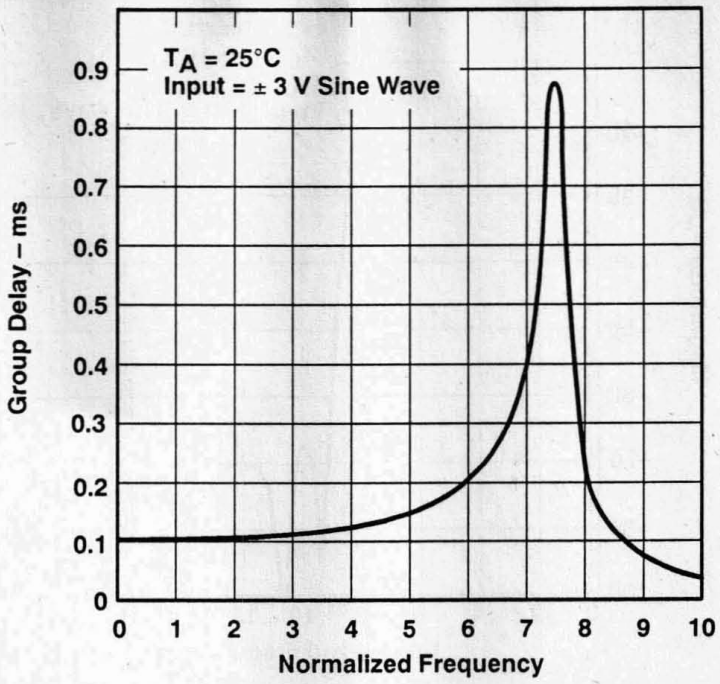


Figure 21

A/D BAND-PASS RESPONSE

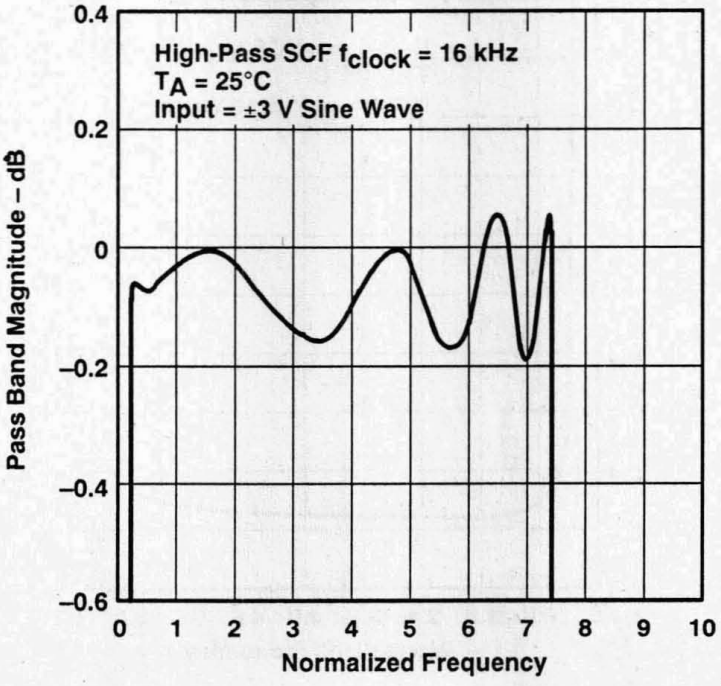


Figure 22

NOTE : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{SCF } f_{clock} \text{ (kHz)}}{288}$

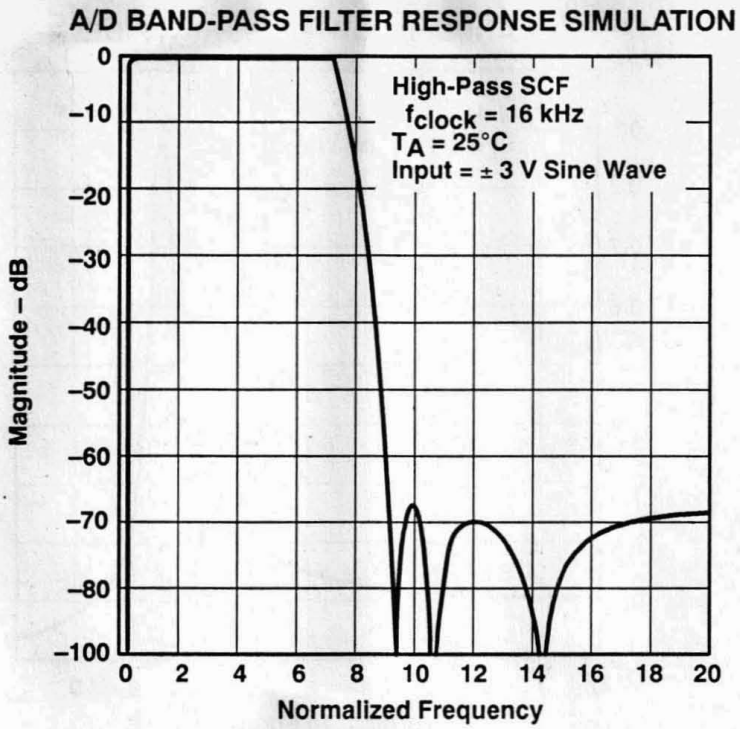


Figure 23

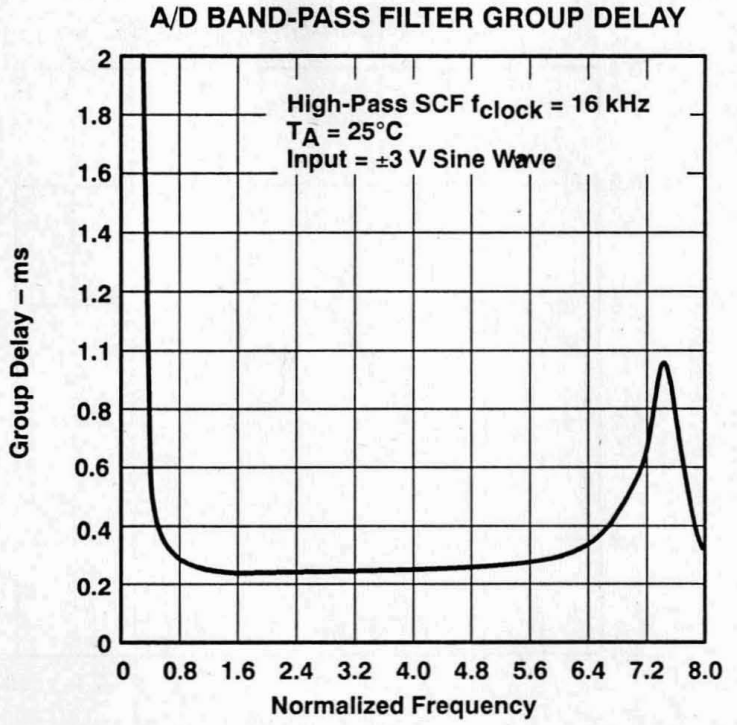


Figure 24

NOTE : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{SCF } f_{clock} \text{ (kHz)}}{288}$

A/D CHANNEL HIGH-PASS FILTER

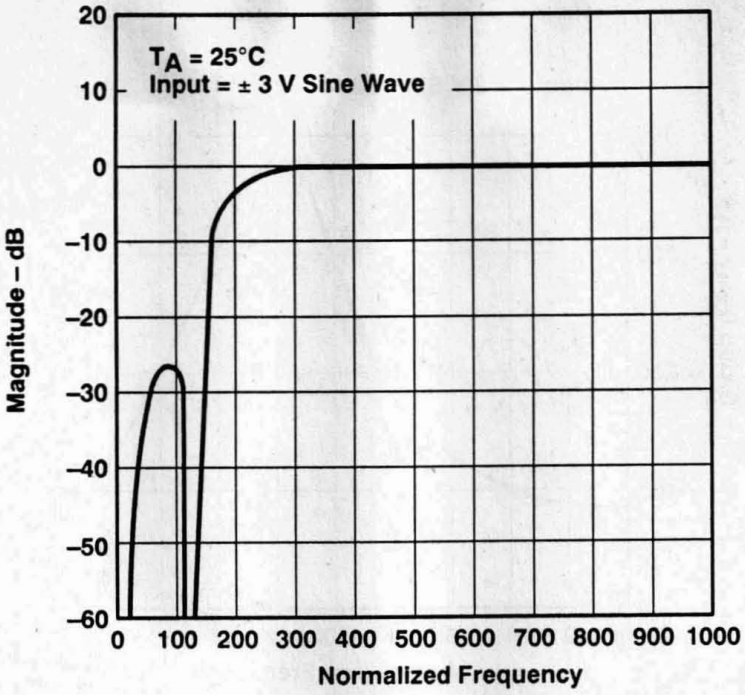


Figure 25

D/A (sin x)/x CORRECTION FILTER RESPONSE

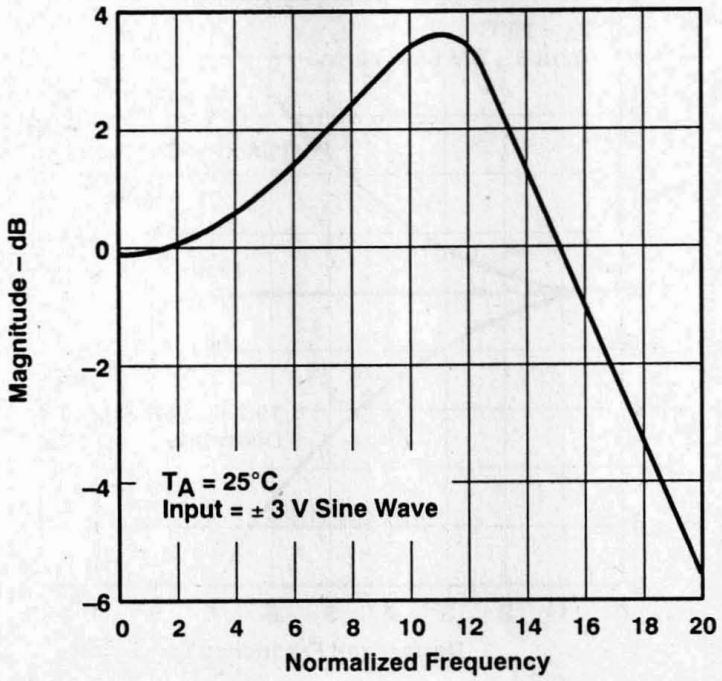


Figure 26

NOTE : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{SCF } f_{clock} \text{ (kHz)}}{288}$

D/A (sin x)/x CORRECTION FILTER RESPONSE

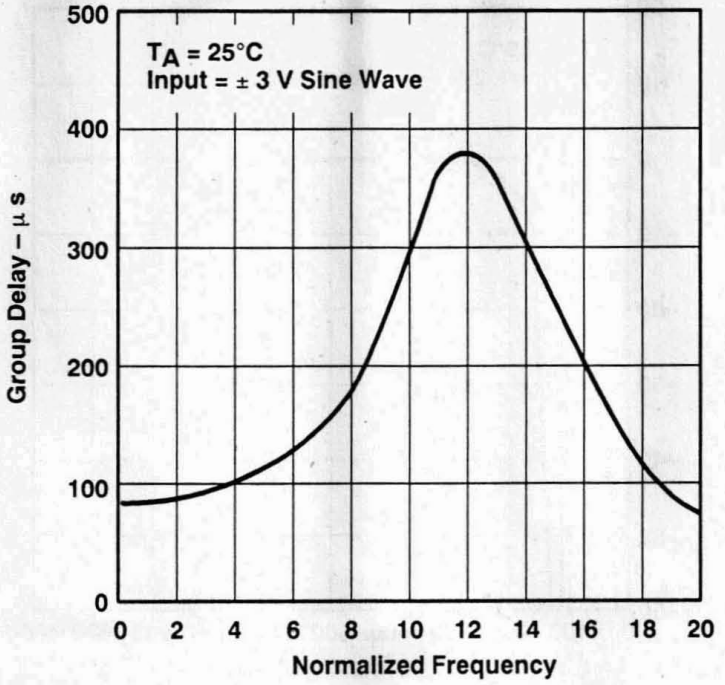


Figure 27

D/A (sin x)/x CORRECTION ERROR

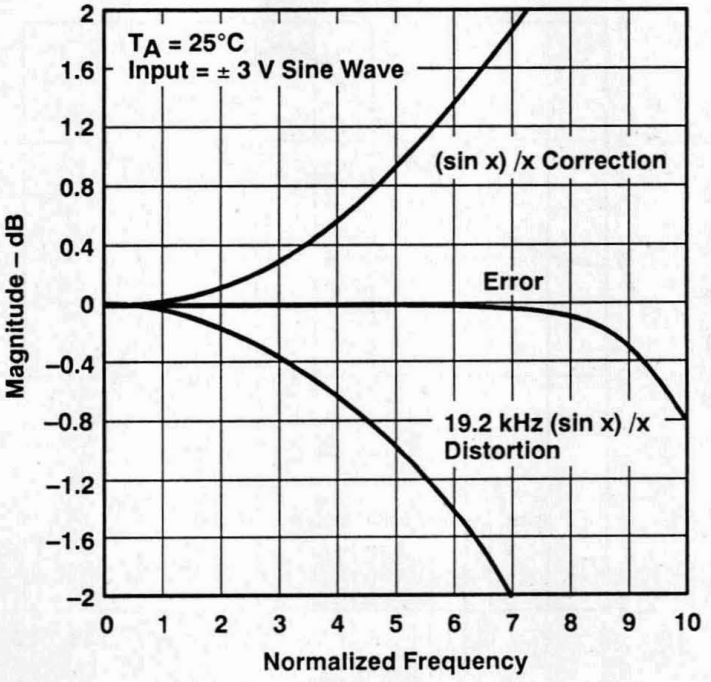


Figure 28

NOTE : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{SCF } f_{clock} \text{ (kHz)}}{288}$

A/D BAND-PASS GROUP DELAY

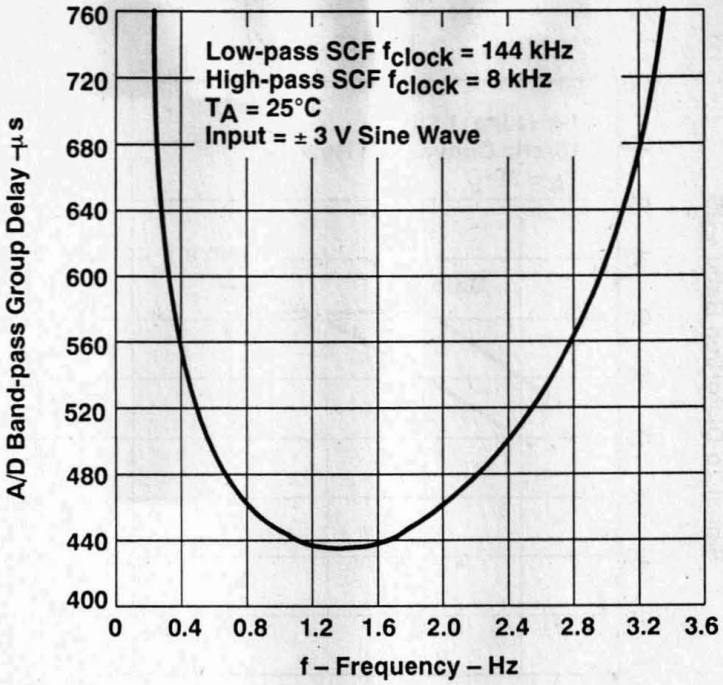


Figure 29

D/A LOW-PASS GROUP DELAY

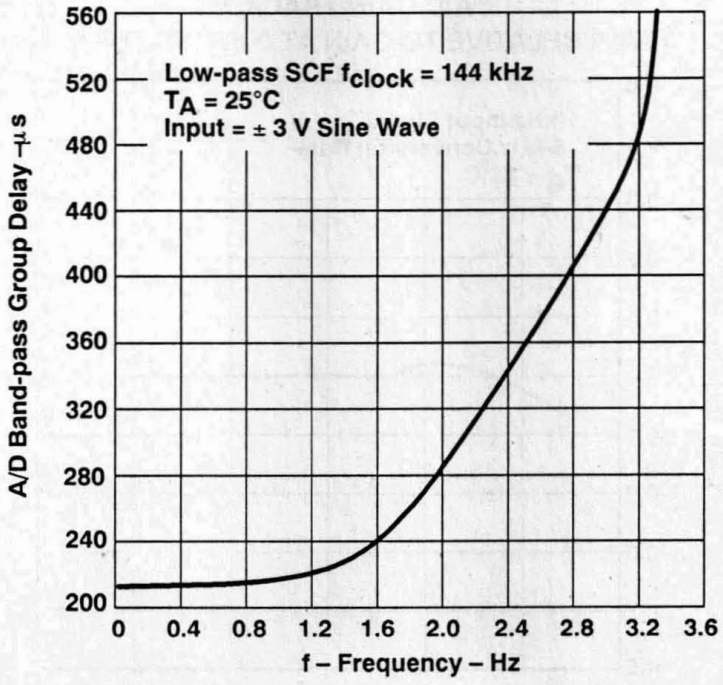


Figure 30

A/D SIGNAL-TO-DISTORTION RATIO vs INPUT SIGNAL

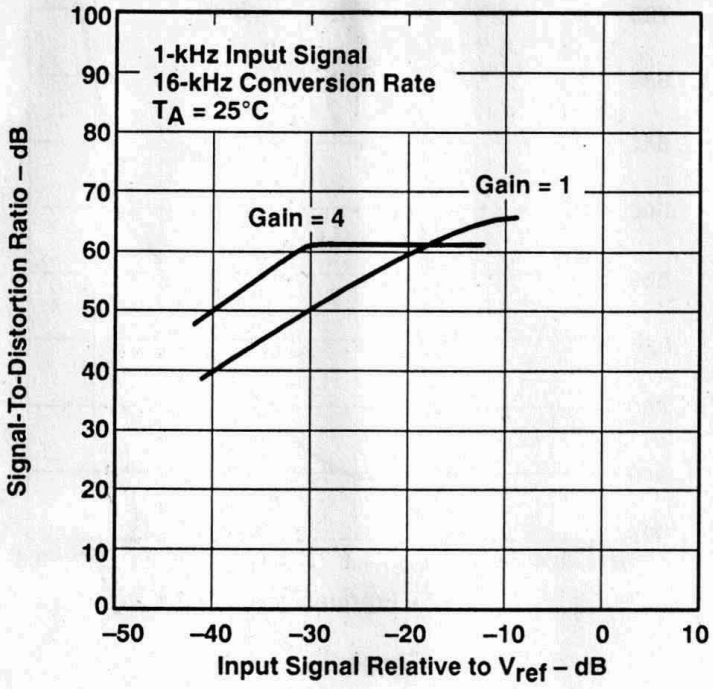


Figure 31

A/D GAIN TRACKING (GAIN RELATIVE TO GAIN AT 0-dB INPUT SIGNAL)

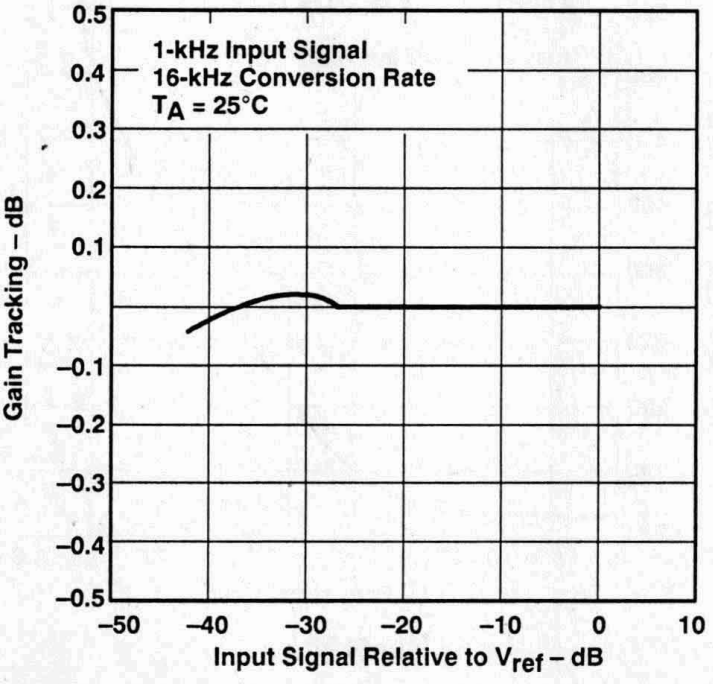


Figure 32

D/A CONVERTER SIGNAL-TO-DISTORTION RATIO vs INPUT SIGNAL

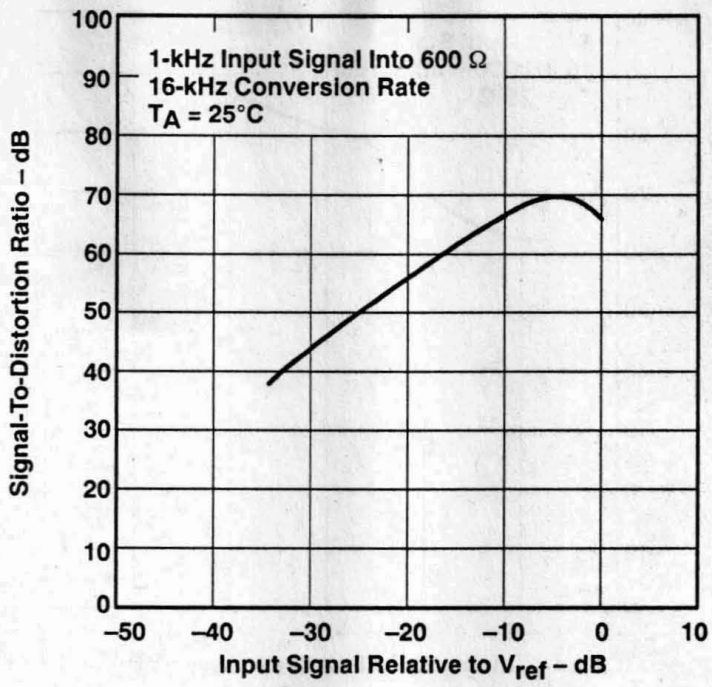


Figure 33

D/A GAIN TRACKING (GAIN RELATIVE TO GAIN AT 0-dB INPUT SIGNAL)

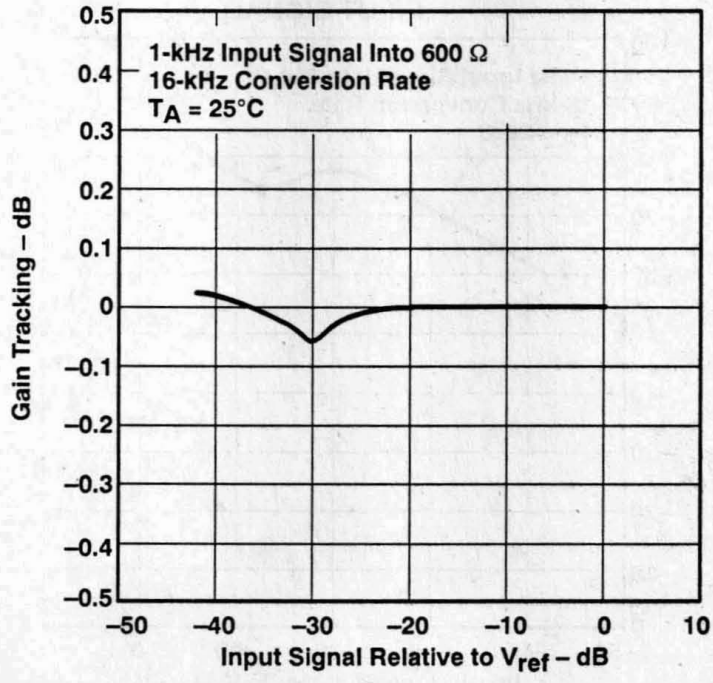


Figure 34

A/D SECOND HARMONIC DISTORTION
vs
INPUT SIGNAL

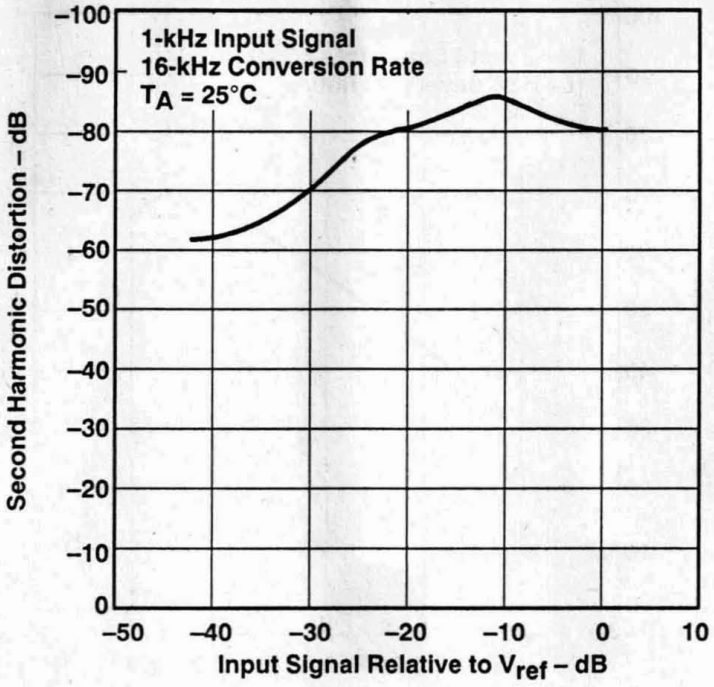


Figure 35

D/A SECOND HARMONIC DISTORTION
vs
INPUT SIGNAL

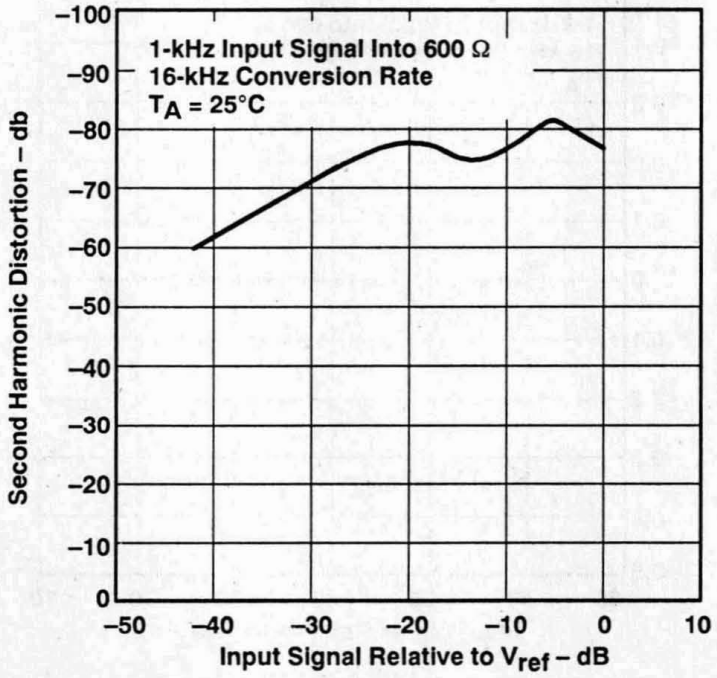


Figure 36

A/D THIRD HARMONIC DISTORTION
vs
INPUT SIGNAL

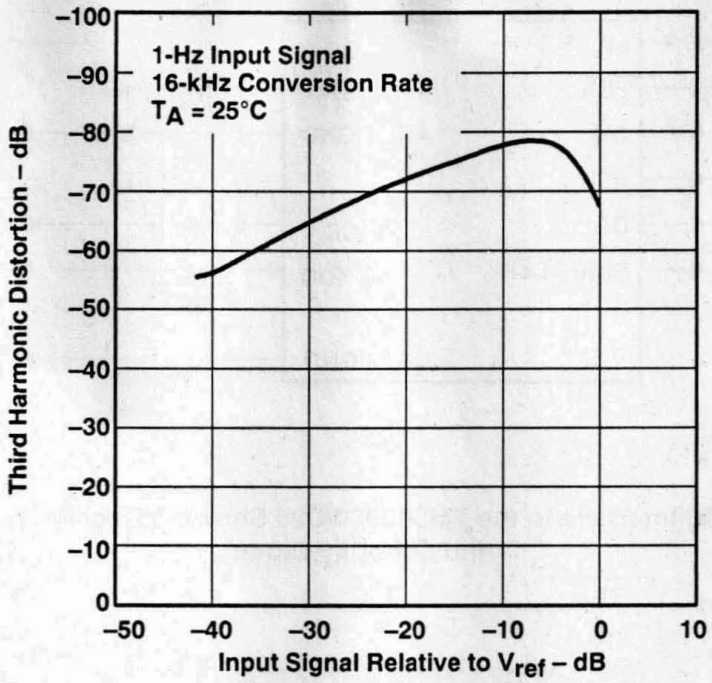


Figure 37

D/A THIRD HARMONIC DISTORTION
vs
INPUT SIGNAL

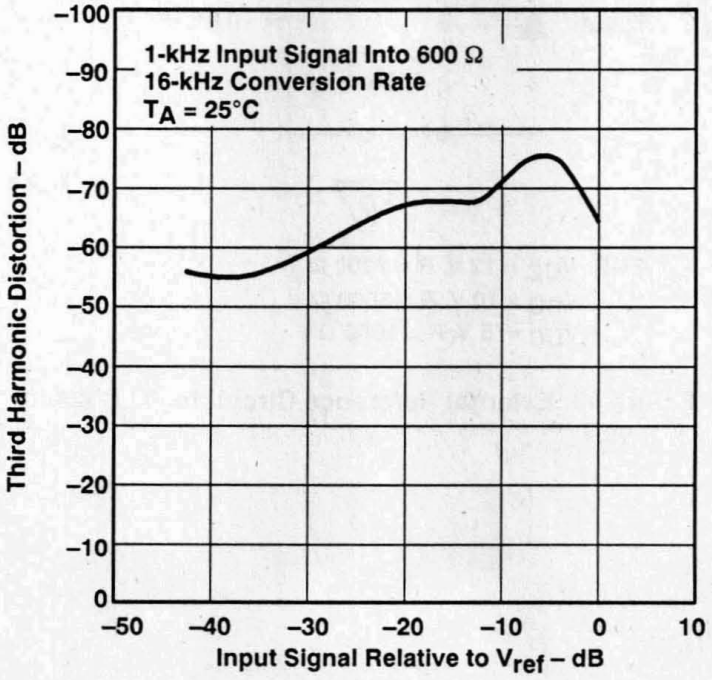


Figure 38

Application Information

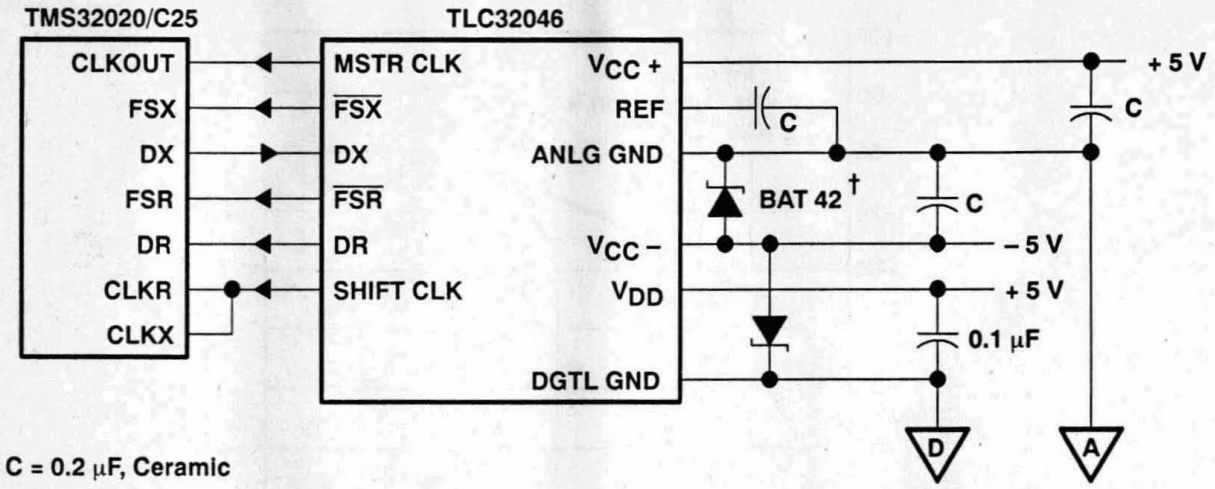
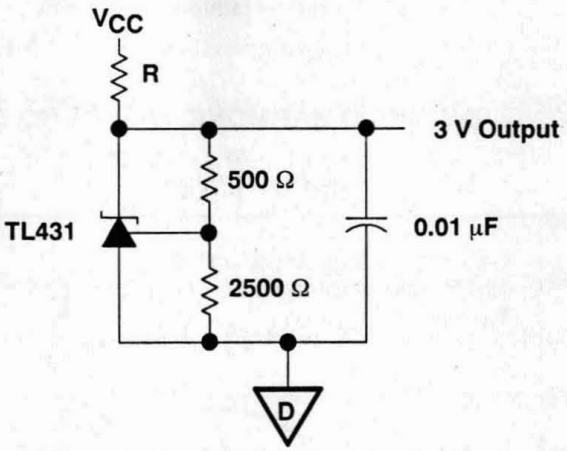


Figure 39. AIC Interface to the TMS32020/C25 Showing Decoupling Capacitors and Schottky Diode†

† Thomson Semiconductors



FOR: V_{CC} = 12 V, R = 7200 Ω
V_{CC} = 10 V, R = 5600 Ω
V_{CC} = 5 V, R = 1600 Ω

Figure 40. External Reference Circuit for TLC32046

TLC32047

Wide-Band Analog Interface Circuit

Data Manual

TEXAS INSTRUMENTS

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Introduction

The TLC32047 wide-band analog interface circuit (AIC) is a complete analog-to-digital and digital-to-analog interface system for advanced digital signal processors (DSPs) similar to the TMS32020, TMS320C25, and TMS320C30. The TLC32047 offers a powerful combination of options under DSP control: three operating modes (dual-word [telephone interface], word, and byte) combined with two word formats (8 bits and 16 bits) and synchronous or asynchronous operation. It provides a high level of flexibility in that conversion and sampling rates, filter bandwidths, input circuitry, receive and transmit gains, and multiplexed analog inputs are under processor control.

This AIC features a

- band-pass switched-capacitor antialiasing input filter
- 14-bit-resolution A/D converter
- 14-bit-resolution D/A converter
- low-pass switched-capacitor output-reconstruction filter.

The antialiasing input filter comprises eighth-order and fourth-order CC-type (Chebyshev/elliptic transitional) low-pass and high-pass filters, respectively. The input filter is implemented in switched-capacitor technology and is preceded by a continuous time filter to eliminate any possibility of aliasing caused by sampled data filtering. When low-pass filtering is desired, the high-pass filter can be switched out of the signal path. A selectable auxiliary differential analog input is provided for applications where more than one analog input is required.

The output-reconstruction filter is an eighth-order CC-type (Chebyshev/elliptic transitional low-pass filter) followed by a second-order (sin x)/x correction filter and is implemented in switched-capacitor technology. This filter is followed by a continuous-time filter to eliminate images of the sample data signal. The on-board (sin x)/x correction filter can be switched out of the signal path using digital signal processor control.

The A/D and D/A architectures ensure no missing codes and monotonic operation. An internal voltage reference is provided to ease the design task and to provide complete control over the performance of the IC. The internal voltage reference is brought out to pin 8. Separate analog and digital voltage supplies and ground are provided to minimize noise and ensure a wide dynamic range. The analog circuit path contains only differential circuitry to keep noise to a minimum. The exception is the DAC sample-and-hold, which utilizes pseudo-differential circuitry.

The TLC32047C is characterized for operation from 0°C to 70°C, and the TLC32047I is characterized for operation from −40°C to 85°C.

Features

- **Advanced LinCMOS™ Silicon-Gate Process Technology**
- **14-Bit Dynamic Range ADC and DAC**
- **16-Bit Dynamic Range Input With Programmable Gain**
- **Synchronous or Asynchronous ADC and DAC Sampling Rates Up to 25,000 Samples Per Second**
- **Programmable Incremental ADC and DAC Conversion Timing Adjustments**
- **Typical Applications**
  - **Speech Encryption for Digital Transmission**
  - **Speech Recognition and Storage Systems**
  - **Speech Synthesis**
  - **Modems at 8-kHz, 9.6-kHz, and 16-kHz Sampling Rates**
  - **Industrial Process Control**
  - **Biomedical Instrumentation**
  - **Acoustical Signal Processing**
  - **Spectral Analysis**
  - **Instrumentation Recorders**
  - **Data Acquisition**
- **Switched-Capacitor Antialiasing Input Filter and Output-Reconstruction Filter**
- **Three Fundamental Modes of Operation: Dual-Word (Telephone Interface), Word, and Byte**
- **600-mil Wide N Package**
- **Digital Output in Twos Complement Format**

FUNCTION TABLE

DATA COMMUNICATIONS FORMAT	SYNCHRONOUS (CONTROL REGISTER BIT D5 = 1)	ASYNCHRONOUS (CONTROL REGISTER BIT D5 = 0)	FORCING CONDITION	DIRECT INTERFACE
16-bit format	Dual-word (telephone interface) mode	Dual-word (telephone interface) mode	Pin 13 = 0 to 5 V Pin 1 = 0 to 5 V	TMS32020, TMS320C25, TMS320C30
16-bit format	Word mode	Word mode	Pin 13 = V_{CC-} (–5 V nom) Pin 1 = V_{CC+} (+5 V nom)	TMS32020, TMS320C25, TMS320C30, indirect interface to TMS320C10.
8-bit format (2 bytes required)	Byte mode	Byte mode	Pin 13 = V_{CC-} (–5 V nom) Pin 1 = V_{CC-} (–5 V nom)	TMS320C17

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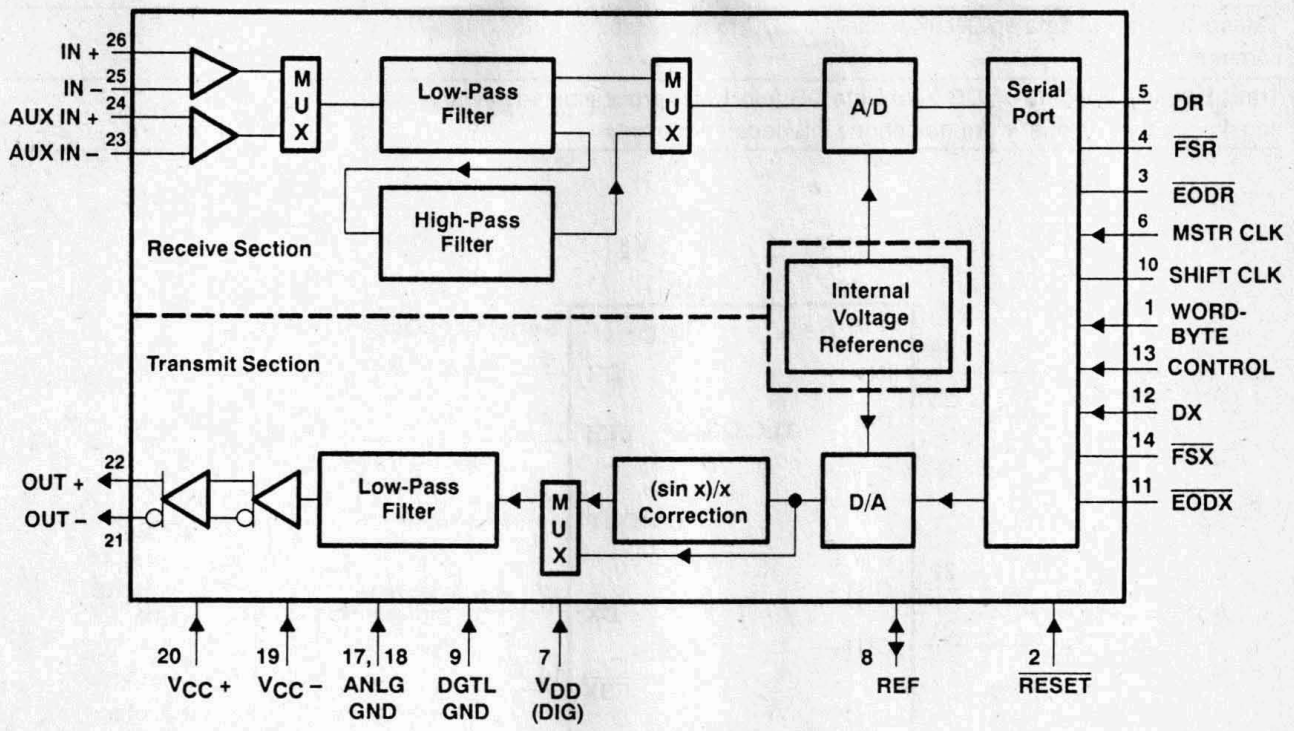
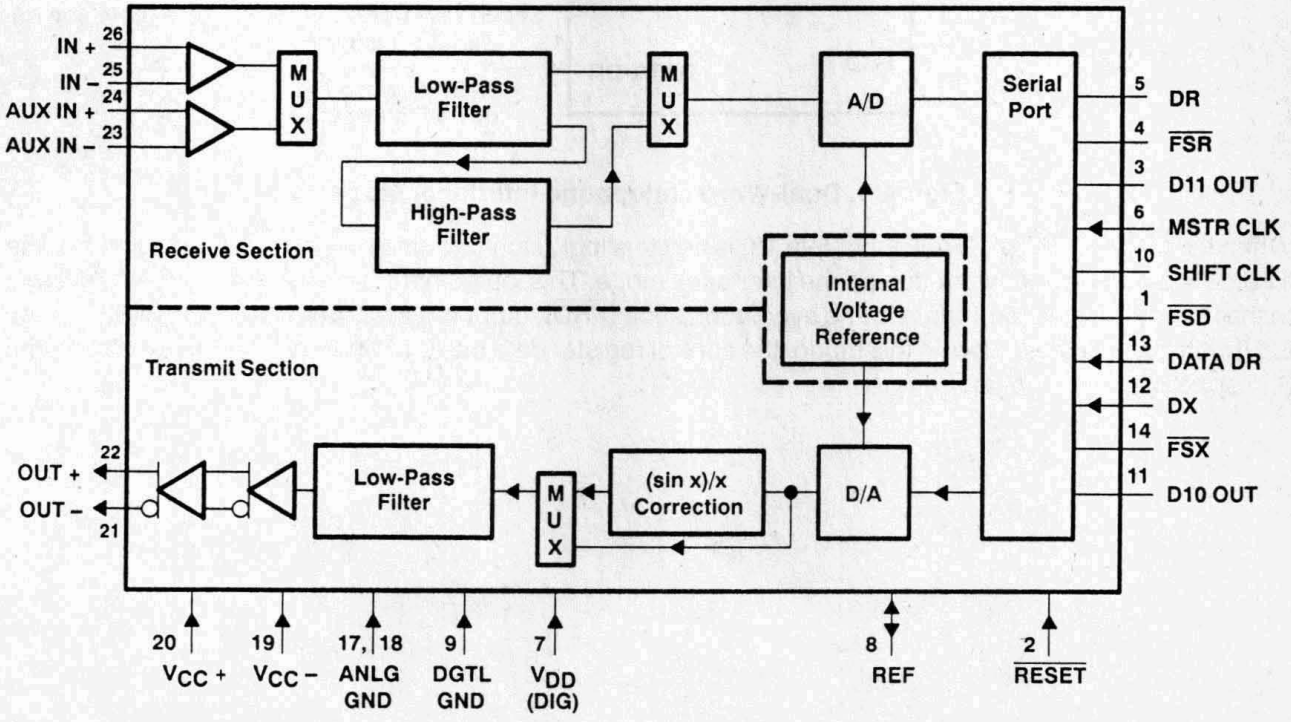
Functional Block Diagrams

WORD OR BYTE MODE



DUAL-WORD (TELEPHONE INTERFACE) MODE



FRAME SYNCHRONIZATION FUNCTIONS

TLC32047 Function	Frame Sync Output
Receiving serial data on DX from processor to internal DAC	$\overline{FSX}$ low
Transmitting serial data on DR from internal ADC to processor, primary communications	$\overline{FSR}$ low
Transmitting serial data on DR from Data DR (pin 13) to processor, secondary communications in dual-word (telephone interface) mode only	$\overline{FSD}$ (pin 1) low

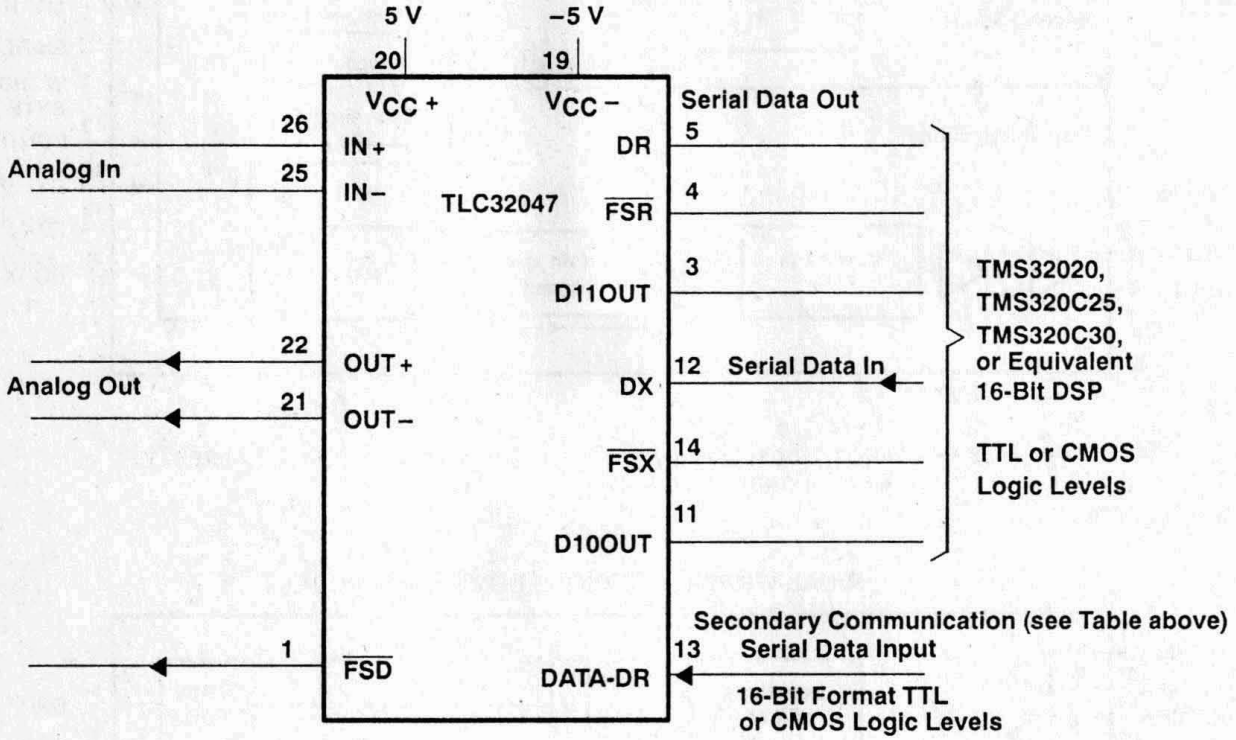


Figure 1. Dual-Word (Telephone Interface) Mode

When the DATA-DR/CONTROL input (pin 13) is tied to a logic signal source varying between 0 and 5 V, the TLC32047 is in the dual-word (telephone interface) mode. This logic signal is routed to the DR line for input to the DSP only when pin 1, data frame synchronization ($\overline{FSD}$), outputs a low level. The $\overline{FSD}$ pulse duration is 16 shift clock pulses. Also, in this mode, the control register data bits D10 and D11 appear on pins 11 and 3, respectively, as outputs.

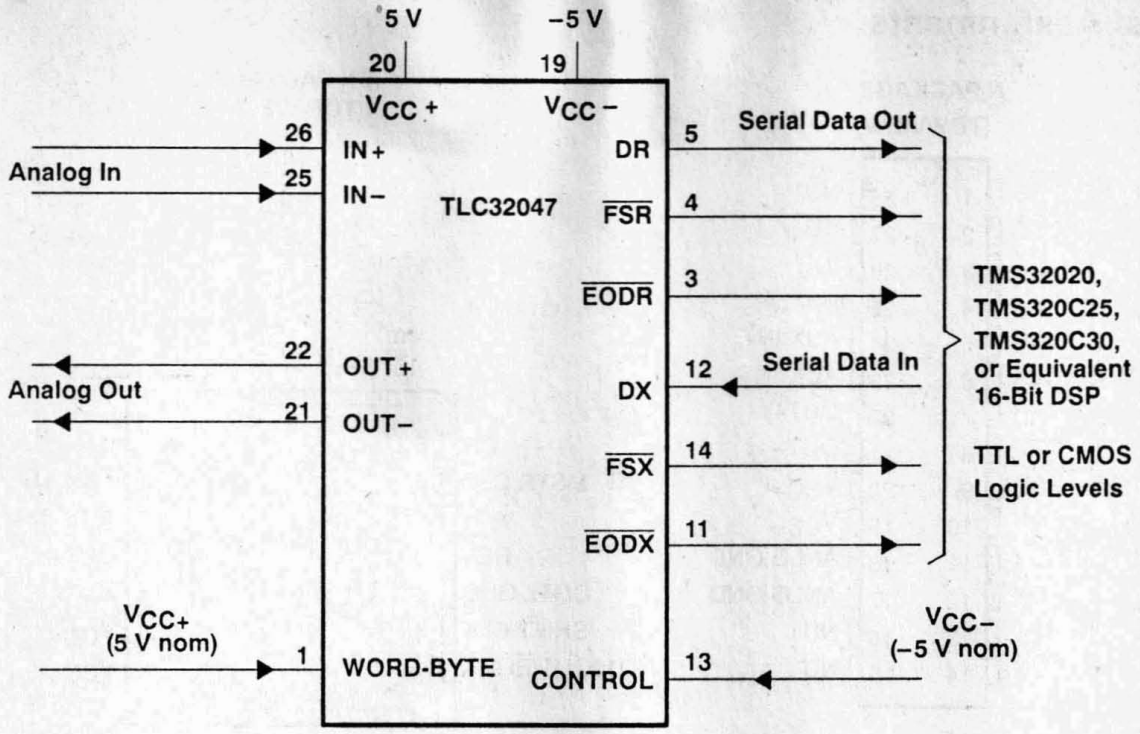


Figure 2. Word Mode

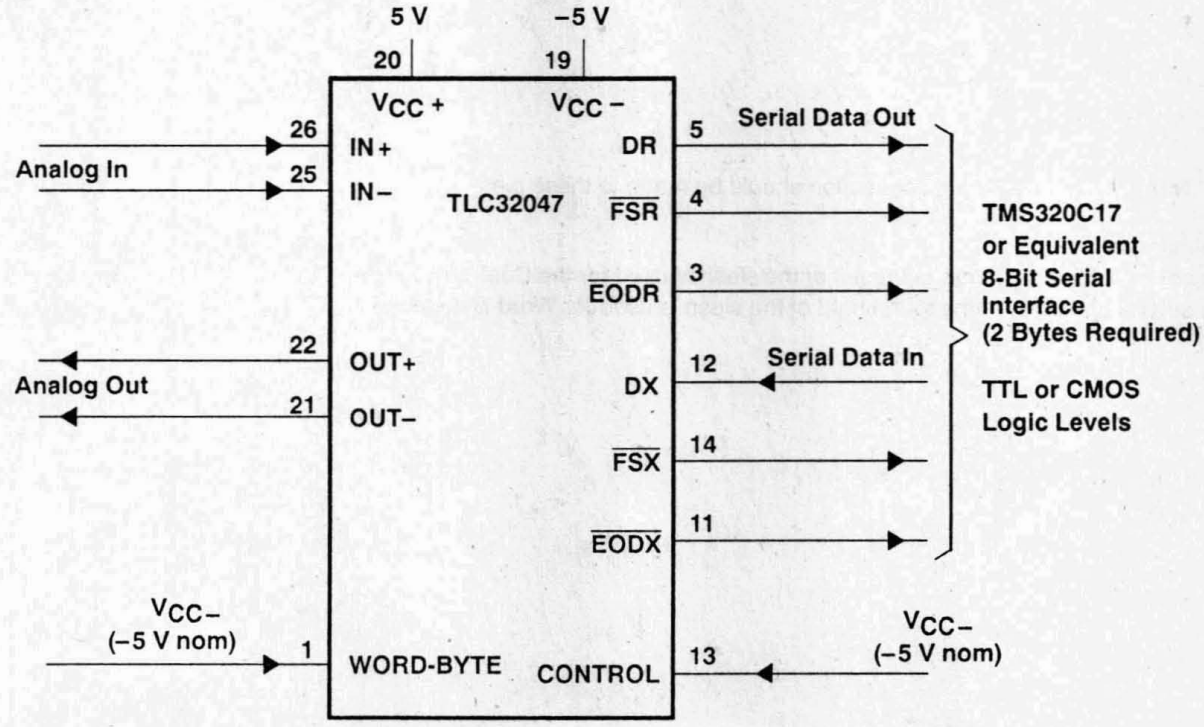
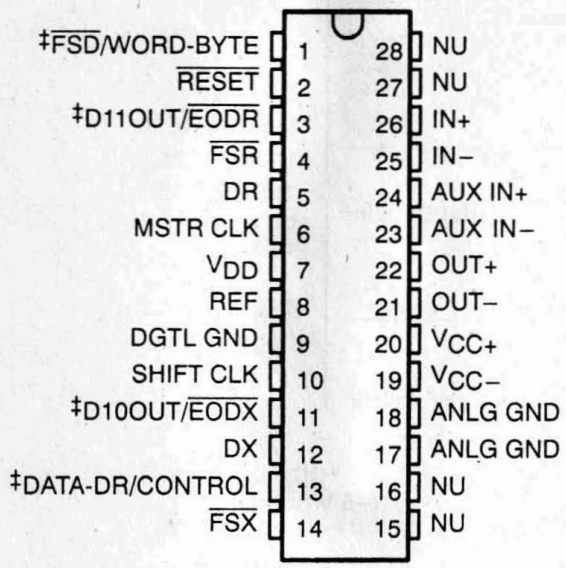


Figure 3. Byte Mode

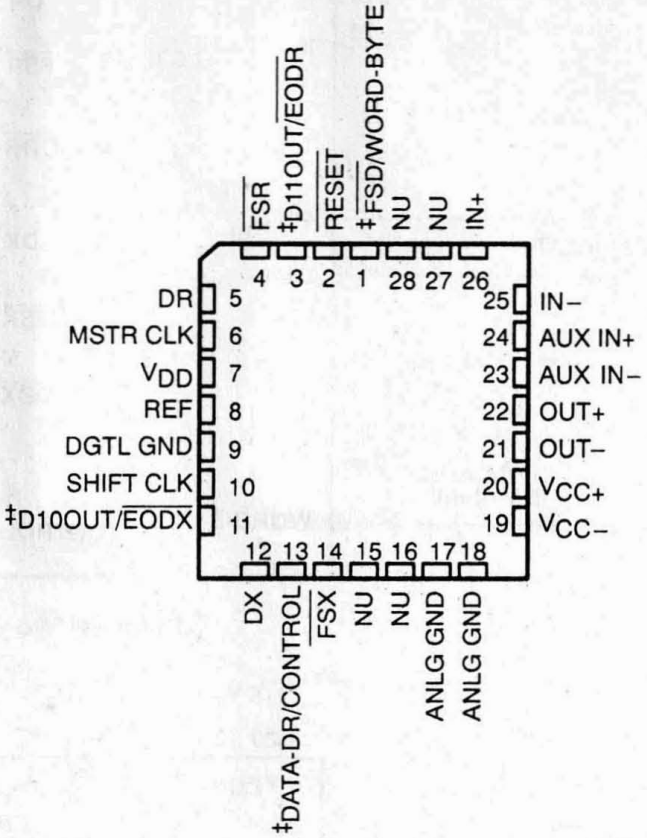
The word or byte mode is selected by first connecting the DATA-DR/CONTROL input (pin 13) to V_{CC-}. $\overline{FSD}$/WORD-BYTE (pin 1) becomes an input and can then be used to select either word or byte transmission formats. The end-of-data transmit ($\overline{EODX}$) and the end-of-data receive ($\overline{EODR}$) signals on pins 11 and 3, respectively, are used to signal the end of word or byte communication (see the Terminal Functions section).

Terminal Assignments

N PACKAGE† (TOP VIEW)



FN PACKAGE (TOP VIEW)



NU - Nonusable; no external connection should be made to these pins.

† 600-mil wide

‡ The portion of the pin name to the left of the slash is used for the Dual-Word (Telephone Interface) mode. The portion of the pin name to the right of the slash is used for Word-Byte mode.

Terminal Functions

PIN NAME	NO.	I/O	DESCRIPTION
ANLG GND	17,18		Analog ground return for all internal analog circuits. Not internally connected to DGTL GND.
AUX IN+	24	I	Noninverting auxiliary analog input stage. This input can be switched into the band-pass filter and ADC path via software control. If the appropriate bit in the control register is a 1, the auxiliary inputs replace the IN+ and IN− inputs. If the bit is a 0, the IN+ and IN− inputs are used (see the DX Serial Data Word Format).
AUX IN−	23	I	Inverting auxiliary analog input (see the above AUX IN+ pin description).
DATA-DR	13	I	The dual-word (telephone interface) mode, selected by applying an input logic level between 0 and 5 V to this input, allows this pin to function as a data input. The data is then framed by the $\overline{FSD}$ signal and transmitted as an output to the DR line during secondary communication. The functions $\overline{FSD}$ (pin 1), D11OUT (pin 3), and D10OUT (pin 11) are valid with this mode selection (see Table 1).
CONTROL			When this input is tied to V_{CC}−, the device is in the word or byte mode. The functions WORD-BYTE (pin 1), $\overline{EODR}$ (pin 3), and $\overline{EODX}$ (pin 11) are valid in this mode. Pin 1 is then used to select either the word or byte mode (see Function Table).
DR	5	O	This pin is used to transmit the ADC output bits from the AIC to the TMS320 serial port. This transmission of bits from the AIC to the TMS320 serial port is synchronized with the SHIFT CLK (pin 10) signal.
DX	12	I	This pin is used to receive the DAC input bits and timing and control information from the TMS320. This serial transmission from the TMS320 serial port is synchronized with the SHIFT CLK (pin 10) signal.
D10OUT	11	O	In the dual-word (telephone interface) mode, bit D10 of the Control Register is output to this pin. When the device is reset, bit D10 is initialized to 0 (see DX Serial Data Word Format). The output update is immediate upon changing bit D10.
$\overline{EODX}$			End of Data Transmit. During the word-mode timing, a low-going pulse occurs on this output immediately after the 16 bits of DAC and control or register information have been transmitted from the TMS320 serial port to the AIC.This signal can be used to interrupt a microprocessor upon completion of serial communications. Also, this signal can be used to strobe and enable external serial-to-parallel shift registers, latches, or external FIFO RAM and to facilitate parallel data bus communications between the DSP and the serial-to-parallel shift registers. During the byte-mode timing, this signal goes low after the first byte has been transmitted from the TMS320 serial port to the AIC and is kept low until the second byte has been transmitted. The TMS320C17 can use this low-going signal to differentiate first and second bytes.
D11OUT	3	O	In the dual-word (telephone interface) mode, bit D11 of the control register is output to this pin. When the device is reset, bit D11 is initialized to 0 (see DX Serial Data Word Format). The output update is immediate upon changing bit D11.
$\overline{EODR}$			End of Data Receive. During the word-mode timing, a low-going pulse occurs on this output immediately after the 16 bits of A/D information have been transmitted from the AIC to the TMS320 serial port. This signal can be used to interrupt a microprocessor upon completion of serial communications. Also, this signal can be used to strobe and enable external serial-to-parallel shift registers, latches, or external FIFO RAM, and to facilitate parallel data bus communications between the DSP and the serial-to-parallel shift registers. During the byte-mode timing, this signal goes low after the first byte has been transmitted from the AIC to the TMS320 serial port and is kept low until the second byte has been transmitted. The TMS320C17 can use this low-going signal to differentiate between first and second bytes.

Terminal Functions (continued)

PIN NAME	NO.	I/O	DESCRIPTION
DGTL GND	9		Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
$\overline{FSD}$	1	O	Frame Sync Data. The $\overline{FSD}$ output remains high during primary communication. In the dual-word (telephone interface) mode, the $\overline{FSD}$ output is identical to the $\overline{FSX}$ output during secondary communication.
WORD-BYTE		I	The WORD-BYTE pin allows differentiation between the word and byte data format (see DATA-DR/CONTROL (pin 13) and Table 1 for details).
$\overline{FSR}$	4	O	Frame Sync Receive. The $\overline{FSR}$ pin is held low during bit transmission. When the $\overline{FSR}$ pin goes low, the TMS320 serial port begins receiving bits from the AIC via the DR pin of the AIC. The most significant DR bit is present on the DR pin before $\overline{FSR}$ goes low. See Serial Port Sections and Internal Timing Configuration Diagrams.
$\overline{FSX}$	14	O	Frame Sync Transmit. When this pin goes low, the TMS320 serial port begins transmitting bits to the AIC via the DX pin of the AIC. The $\overline{FSX}$ pin is held low during bit transmission (see Serial Port Sections and Internal Timing Configuration Diagrams).
IN+	26	I	Noninverting input to analog input amplifier stage
IN−	25	I	Inverting input to analog input amplifier stage
MSTR CLK	6	I	The master clock signal is used to derive all the key logic signals of the AIC, such as the shift clock, the switched-capacitor filter clocks, and the A/D and D/A timing signals. The Internal Timing Configuration diagram shows how these key signals are derived. The frequencies of these signals are synchronous submultiples of the master clock frequency to eliminate unwanted aliasing when the sampled analog signals are transferred between the switched-capacitor filters and the ADC and DAC converters (see the Internal Timing Configuration).
OUT+	22	O	Noninverting output of analog output power amplifier. Drives transformer hybrids or high-impedance loads directly in a differential or a single-ended configuration.
OUT−	21	O	Inverting output of analog output power amplifier. Functionally identical with and complementary to OUT+.
REF	8	I/O	The internal voltage reference is brought out on this pin. An external voltage reference can be applied to this pin to override the internal voltage reference.
$\overline{RESET}$	2	I	A reset function is provided to initialize TA, TA', TB, RA, RA', RB (see Figure 2-1), and the control registers. This reset function initiates serial communications between the AIC and DSP. The reset function initializes all AIC registers, including the control register. After a negative-going pulse on the $\overline{RESET}$ pin, the AIC registers are initialized to provide a 16-kHz data conversion rate for a 10.368-MHz master clock input signal. The conversion rate adjust registers, TA' and RA', are reset to 1. The CONTROL register bits are reset as follows (see AIC DX Data Word Format section): D11 = 0, D10 = 0, D9 = 1, D7 = 1, D6 = 1, D5 = 1, D4 = 0, D3 = 0, D2 = 1 The shift clock (SCLK) is held high during $\overline{RESET}$. This initialization allows normal serial-port communication to occur between the AIC and the DSP.
SHIFT CLK	10	O	The shift clock signal is obtained by dividing the master clock signal frequency by four. This signal is used to clock the serial data transfers of the AIC.
V_{DD}	7		Digital supply voltage, 5 V ±5%
$V_{CC}+$	20		Positive analog supply voltage, 5 V ±5%
$V_{CC}-$	19		Negative analog supply voltage, −5 V ±5%

Detailed Description

Table 1. Mode-Selection Function Table

DATA-DR/ CONTROL (Pin 13)	$\overline{FSD}$/ WORD-BYTE (Pin 1)	CONTROL REGISTER BIT (D5)	OPERATING MODE	SERIAL CONFIGURATION	DESCRIPTION
Data in (0 to 5 V)	$\overline{FSD}$ out (0 to 5 V)	1	Dual-Word (Telephone Interface)	Synchronous, One 16-Bit Word	Pin functions DATA-DR (pin 13†), $\overline{FSD}$ (pin 1†), D11OUT (pin 3), and D10OUT (pin 11) are applicable in this configuration. $\overline{FSD}$ is asserted during secondary communication, but the $\overline{FSR}$ is not asserted. However, $\overline{FSD}$ remains high during primary communication.
Data in (0 to 5 V)	$\overline{FSD}$ out (0 to 5 V)	0	Dual-Word (Telephone Interface)	Asynchronous, One 16-Bit Word	Pin functions DATA-DR (pin 13†), $\overline{FSD}$ (pin 1†), D11OUT (pin 3), and D10OUT (pin 11) are applicable in this configuration. $\overline{FSD}$ is asserted during secondary communication, but the $\overline{FSR}$ is not asserted. However, $\overline{FSD}$ remains high during primary communication. If secondary communications occur while the A/D conversion is being transmitted from the DR (pin 5), $\overline{FSD}$ cannot go low, and data from the DATA-DR pin cannot go onto the DR pin (pin 5).
V_{CC-}	V_{CC+}	1	WORD	Synchronous, One 16-Bit Word	Pin functions CONTROL (pin 13†), WORD-BYTE (pin 1†), $\overline{EODR}$ (pin 3), and $\overline{EODX}$ (pin 11) are applicable in this configuration.
		0		Asynchronous, One 16-bit Word	Pin functions CONTROL (pin 13†), WORD-BYTE (pin 1†), $\overline{EODR}$ (pin 3), and $\overline{EODX}$ (pin 11) are applicable in this configuration.
	V_{CC-}	1	BYTE	Synchronous, Two 8-Bit Bytes	Pin functions CONTROL (pin 13†), WORD-BYTE (pin 1†), $\overline{EODR}$ (pin 3), and $\overline{EODX}$ (pin 11) are applicable in this configuration.
		0		Asynchronous, Two 8-Bit Bytes	Pin functions CONTROL (pin 13†), WORD-BYTE (pin 1†), $\overline{EODR}$ (pin 3), and $\overline{EODX}$ (pin 11) are applicable in this configuration.

† Pin 13 has an internal pulldown resistor to −5 V, and pin 1 has an internal pullup resistor to 5 V.

Internal Timing Configuration (see Figure 4)

All the internal timing of the AIC is derived from the high-frequency clock signal that drives the master clock input pin. The shift clock signal, which strobes the serial port data between the AIC and DSP, is derived by dividing the master clock input signal frequency by four.

The TX(A) counter and the TX(B) counter, which are driven by the master clock signal, determine the D/A conversion timing. Similarly, the RX(A) counter and the RX(B) counter determine the A/D conversion timing. In order for the low-pass switched-capacitor filter in the D/A path (see Functional Block Diagram) to meet its transfer function specifications, the frequency of its clock input must be 432 kHz. If the clock frequency is not 432 kHz, the filter transfer function frequencies are frequency-scaled by the ratios of the clock frequency to 432 kHz:

$$\text{Absolute Frequency (kHz)} = \frac{\text{Normalized Frequency} \times \text{SCF } f_{clock}\text{ (kHz)}}{432} \quad (1)$$

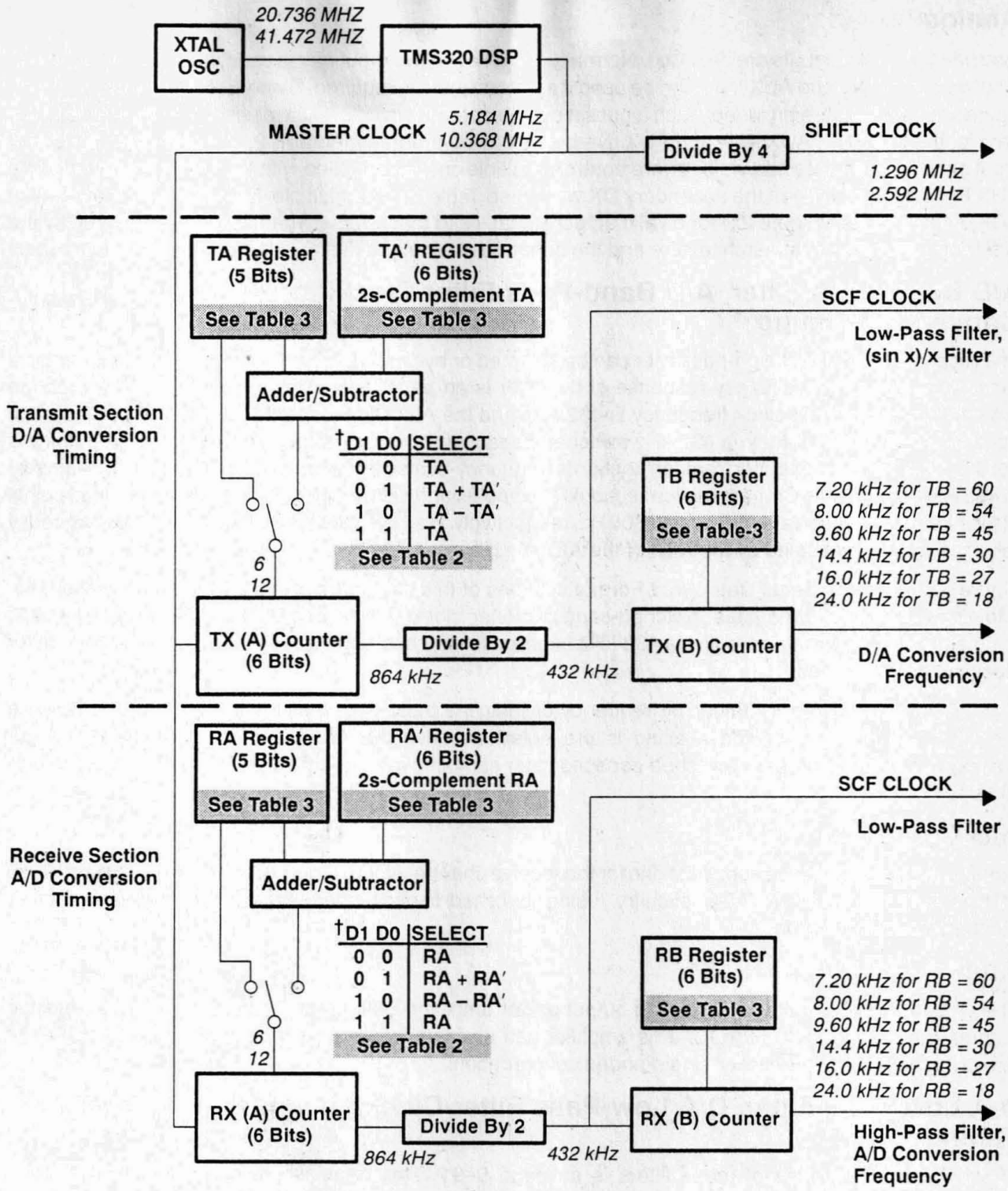
To obtain the specified filter response, the combination of master clock frequency and the TX(A) counter and the RX(A) counter values must yield a 432-kHz switched-capacitor clock signal. This 432-kHz clock signal can then be divided by the TX(B) counter to establish the D/A conversion timing.

The transfer function of the band-pass switched-capacitor filter in the A/D path (see Functional Block Diagram) is a composite of its high-pass and low-pass transfer functions. When the Shift Clock Frequency (SCF) is 432 kHz, the high-frequency roll-off of the low-pass section will meet the band-pass filter transfer function specification. Otherwise, the high-frequency roll-off will be frequency-scaled by the ratio of the high-pass section's SCF clock to 432 kHz (see Figure 5–5). The low-frequency roll-off of the high-pass section meets the band-pass filter transfer function specification when the A/D conversion rate is 24 kHz. If not, the low-frequency roll-off of the high-pass section is frequency-scaled by the ratio of the A/D conversion rate to 24 kHz.

The TX(A) counter and the TX(B) counter are reloaded each D/A conversion period, while the RX(A) counter and the RX(B) counter are reloaded every A/D conversion period. The TX(B) counter and the RX(B) counter are loaded with the values in the TB and RB registers, respectively. Via software control, the TX(A) counter can be loaded with the TA register, the TA register less the TA′ register, or the TA register plus the TA′ register. By selecting the TA register less the TA′ register option, the upcoming conversion timing occurs earlier by an amount of time that equals TA′ times the signal period of the master clock. If the TA register plus the TA′ register option is executed, the upcoming conversion timing occurs later by an amount of time that equals TA′ times the signal period of the master clock. Thus, the D/A conversion timing can be advanced or retarded. An identical ability to alter the A/D conversion timing is provided. However, the RX(A) counter can be programmed via software control with the RA register, the RA register less the RA′ register, or the RA register plus the RA′ register.

The ability to advance or retard conversion timing is particularly useful for modem applications. This feature allows controlled changes in the A/D and D/A conversion timing and can be used to enhance signal-to-noise performance, to perform frequency-tracking functions, and to generate nonstandard modem frequencies.

If the transmit and receive sections are configured to be synchronous, then the low-pass and band-pass switched-capacitor filter clocks are derived from the TX(A) counter. Also, both the D/A and A/D conversion timings are derived from the TX(A) counter and the TX(B) counter. When the transmit and receive sections are configured to be synchronous, the RX(A) counter, RX(B) counter, RA register, RA′ register, and RB registers are not used.



† These control bits are described in the DX Serial Data Word Format section.

NOTES: A. Tables 2 and 3 (pages 9–79 and 9–80) are primary and secondary communication protocols, respectively.

B. In synchronous operation, RA, RA', RB, RX(A), and RX(B) are not used. TA, TA', TB, TX(A), and TX(B) are used instead.

C. Items in italics refer only to frequencies and register contents, which are variable. A crystal oscillator driving 20.736 MHz into the TMS320-series DSP will provide a master clock frequency of 5.184 MHz. The TLC32047 will produce a shift clock frequency of 1.296 MHz. If the TX(A) register contents equal 6, the SCF clock frequency will then be 432 kHz, and the D/A conversion frequency will be 432 kHz ÷ T(B).

Figure 4. Asynchronous Internal Timing Configuration

Analog Input

Two pairs of analog inputs are provided. Normally, the IN+ and IN– input pair is used; however, the auxiliary input pair, AUX IN+ and AUX IN–, can be used if a second input is required. Since sufficient common-mode range and rejection are provided, each input set can be operated in differential or single-ended modes. The gain for the IN+, IN–, AUX IN+, and AUX IN– inputs can be programmed to 1, 2, or 4 (see Table 7). Either input circuit can be selected via software control. Multiplexing is controlled with the D4 bit (enable/disable AUX IN+ and AUX IN–) of the secondary DX word (see Table 3). The multiplexing requires a 2-ms wait at SCF = 432 kHz (see Figure 21) for a valid output signal. Note that a wide dynamic range is assured by the differential internal analog architecture and the separate analog and digital voltage supplies and grounds.

A/D Band-Pass Filter, A/D Band-Pass Filter Clocking, and A/D Conversion Timing

The receive-channel A/D high-pass filter can be selected or bypassed via software control (see Functional Block Diagram). The frequency response of this filter is on page 9–91. This response results when the switched-capacitor filter clock frequency is 432 kHz and the A/D sample rate is 24 kHz. Several possible options can be used to attain a 432-kHz switched-capacitor filter clock. When the filter clock frequency is not 432 kHz, the low-pass filter transfer function is frequency-scaled by the ratio of the actual clock frequency to 432 kHz (see Typical Characteristics section). The ripple bandwidth and 3-dB low-frequency roll-off points of the high-pass section are 450 Hz and 300 Hz, respectively. However, the high-pass section low-frequency roll-off is frequency-scaled by the ratio of the A/D sample rate to 24 kHz.

Figure 4 and the DX Serial Data Word Format sections of this data manual indicate the many options for attaining a 432-kHz band-pass switched-capacitor filter clock. These sections indicate that the RX(A) counter can be programmed to give a 432-kHz band-pass switched-capacitor filter clock for several master clock input frequencies.

The A/D conversion rate is attained by frequency-dividing the band-pass switched-capacitor filter clock with the RX(B) counter. Unwanted aliasing is prevented because the A/D conversion rate is an integer submultiple of the band-pass switched-capacitor filter sampling rate, and the two rates are synchronously locked.

A/D Converter

Fundamental performance specifications for the receive channel ADC circuitry are on pages 9–88 and 9–89 of this data manual. The ADC circuitry, using switched-capacitor techniques, provides an inherent sample-and-hold function.

Analog Output

The analog output circuitry is an analog output power amplifier. Both noninverting and inverting amplifier outputs are brought out of the IC. This amplifier can drive transformer hybrids or low-impedance loads directly in either a differential or single-ended configuration.

D/A Low-Pass Filter, D/A Low-Pass Filter Clocking, and D/A Conversion Timing

The frequency response of these filters is on page 9–91. This response results when the low-pass switched-capacitor filter clock frequency is 432 kHz (see Equation 1). Like the A/D filter, the transfer function of this filter is frequency-scaled when the clock frequency is not 432 kHz (see Typical Characteristics section). A continuous-time filter is provided on the output of the low-pass filter to eliminate the periodic sample data signal information, which occurs at multiples of the 432-kHz switched-capacitor clock feedthrough.

The D/A conversion rate is attained by frequency-dividing the 432-kHz switched-capacitor filter clock with the T(B) counter. Unwanted aliasing is prevented because the D/A conversion rate is an integer submultiple of the switched-capacitor low-pass filter sampling rate, and the two rates are synchronously locked.

D/A Converter

Fundamental performance specifications for the transmit channel DAC circuitry are on pages 9–89 and 9–90. The DAC has a sample-and-hold function that is realized with a switched-capacitor ladder.

Serial Port

The serial port has four possible configurations summarized in the Function Table on page 9–64. These configurations are briefly described below.

1. The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS320C17. The communications protocol is two 8-bit bytes.
2. The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS32020, TMS320C25, and TMS320C30. The communications protocol is one 16-bit word.
3. The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS320C17. The communications protocol is two 8-bit bytes.
4. The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS32020, TMS320C25, TMS320C30, or two SN74299 serial-to-parallel shift registers, which can interface in parallel to the TMS32010, TMS320C15, to any other digital signal processor, or to external FIFO circuitry. The communications protocol is one 16-bit word.

Synchronous Operation

When the transmit and receive sections are operated synchronously, the low-pass filter clock drives both low-pass and band-pass filters (see Functional Block Diagram). The A/D conversion timing is derived from and equal to the D/A conversion timing. When data bit D5 in the control register is a logic 1, transmit and receive sections are synchronous. The band-pass switched-capacitor filter and the A/D converter timing are derived from the TX(A) counter, the TX(B) counter, and the TA and TA' registers. In synchronous operation, both the A/D and the D/A channels operate from the same frequencies. The $\overline{\text{FSX}}$ and the $\overline{\text{FSR}}$ timing is identical during primary communication, but $\overline{\text{FSR}}$ is not asserted during secondary communication because there is no new A/D conversion result.

One 16-Bit Word (Dual-Word [Telephone Interface] or Word Mode)

The serial port interfaces directly with the serial ports of the TMS32020, TMS320C25, and the TMS320C30, and communicates in one 16-bit word. The operation sequence is as follows:

1. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought low by the TLC32047 AIC.
2. One 16-bit word is transmitted and one 16-bit word is received.
3. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought high.
4. The $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ pins emit low-going pulses one shift clock wide. $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ are valid in the word or byte mode only.

If the device is in the dual-word (telephone interface) mode, $\overline{\text{FSD}}$ goes low during the secondary communication period and enables the data word received at the DATA-DR/CONTROL input pin to be routed to the DR line. The secondary communication period occurs four shift clocks after completion of primary communications.

Two 8-Bit Bytes (Byte Mode)

The serial port interfaces directly with the serial port of the TMS320C17 and communicates in two 8-bit bytes. The operation sequence is as follows:

1. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought low.
2. One 8-bit word is transmitted and one 8-bit word is received.
3. The $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ pins are brought low.
4. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins emit positive frame-sync pulses that are four shift clock cycles wide.

5. One 8-bit byte is transmitted and one 8-bit byte is received.
6. The $\overline{FSX}$ and $\overline{FSR}$ pins are brought high.
7. The $\overline{EODX}$ and $\overline{EODR}$ pins are brought high.

Synchronous Operating Frequencies

The synchronous operating frequencies are determined by the following equations.

Switched capacitor filter (SCF) frequencies (see Figure 4):

$$\text{Low-pass SCF clock frequency} \quad (\text{D/A and A/D channels}) = \frac{\text{master clock frequency}}{\text{T(A)} \times 2}$$

$$\text{High-pass SCF clock frequency (A/D channel)} = \text{A/D conversion frequency}$$

$$\text{Conversion frequency (A/D and D/A channels)} = \frac{\text{Low pass SCF clock frequency}}{\text{T(B)}}$$

$$= \frac{\text{master clock frequency}}{\text{T(A)} \times 2 \times \text{T(B)}}$$

NOTE: T(A), T(B), R(A), and R(B) are the contents of the TA, TB, RA, and RB registers, respectively.

Asynchronous Operation

When the transmit and the receive sections are operated asynchronously, the low-pass and band-pass filter clocks are independently generated from the master clock. The D/A and the A/D conversion timing is also determined independently.

D/A timing is set by the counters and registers described in synchronous operation, but the RA and RB registers are substituted for the TA and TB registers to determine the A/D channel sample rate and the A/D path switched-capacitor filter frequencies. Asynchronous operation is selected by control register bit D5 being zero.

One 16-Bit Word (Word Mode)

The serial port interfaces directly with the serial ports of the TMS32020, TMS320C25, and TMS320C30 and communicates with 16-bit word formats. The operation sequence is as follows:

1. The $\overline{FSX}$ or $\overline{FSR}$ pins are brought low by the TLC32047 AIC.
2. One 16-bit word is transmitted or one 16-bit word is received.
3. The $\overline{FSX}$ or $\overline{FSR}$ pins are brought high.
4. The $\overline{EODX}$ or $\overline{EODR}$ pins emit low-going pulses one shift clock wide. $\overline{EODX}$ and $\overline{EODR}$ are valid in either the word or byte mode only.

Two 8-Bit Bytes (Byte Mode)

The serial port interfaces directly with the serial port of the TMS320C17 and communicates in two 8-bit bytes. The operating sequence is as follows:

1. The $\overline{FSX}$ or $\overline{FSR}$ pins are brought low by the TLC32047 AIC.
2. One byte is transmitted or received.
3. The $\overline{EODX}$ or $\overline{EODR}$ pins are brought low.
4. The $\overline{FSX}$ or $\overline{FSR}$ pins are brought high for four shift clock periods and then brought low.
5. The second byte is transmitted or received.
6. The $\overline{FSX}$ or $\overline{FSR}$ pins are brought high.
7. The $\overline{EODX}$ or $\overline{EODR}$ pins are brought high.

Asynchronous Operating Frequencies

The asynchronous operating frequencies are determined by the following equations.

Switched-capacitor filter frequencies (see Figure 4):

$$\text{Low-pass D/A SCF clock frequency} = \frac{\text{master clock frequency}}{\text{T(A)} \times 2}$$

$$\text{Low-pass A/D SCF clock frequency} = \frac{\text{master clock frequency}}{\text{R(A)} \times 2}$$

$$\text{High-pass SCF clock frequency (A/D channel)} = \text{A/D conversion frequency} \quad (2)$$

Conversion frequency:

$$\text{D/A conversion frequency} = \frac{\text{Low-pass D/A SCF clock frequency}}{\text{T(B)}}$$

$$\text{A/D conversion frequency} = \frac{\text{Low-pass A/D SCF clock frequency (for low pass receive filter)}}{\text{R(B)}} \quad (3)$$

NOTE: T(A), T(B), R(A), and R(B) are the contents of the TA, TB, RA, and RB registers, respectively.

Operation of TLC32047 With Internal Voltage Reference

The internal reference of the TLC32047 eliminates the need for an external voltage reference and provides overall circuit cost reduction. The internal reference eases the design task and provides complete control of the IC performance. The internal reference is brought out to pin 8. To keep the amount of noise on the reference signal to a minimum, an external capacitor can be connected between REF and ANLG GND.

Operation of TLC32047 With External Voltage Reference

The REF pin can be driven from an external reference circuit. This external circuit must be capable of supplying 250 μA and must be protected adequately from noise and crosstalk from the analog input.

Reset

A reset function is provided to initiate serial communications between the AIC and DSP and to allow fast, cost-effective testing during manufacturing. The reset function initializes all AIC registers, including the control register. After a negative-going pulse on the $\overline{\text{RESET}}$ pin, the AIC is initialized. This initialization allows normal serial port communications activity to occur between AIC and DSP (see AIC DX Data Word Format section). After RESET, TA=TB=RA=RB=18 (or 12 hexadecimal), TA′=RA′=01 (hexadecimal), the A/D high-pass filter is inserted, the loop-back function is deleted, AUX IN+ and AUX IN− pins are disabled, transmit and receive sections are in synchronous operation, programmable gain is set to 1, the on-board (sin x)/x correction filter is not selected, D10 OUT is set to 0, and D11 OUT is set to 0.

Loopback

This feature allows the circuit to be tested remotely. In loopback, the OUT+ and OUT− pins are internally connected to the IN+ and IN− pins. The DAC bits (D15 to D2), which are transmitted to the DX pin, can be compared with the ADC bits (D15 to D2), received from the DR pin. The bits on the DR pin equal the bits on the DX pin. However, there is some difference in these bits due to the ADC and DAC output offsets.

The loopback feature is implemented with digital signal processor control by transmitting a logic '1' for data bit D3 in the DX secondary communication to the control register (see Table 3).

Communications Word Sequence

In the Dual-Word (Telephone Interface) mode, there are two data words that are presented to the DSP or μP from the DR terminal. The first data word is the ADC conversion result occurring during the FSR time, and the second is the serial data applied to the DATA-DR pin during the FSD time. FSR is not asserted during secondary communications and FSD is not asserted during primary communications.

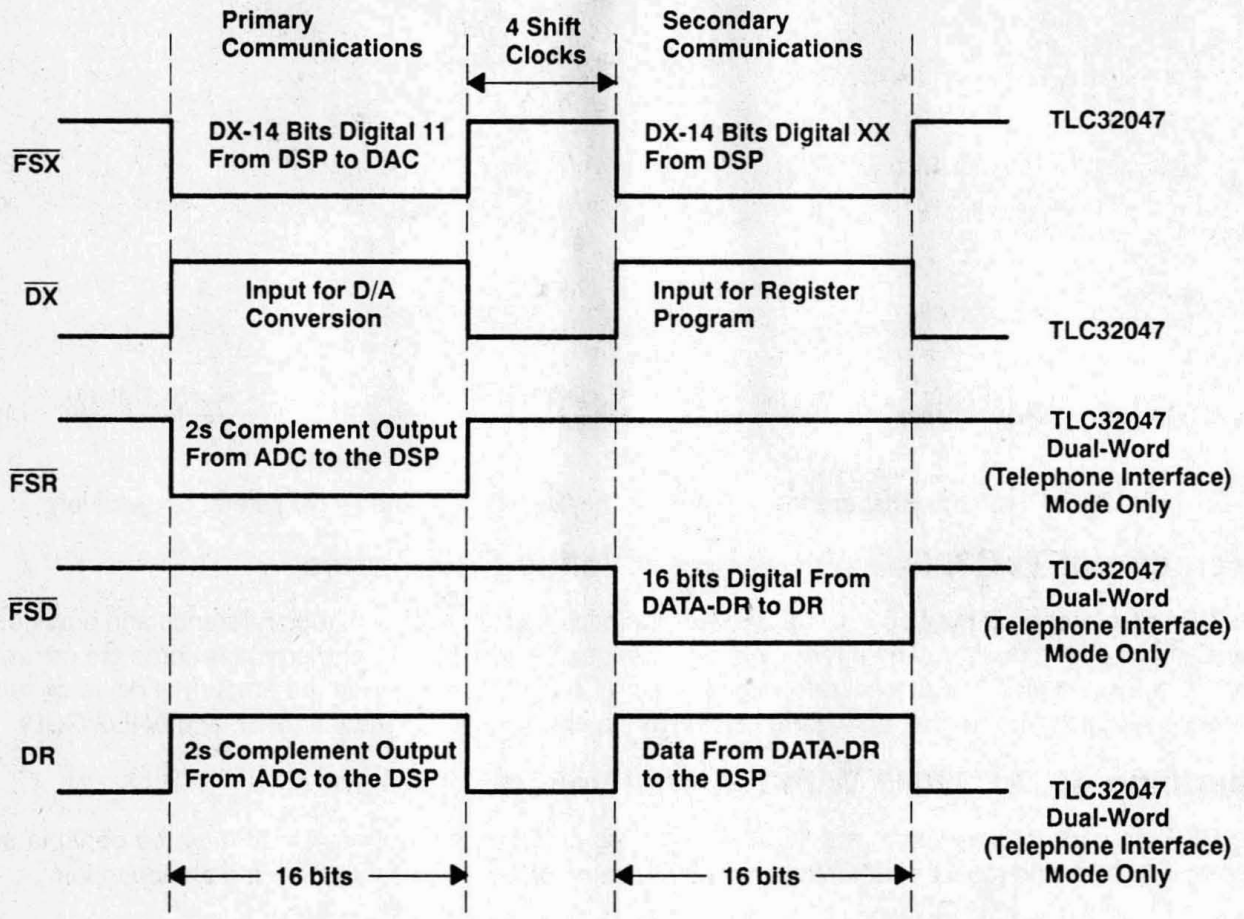


Figure 5. Primary and Secondary Communications Word Sequence

DR Word Bit Pattern

A/D MSB
1st bit sent ↓

A/D LSB ↓

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

The data word is the 14-bit conversion result of the receive channel to the processor in 2s complement format. With 16-bit processors, the data is 16 bits long with the two LSBs at zero. Using 8-bit processors, the data word is transmitted in the same order as one 16-bit word, but as two bytes with the two LSBs of the second byte set to zero.

Primary DX Word Bit Pattern

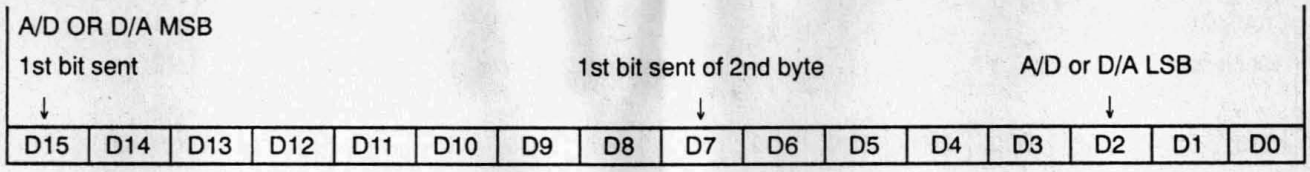


Table 2. Primary DX Serial Communication Protocol

FUNCTIONS	D1	D0
D15 (MSB)-D2 → DAC Register. TA → TX(A), RA → RX(A). See Figure 4. TB → TX(B), RB → RX(B). See Figure 4.	0	0
D15 (MSB)-D2 → DAC Register. TA+TA′ → TX(A), RA+RA′ → RX(A). See Figure 4. TB → TX(B), RB → RX(B). See Figure 4. The next D/A and A/D conversion period will be changed by the addition of TA′ and RA′ master clock cycles, in which TA′ and RA′ can be positive, negative, or zero. Refer to Table 4, AIC Responses to Improper Conditions.	0	1
D15 (MSB)-D2 → DAC Register. TA–TA′ → TX(A), RA–RA′ → RX(A). See Figure 4. TB → TX(B), RB → RX(B). See Figure 4. The next D/A and A/D conversion period will be changed by the subtraction of TA′ and RA′ master clock cycles, in which TA′ and RA′ can be positive, negative, or zero. Refer to Table 4, AIC Responses to Improper Conditions.	1	0
D15 (MSB)-D2 → DAC Register. TA → TX(A), RA → RX(A). See Figure 4. TB → TX(B), RB → RX(B). See Figure 4. After a delay of four shift cycles, a secondary transmission follows to program the AIC to operate in the desired configuration. In the telephone interface mode, data on DATA DR (pin 13) is routed to DR (Serial Data Output) during secondary transmission.	1	1

NOTE: Setting the two least significant bits to 1 in the normal transmission of DAC information (primary communications) to the AIC initiates secondary communications upon completion of the primary communications. When the primary communication is complete, $\overline{FSX}$ remains high for four SHIFT CLOCK cycles and then goes low and initiates the secondary communication. The timing specifications for the primary and secondary communications are identical. In this manner, the secondary communication, if initiated, is interleaved between successive primary communications. This interleaving prevents the secondary communication from interfering with the primary communications and DAC timing. This prevents the AIC from skipping a DAC output. It is important to note that $\overline{FSR}$ is not asserted during secondary communications activity. However, in the dual-word (telephone interface) mode, $\overline{FSD}$ is asserted during secondary communications but not during primary communications.

Secondary DX Word Bit Pattern

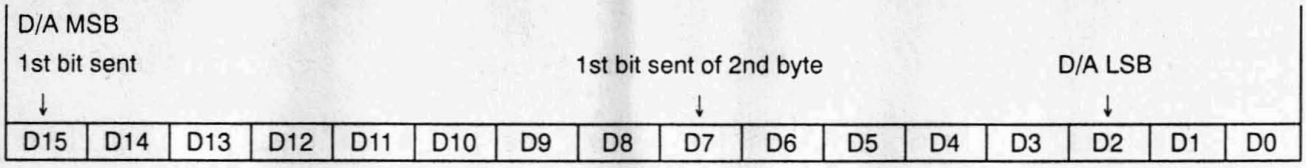


Table 3. Secondary DX Serial Communication Protocol

FUNCTIONS	D1	D0
D13 (MSB)-D9 → TA , 5 bits unsigned binary. See Figure 4. D6 (MSB)-D2 → RA, 5 bits unsigned binary. See Figure 4. D15, D14, D8, and D7 are unassigned.	0	0
D14 (sign bit)-D9 → TA′, 6 bits 2s complement. See Figure 4. D7 (sign bit)-D2 → RA′, 6 bits 2s complement. See Figure 4. D15 and D8 are unassigned.	0	1
D14 (MSB)-D9 → TB, 6 bits unsigned binary. See Figure 4. D7 (MSB)-D2 → RB, 6 bits unsigned binary. See Figure 4. D15 and D8 are unassigned.	1	0
D2 = 0/1 deletes/inserts the A/D high-pass filter. D3 = 0/1 deletes/inserts the loopback function. D4 = 0/1 disables/enables the AUX IN+ and AUX IN– pins. D5 = 0/1 asynchronous/synchronous transmit and receive sections. D6 = 0/1 gain control bits (see Table 7). D7 = 0/1 gain control bits (see Table 7). D9 = 0/1 delete/insert on-board second-order (sinx)/x correction filter D10 = 0/1 output to D10OUT (dual-word (telephone interface) mode) D11 = 0/1 output to D11OUT (dual-word (telephone interface) mode) D8, D12–D15 are unassigned.	1	1

Reset Function

A reset function is provided to initiate serial communications between the AIC and DSP. The reset function initializes all AIC registers, including the control register. After power has been applied to the AIC, a negative-going pulse on the $\overline{\text{RESET}}$ pin initializes the AIC registers to provide a 16-kHz A/D and D/A conversion rate for a 10.368-MHz master clock input signal. Also, the pass-bands of the A/D and D/A filters are 300 Hz to 7200 Hz and 0 Hz to 7200 Hz, respectively. Therefore, the filter bandwidths are 66% of those shown in the filter transfer function specification section. The AIC, excepting the CONTROL register, is initialized as follows (see AIC DX Data Word Format section):

REGISTER	TA	TA′	TB	RA	RA′	RB
INITIALIZED VALUE (HEX)	12	01	12	12	01	12

The CONTROL register bits are reset as follows (see Table 3):

D11 = 0, D10 = 0, D9 = 1, D7 = 1, D6 = 1, D5 = 1, D4 = 0, D3 = 0, D2 = 1

This initialization allows normal serial port communications to occur between the AIC and the DSP. If the transmit and receive sections are configured to operate synchronously and the user wishes to program different conversion rates, only the TA, TA′, and TB register need to be programmed. Both transmit and receive timing are synchronously derived from these registers (see the Terminal Functions and DX Serial Data Word Format sections).

Figure 6 shows a circuit that provides a reset on power-up when power is applied in the sequence given in the Power-Up Sequence section. The circuit depends on the power supplies reaching their recommended values a minimum of 800 ns before the capacitor charges to 0.8 V above DGTL GND.

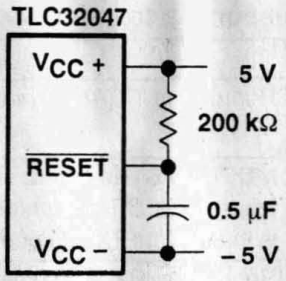


Figure 6. Reset on Power-Up Circuit

Power-Up Sequence

To ensure proper operation of the AIC and as a safeguard against latch-up, it is recommended that Schottky diodes with forward voltages less than or equal to 0.4 V be connected from V_{CC-} to ANLG GND and from V_{CC-} to DGTL GND. In the absence of such diodes, power is applied in the following sequence: ANLG GND and DGTL GND, V_{CC-}, then V_{CC+} and V_{DD}. Also, no input signal is applied until after power-up.

AIC Register Constraints

The following constraints are placed on the contents of the AIC registers:

1. TA register must be ≥ 4 in word mode (WORD/BYTE= High).
2. TA register must be ≥ 5 in byte mode (WORD/BYTE= Low).
3. TA′ register can be either positive, negative, or zero.
4. RA register must be ≥ 4 in word mode (WORD/BYTE = High).
5. RA register must be ≥ 5 in byte mode (WORD/BYTE = Low).
6. RA′ register can be either positive, negative, or zero.
7. (TA register ± TA′ register) must be > 1.
8. (RA register ± RA′ register) must be > 1.
9. TB register must be ≥ 15.
10. RB register must be ≥ 15.

AIC Responses to Improper Conditions

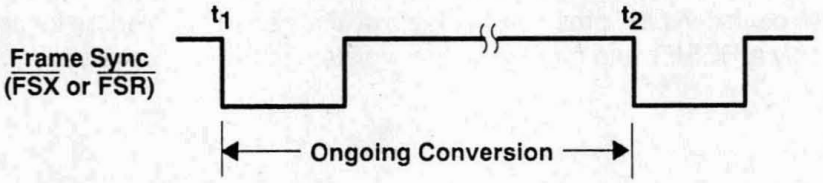
The AIC has provisions for responding to improper conditions. These improper conditions and the response of the AIC to these conditions are presented in Table 4. The general procedure for correcting any improper operation is to apply a RESET and reprogram the registers to the proper value.

Table 4. AIC Responses to Improper Conditions

IMPROPER CONDITION	AIC RESPONSE
TA register + TA′ register = 0 or 1 TA register – TA′ register = 0 or 1	Reprogram TX(A) counter with TA register value
TA register + TA′ register < 0	MODULO 64 arithmetic is used to ensure that a positive value is loaded into TX(A) counter, i.e., TA register + TA′ register + 40 HEX is loaded into TX(A) counter.
RA register + RA′ register = 0 or 1 RA register – RA′ register = 0 or 1	Reprogram RX(A) counter with RA register value
RA register + RA′ register = 0 or 1	MODULO 64 arithmetic is used to ensure that a positive value is loaded into RX(A) counter, i.e., RA register + RA′ register + 40 HEX is loaded into RX(A) counter.
TA register = 0 or 1 RA register = 0 or 1	AIC is shut down. Reprogram TA or RA registers after a reset.
TA register < 4 in word mode TA register < 5 in byte mode RA register < 4 in word mode RA register < 5 in byte mode	The AIC serial port no longer operates. Reprogram TA or RA registers after a reset.
TB register < 15	ADC no longer operates
RB register < 15	DAC no longer operates
AIC and DSP cannot communicate	Hold last DAC output

Operation With Conversion Times Too Close Together

If the difference between two successive D/A conversion frame syncs is less than 1/25 kHz, the AIC operates improperly. In this situation, the second D/A conversion frame sync occurs too quickly, and there is not enough time for the ongoing conversion to be completed. This situation can occur if the A and B registers are improperly programmed or if the A + A′ register result is too small. When incrementally adjusting the conversion period via the A + A′ register options, the designer should not violate this requirement. See Figure 7.



$t_2 - t_1 \leq 1/25$ kHz

Figure 7. Conversion Times Too Close Together

More Than One Receive Frame Sync Occurring Between Two Transmit Frame Syncs – Asynchronous Operation

When incrementally adjusting the conversion period via the A + A′ or A – A′ register options, a specific protocol is followed. The command to use the incremental conversion period adjust option is sent to the AIC during an $\overline{\text{FSX}}$ frame sync. The ongoing conversion period is then adjusted; however, either receive conversion period A or conversion period B may be adjusted. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. If there is sufficient time between t_1 and t_2, the receive conversion period adjustment is performed during receive conversion period A. Otherwise, the adjustment is performed during receive conversion period B.

The adjustment command only adjusts one transmit conversion period and one receive conversion period. To adjust another pair of transmit and receive conversion periods, another command must be issued during a subsequent $\overline{FSX}$ frame (see Figure 8).

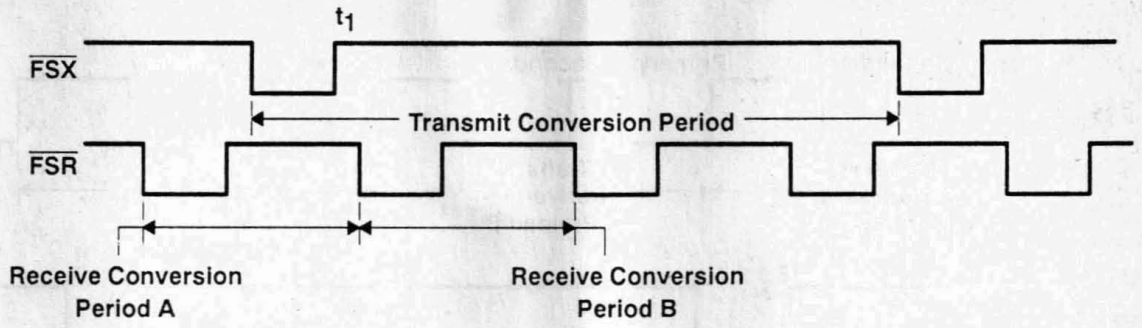


Figure 8. More Than One Receive Frame Sync Between Two Transmit Frame Syncs

More Than One Transmit Frame Sync Occurring Between Two Receive Frame Syncs – Asynchronous Operation

When incrementally adjusting the conversion period via the A + A′ or A – A′ register options, a specific protocol must be followed. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. The command to use the incremental conversion period adjust options is sent to the AIC during an $\overline{FSX}$ frame sync. The ongoing transmit conversion period is then adjusted. However, three possibilities exist for the receive conversion period adjustment as shown in Figure 9. When the adjustment command is issued during transmit conversion period A, receive conversion period A is adjusted if there is sufficient time between t1 and t2. If there is not sufficient time between t1 and t2, receive conversion period B is adjusted. The third option is that the receive portion of an adjustment command can be ignored if the adjustment command is sent during a receive conversion period, which is adjusted due to a prior adjustment command. For example, if adjustment commands are issued during transmit conversion periods A, B, and C, the first two commands may cause receive conversion periods A and B to be adjusted, while the third receive adjustment command is ignored. The third adjustment command is ignored since it was issued during receive conversion period B, which already is adjusted via the transmit conversion period B adjustment command.

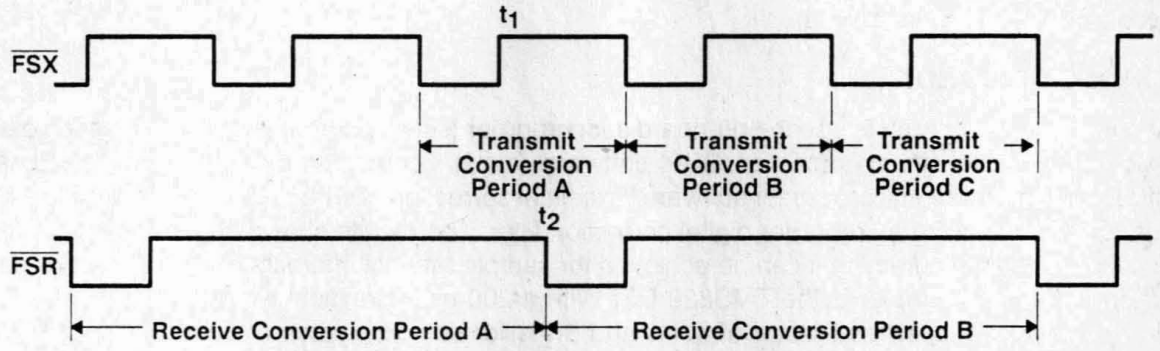


Figure 9. More Than One Transmit Frame Sync Between Two Receive Frame Syncs

More than One Set of Primary and Secondary DX Serial Communications Occurring Between Two Receive Frame Syncs (See DX Serial Data Word Format section) – Asynchronous Operation

The TA, TA′, TB, and control register information that is transmitted in the secondary communication is accepted and applied during the ongoing transmit conversion period. If there is sufficient time between t_1 and t_2, the TA, RA′, and RB register information, sent during transmit conversion period A, is applied to

receive conversion period A. Otherwise, this information is applied during receive conversion period B. If RA, RA′, and RB register information has been received and is being applied during an ongoing conversion period, any subsequent RA, RA′, or RB information received during this receive conversion period is disregarded. See Figure 10.

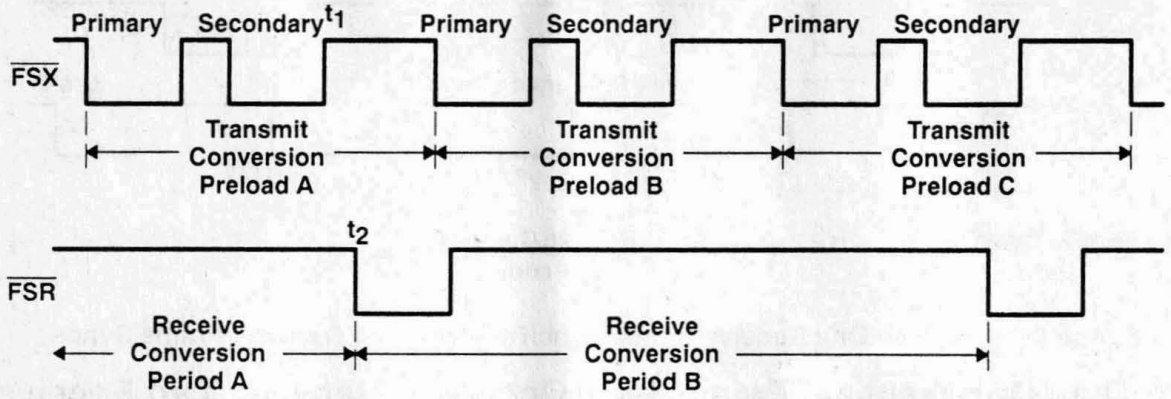


Figure 10. More Than One Set of Primary and Secondary DX Serial Communications Between Two Receive Frame Syncs

System Frequency Response Correction

The (sin x)/x correction for the DAC zero-order sample-and-hold output can be provided by an on-board second-order (sin x)/x correction filter (see Functional Block Diagram). This (sin x)/x correction filter can be inserted into or omitted from the signal path by digital-signal-processor control (data bit D9 in the DX secondary communications). When inserted, the (sin x)/x correction filter precedes the switched-capacitor low-pass filter. When the TB register (see Figure 4) equals 15, the correction results of Figures 26, 27, and 28 can be obtained.

The (sin x)/x correction [see section (sin x)/x] can also be accomplished by disabling the on-board second-order correction filter and performing the (sin x)/x correction in digital signal processor software. The system frequency response can be corrected via DSP software to ± 0.1 dB accuracy to a band edge of 3000 Hz for all sampling rates. This correction is accomplished with a first-order digital correction filter, that requires seven TMS320 instruction cycles. With a 200-ns instruction cycle, seven instructions represent an overhead factor of 1.1% and 1.3% for sampling rates of 8 and 9.6 kHz, respectively (see the (sin x)/x Correction Section for more details).

(sin x)/x Correction

If the designer does not wish to use the on-board second-order (sin x)/x correction filter, correction can be accomplished in digital signal processor (DSP) software. (sin x)/x correction can be accomplished easily and efficiently in digital signal processor software. Excellent correction accuracy can be achieved to a band edge of 3000 Hz by using a first-order digital correction filter. The results shown below are typical of the numerical correction accuracy that can be achieved for sample rates of interest. The filter requires seven instruction cycles per sample on the TMS320 DS. With a 200-ns instruction cycle, nine instructions per sample represents an overhead factor of 1.4% and 1.7% for sampling rates of 8000 Hz and 9600 Hz, respectively. This correction adds a slight amount of group delay at the upper edge of the 300-Hz to 3000-Hz band.

(sin x)/x Roll-Off for a Zero-Order Hold Function

The (sin x)/x roll-off error for the AIC DAC zero-order hold function at a band-edge frequency of 3000 Hz for the various sampling rates is shown in Table 8 (see Figure 28).

Table 5. (sin x)/x Roll-Off Error

f_S (Hz)	Error = 20 log $\frac{\sin \pi f/f_S}{\pi f/f_S}$ f = 3000 Hz (dB)
7200	−2.64
8000	−2.11
9600	−1.44
14400	−0.63
16000	−0.50
19200	−0.35
25000	−0.21

The actual AIC (sin x)/x roll-off is slightly less than the figures above because the AIC has less than 100% duty cycle hold interval.

Correction Filter

To externally compensate for the (sin x)/x roll-off of the AIC, a first-order correction filter can be implemented as shown in Figure 11.

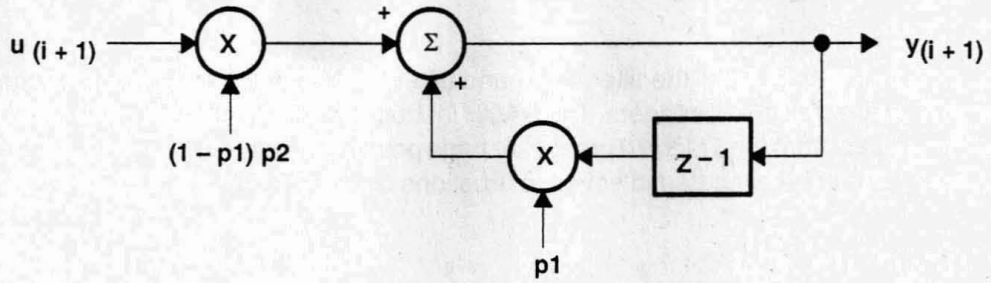


Figure 11. First-Order Correction Filter

The difference equation for this correction filter is:

$$y_{(i+1)} = p2 \cdot (1 - p1) \cdot u_{(i+1)} + p1 \cdot y_{(i)} \quad (4)$$

where the constant p1 determines the pole locations.

The resulting squared magnitude transfer function is:

$$\left| H\,(f) \right|^2 = \frac{(p2)^2 \cdot (1-p1)^2}{1-2 \cdot p1 \cdot \cos\,(2\pi\, f/f_S) + (p1)^2} \quad (5)$$

Correction Results

Table 6 shows the optimum p values and the corresponding correction results for 8000-Hz and 9600-Hz sampling rates (see Figures 26, 27, and 28).

Table 6. (sin x)/x Correction Table for f_S = 8000 Hz and f_S = 9600 Hz

f (Hz)	ROLL-OFF ERROR (dB) f_S = 8000 Hz p1 = −0.14813 p2 = 0.9888	ROLL-OFF ERROR (dB) f_S = 9600 Hz p1 = −0.1307 p2 = 0.9951
300	−0.099	−0.043
600	−0.089	−0.043
900	−0.054	0
1200	−0.002	0
1500	0.041	0
1800	0.079	0.043
2100	0.100	0.043
2400	0.091	0.043
2700	−0.043	0
3000	−0.102	−0.043

TMS320 Software Requirements

The digital correction filter equation can be written in state variable form as follows:

$$y_{(i+1)} = y_{(i)} \cdot k1 + u_{(i+1)} \cdot k2$$

where k1 = p1, k2 = (1 − p1)p2, y(i) is the filter state, and u(i+1) is the next I/O sample. The coefficients k1 and k2 must be represented as 16-bit integers. The SACH instruction (with the proper shift) yields the correct result. With the assumption that the TMS320 processor page pointer and memory configuration are properly initialized, the equation can be executed in seven instructions or seven cycles with the following program:

```
ZAC
LT K2
MPY U
LTA K1
MPY Y
APAC
SACH (dma), (shift)
```

Specifications

Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)

Supply voltage range, V_{CC+} (see Note 1) ..... −0.3 V to 15 V
Supply voltage range, V_{CC-} (see Note 1) ..... −0.3 V to 15 V
Supply voltage range, V_{DD} ..... −0.3 V to 15 V
Output voltage range, V_O ..... −0.3 V to 15 V
Input voltage range, V_I ..... −0.3 V to 15 V
Digital ground voltage range ..... −0.3 V to 15 V
Operating free-air temperature range: TLC32047C ..... 0°C to 70°C
TLC32047I ..... −40°C to 85°C
Storage temperature range ..... −40°C to 125°C
Case temperature for 10 seconds: FN package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package ... 260°C

NOTE 1: Voltage values for maximum ratings are with respect to V_{CC-}.

Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} (see Note 2)		4.75	5	5.25	V
Supply voltage, V_{CC-} (see Note 2)		−4.75	−5	−5.25	V
Digital supply voltage, V_{DD} (see Note 2)		4.75	5	5.25	V
Digital ground voltage with respect to ANLG GND, DGTL GND			0		V
Reference input voltage, $V_{ref(ext)}$ (see Note 2)		2		4	V
High-level input voltage, V_{IH}		2		V_{DD}	V
Low-level input voltage, V_{IL} (see Note 3)		0		0.8	V
Load resistance at OUT+ and/or OUT−, R_L		300			Ω
Load capacitance at OUT+ and/or OUT−, C_L				100	pF
MSTR CLK frequency (see Note 4)			5	10.368	MHz
Analog input amplifier common mode input voltage (see Note 5)				±1.5	V
A/D or D/A conversion rate				25	kHz
Operating free-air temperature range, T_A	TLC32047C	0		70	°C
	TLC32047I	−40		85	

NOTES: 2. Voltages at analog inputs and outputs, REF, V_{CC+}, and V_{CC-} are with respect to the ANLG GND terminal. Voltages at digital inputs and outputs and V_{DD} are with respect to the DGTL GND terminal.

3. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data manual for logic voltage levels only.
4. The band-pass switched-capacitor filter (SCF) specifications apply only when the low-pass section SCF clock is 432 kHz and the high-pass section SCF clock is 24 kHz. If the low-pass SCF clock is shifted from 432 kHz, the low-pass roll-off frequency shifts by the ratio of the low-pass SCF clock to 432 kHz. If the high-pass SCF clock is shifted from 24 kHz, the high-pass roll-off frequency shifts by the ratio of the high-pass SCF clock to 24 kHz. Similarly, the low-pass switched-capacitor filter (SCF) specifications apply only when the SCF clock is 432 kHz. If the SCF clock is shifted from 432 kHz, the low-pass roll-off frequency shifts by the ratio of the SCF clock to 432 kHz.
5. This range applies when (IN+ – IN−) or (AUX IN+ – AUX IN−) equals ± 6 V.

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (Unless Otherwise Noted)

total device, MSTR CLK frequency = 5.184 MHz, outputs not loaded

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 4.75 V, I_{OH} = −300 μA	2.4			V
V_{OL}	Low-level output voltage		V_{DD} = 4.75 V, I_{OL} = 2 mA			0.4	V
I_{CC+}	Supply current from V_{CC+}	TLC32047C				35	mA
		TLC32047I				40	
I_{CC-}	Supply current from V_{CC-}	TLC32047C				−35	mA
		TLC32047I				−40	
I_{DD}	Supply current from V_{DD}					7	mA
V_{ref}	Internal reference output voltage			3		3.3	V
α_{Vref}	Temperature coefficient of internal reference voltage				250		ppm/°C
r_o	Output resistance at REF				100		kΩ

power supply rejection and crosstalk attenuation

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{CC+} or V_{CC-} supply voltage rejection ratio, receive channel	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at DR (ADC output)		30		dB
	f = 30 kHz to 50 kHz			45		
V_{CC+} or V_{CC-} supply voltage rejection ratio, transmit channel (single-ended)	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at OUT+		30		dB
	f = 30 kHz to 50 kHz			45		
Crosstalk attenuation, transmit-to-receive (single-ended)				80		dB

serial port

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −300 μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4	V
I_I	Input current				±10	μA
I_I	Input current, DATA-DR/CONTROL				±100	μA
C_i	Input capacitance			15		pF
C_o	Output capacitance			15		pF

receive amplifier input

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	A/D converter offset error (filters in)			10	70	mV
CMRR	Common-mode rejection ratio at IN+, IN−, or AUX IN+, AUX IN−	See Note 6		55		dB
r_I	Input resistance at IN+, IN− or AUX IN+, AUX IN−, REF			100		kΩ

† All typical values are at T_A = 25°C.

NOTE 6: The test condition is a 0-dBm, 1-kHz input signal with a 24-kHz conversion rate.

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (Unless Otherwise Noted) (Continued)

transmit filter output

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OO}	Output offset voltage at OUT+ or OUT− (single-ended relative to ANLG GND)			15	80	mV
V_{OM}	Maximum peak output voltage swing across R_L at OUT+ or OUT− (single-ended)	$R_L \geq 300\ \Omega$, Offset voltage = 0	±3			V
V_{OM}	Maximum peak output voltage swing between OUT+ and OUT− (differential output)	$R_L \geq 600\ \Omega$	±6			V

† All typical values are at T_A = 25°C.

receive and transmit channel system distortion, SCF clock frequency = 432 kHz (see Note 7)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Attenuation of second harmonic of A/D input signal	single-ended	V_{in} = −0.1 dB to −24 dB		70		dB
	differential		62	70		
Attenuation of third and higher harmonics of A/D input signal	single-ended			65		dB
	differential		57	65		
Attenuation of second harmonic of D/A input signal	single-ended	V_{in} = −0 dB to −24 dB		70		dB
	differential		62	70		
Attenuation of third and higher harmonics of D/A input signal	single-ended			65		dB
	differential		57	65		

† All typical values are at T_A = 25°C.

receive channel signal-to-distortion ratio (see Note 7)

PARAMETER	TEST CONDITIONS	A_V = 1 V/V‡		A_V = 2 V/V‡		A_V = 4 V/V‡		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
A/D channel signal-to-distortion ratio	V_{in} = −6 dB to −0.1 dB	56		§		§		dB
	V_{in} = −12 dB to −6 dB	56		56		§		
	V_{in} = −18 dB to −12 dB	53		56		56		
	V_{in} = −24 dB to −18 dB	47		53		56		
	V_{in} = −30 dB to −24 dB	41		47		53		
	V_{in} = −36 dB to −30 dB	35		41		47		
	V_{in} = −42 dB to −36 dB	29		35		41		
	V_{in} = −48 dB to −42 dB	23		29		35		
	V_{in} = −54 dB to −48 dB	17		23		29		

‡ A_V is the programmable gain of the input amplifier.

§ Measurements under these conditions are unreliable due to overrange and signal clipping.

NOTE 7: The test condition is a 1-kHz input signal with a 24-kHz conversion rate. The load impedance for the DAC is 600 Ω. Input and output voltages are referred to V_{ref}.

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (Unless Otherwise Noted) (Continued)

transmit channel signal-to-distortion ratio (see Note 7)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
D/A channel signal-to-distortion ratio	V_{in} = −6 dB to −0.1 dB	58		dB
	V_{in} = −12 dB to −6 dB	58		
	V_{in} = −18 dB to −12 dB	56		
	V_{in} = −24 dB to −18 dB	50		
	V_{in} = −30 dB to −24 dB	44		
	V_{in} = −36 dB to −30 dB	38		
	V_{in} = −42 dB to −36 dB	32		
	V_{in} = −48 dB to −42 dB	26		
	V_{in} = −54 dB to −48 dB	20		

NOTE 7: The test condition is a 1-kHz input signal with a 24-kHz conversion rate. The load impedance for the DAC is 600 Ω. Input and output voltages are referred to V_{ref}.

receive and transmit gain and dynamic range (see Note 8)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit gain tracking error	V_{out} = −48 dB to 0 dB signal range		±0.05	±0.25	dB
Receive gain tracking error	V_{in} = −48 dB to 0 dB signal range		±0.05	±0.25	dB

NOTE 8: Gain tracking is relative to the absolute gain at 1 kHz and 0 dB (0 dB relative to V_{ref}).

receive channel band-pass filter transfer function, SCF f_{clock} = 432 kHz, input (IN+ – IN–) is a ±3-V sine wave‡ (see Note 9)

PARAMETER	TEST CONDITION	FREQUENCY	ADJUSTMENT	MIN	TYP†	MAX	UNIT
Filter gain	Input signal reference is 0 dB	f ≤ 150 Hz	K1 × 0 dB	−33	−29	−25	dB
		f = 300 Hz	K1 × −0.26 dB	−4	−2	−1	
		f = 450 Hz to 9300 Hz	K1 × 0 dB	−0.25	0	0.25	
		f = 9300 Hz to 9900 Hz	K1 × 0 dB	−0.3	0	0.3	
		f = 9900 Hz to 10950 Hz	K1 × 0 dB	−0.5	0	0.5	
		f = 11.4 kHz	K1 × 2.3 dB	−5	−2	−0.5	
		f = 12 kHz	K1 × 2.7 dB		−16	−14	
		f ≥ 13.2 kHz	K1 × 3.2 dB			−40	
		f ≥ 15 kHz	K1 × 0 dB			−60	

† All typical values are at T_A = 25°C.

‡ The MIN, TYP, and MAX specifications are given for a 432-kHz SCF clock frequency. A slight error in the 432-kHz SCF may result from inaccuracies in the MSTR CLK frequency, resulting from crystal frequency tolerances. If this frequency error is less than 0.25%, the ADJUSTMENT ADDEND should be added to the MIN, TYP, and MAX specifications, where K1 = 100 • [(SCF frequency – 432 kHz)/432 kHz]. For errors greater than 0.25%, see Note 9.

NOTE 9: The filter gain outside of the pass band is measured with respect to the gain at 1 kHz. The filter gain within the pass band is measured with respect to the average gain within the pass band. The pass bands are 450 Hz to 10.95 kHz and 0 to 10.95 kHz for the band-pass and low-pass filters, respectively. For switched-capacitor filter clocks at frequencies other than 432 kHz, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 432 kHz.

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (Unless Otherwise Noted) (Continued)

receive and transmit channel low-pass filter transfer function, SCF f_{clock} = 432 kHz (see Note 9)

PARAMETER	TEST CONDITION	FREQUENCY RANGE	ADJUSTMENT ADDEND‡	MIN	TYP†	MAX	UNIT
Filter gain	Input signal reference is 0 dB	f = 0 Hz to 9300 Hz	K1 × 0 dB	−0.25	0	0.25	dB
		f = 9300 Hz to 9900 Hz	K1 × 0 dB	−0.3	0	0.3	
		f = 9900 Hz to 10950 Hz	K1 × 0 dB	−0.5	0	0.5	
		f = 11.4 kHz	K1 × 2.3 dB	−5	−2	−0.5	
		f = 12 kHz	K1 × 2.7 dB		−16	−14	
		f ≥ 13.2 kHz	K1 × 3.2 dB			−40	
		f ≥ 15 kHz	K1 × 0 dB			−60	

† All typical values are at T_A = 25°C.

‡ The MIN, TYP, and MAX specifications are given for a 432-kHz SCF clock frequency. A slight error in the 432-kHz SCF may result from inaccuracies in the MSTR CLK frequency, resulting from crystal frequency tolerances. If this frequency error is less than 0.25%, the ADJUSTMENT ADDEND should be added to the MIN, TYP, and MAX specifications, where K1 = 100 • [(SCF frequency − 432 kHz)/432 kHz]. For errors greater than 0.25%, see Note 9.

NOTE 9: The filter gain outside of the pass band is measured with respect to the gain at 1 kHz. The filter gain within the pass band is measured with respect to the average gain within the pass band. The pass bands are 450 Hz to 10.95 kHz and 0 to 10.95 kHz for the band-pass and low-pass filters, respectively. For switched-capacitor filter clocks at frequencies other than 432 kHz, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 432 kHz.

Operating Characteristics Over Recommended Operating Free-Air Temperature Range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V

receive and transmit noise (measurement includes low-pass and band-pass switched-capacitor filters)

PARAMETER		TEST CONDITIONS	TYP†	MAX	UNIT
Transmit noise	broadband with (sin x)/x	DX = input = 00000000000000, constant input code	280	500	μV rms
	broadband without (sin x)/x		250	450	
	0 to 12 kHz with (sin x)/x		250	400	
	0 to 12 kHz without (sin x)/x		240	400	
Receive noise (see Note 10)		Inputs grounded, gain = 1	300	500	μV rms
			18		dBrnc0

† All typical values are at T_A = 25°C.

NOTE 10: The noise is computed by statistically evaluating the digital output of the A/D converter.

Timing Requirements

serial port recommended input signals

	PARAMETER	MIN	MAX	UNIT
$t_{c(MCLK)}$	Master clock cycle time	95		ns
$t_{r(MCLK)}$	Master clock rise time		10	ns
$t_{f(MCLK)}$	Master clock fall time		10	ns
	Master clock duty cycle	25%	75%	
	$\overline{\text{RESET}}$ pulse duration (see Note 11)	800		ns
$t_{su(DX)}$	DX setup time before SCLK↓	20		ns
$t_{h(DX)}$	DX hold time after SCLK↓	$t_{c(SCLK)}/4$		ns

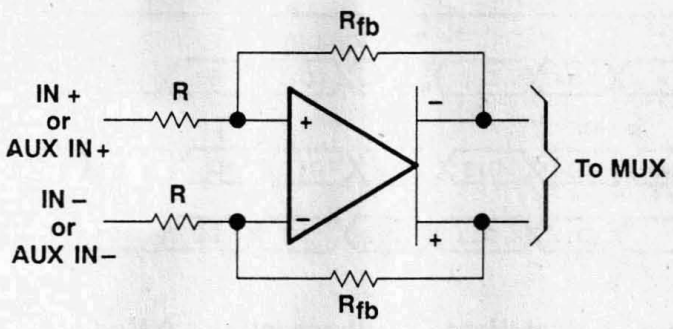
NOTE 11: $\overline{\text{RESET}}$ pulse duration is the amount of time that the reset pin is held below 0.8 V after the power supplies have reached their recommended values.

serial port – AIC output signals, C_L = 30 pF for SHIFT CLK output, C_L = 15 pF for all other outputs

	PARAMETER	MIN	TYP†	MAX	UNIT
$t_{c(SCLK)}$	Shift clock (SCLK) cycle time	380			ns
$t_{f(SCLK)}$	Shift clock (SCLK) fall time		3	8	ns
$t_{r(SCLK)}$	Shift clock (SCLK) rise time		3	8	ns
	Shift clock (SCLK) duty cycle	45		55	%
$t_{d(CH-FL)}$	Delay from SCLK↑ to $\overline{\text{FSR}}/\overline{\text{FSX}}/\overline{\text{FSD}}$↓		30		ns
$t_{d(CH-FH)}$	Delay from SCLK↑ to $\overline{\text{FSR}}/\overline{\text{FSX}}/\overline{\text{FSD}}$↑		35	90	ns
$t_{d(CH-DR)}$	DR valid after SCLK↑			90	ns
$t_{d(CH-EL)}$	Delay from SCLK↑ to $\overline{\text{EODX}}/\overline{\text{EODR}}$↓ in word mode			90	ns
$t_{d(CH-EH)}$	Delay from SCLK↑ to $\overline{\text{EODX}}/\overline{\text{EODR}}$↑ in word mode			90	ns
$t_{f(EODX)}$	$\overline{\text{EODX}}$ fall time		2	8	ns
$t_{f(EODR)}$	$\overline{\text{EODR}}$ fall time		2	8	ns
$t_{d(CH-EL)}$	Delay from SCLK↑ to $\overline{\text{EODX}}/\overline{\text{EODR}}$↓ in byte mode			90	ns
$t_{d(CH-EH)}$	Delay from SCLK↑ to $\overline{\text{EODX}}/\overline{\text{EODR}}$↑ in byte mode			90	ns
$t_{d(MH-SL)}$	Delay from MSTR CLK↑ to SCLK↓		65	170	ns
$t_{d(MH-SH)}$	Delay from MSTR CLK↑ to SCLK↑		65	170	ns

† Typical values are at T_A = 25°C.

Parameter Measurement Information



R_{fb} = R for D6 = 1 and D7 = 1
D6 = 0 and D7 = 0
R_{fb} = 2R for D6 = 1 and D7 = 0
R_{fb} = 4R for D6 = 0, and D7 = 1

Figure 12. IN+ and IN– Gain Control Circuitry

Table 7. Gain Control Table (Analog Input Signal Required for Full-Scale Bipolar A/D Conversion Twos Complement)†

INPUT CONFIGURATIONS	CONTROL REGISTER BITS		ANALOG INPUT‡§	A/D CONVERSION RESULT
	D6	D7		
Differential configuration Analog input = IN+ – IN– = AUX IN+ – AUX IN–	1	1	V_{ID} = ±6 V	±full scale
	0	0		
	1	0	V_{ID} = ±3 V	±full scale
	0	1	V_{ID} = ±1.5 V	±full scale
Single-ended configuration Analog input = IN+ – ANLG GND = AUX IN+ – ANLG GND	1	1	V_I = ±3 V	±half scale
	0	0		
	1	0	V_I = ±3 V	±full scale
	0	1	V_I = ±1.5 V	±full scale

† V_{CC+} = 5 V, V_{CC-} = –5 V, V_{DD} = 5 V
‡ V_{ID} = Differential Input Voltage, V_I = Input voltage referenced to ground with IN– or AUX IN– connected to ground.
§ In this example, V_{ref} is assumed to be 3 V. In order to minimize distortion, it is recommended that the analog input not exceed 0.1 dB below full scale.

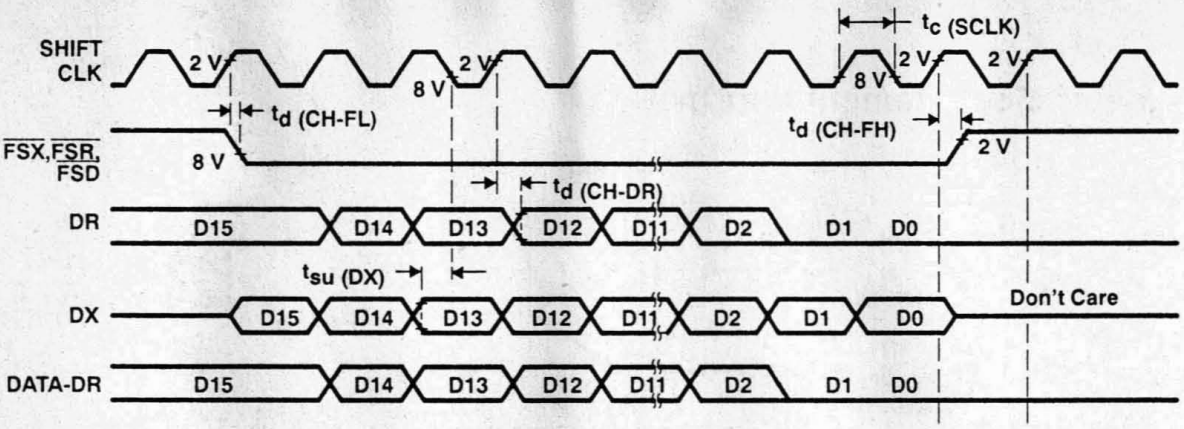


Figure 13. Dual-Word (Telephone Interface) Mode Timing

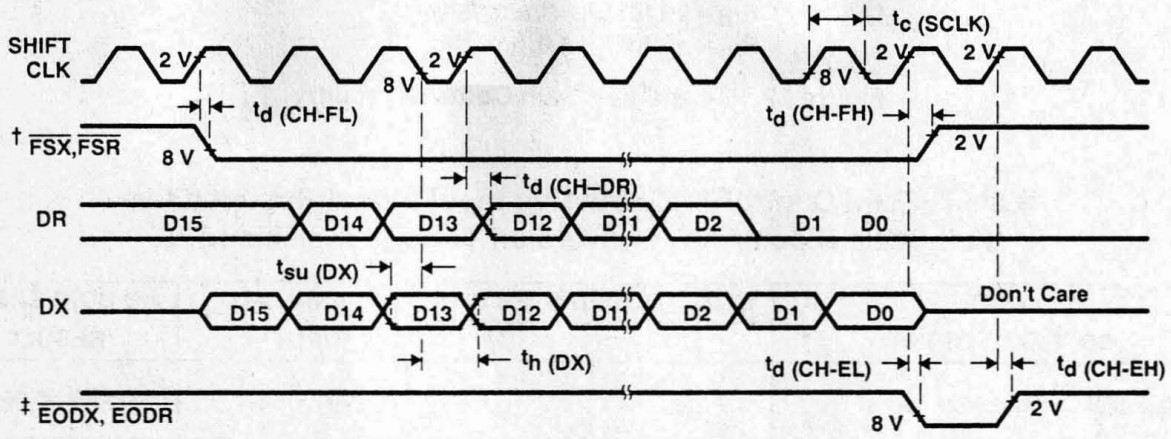


Figure 14. Word Timing

† The time between falling edges of $\overline{FSR}$ is the A/D conversion period and the time between falling edges of $\overline{FSX}$ is the D/A conversion period.

‡ In the word format, $\overline{EODX}$ and $\overline{EODR}$ go low to signal the end of a 16-bit data word to the processor. The word-cycle is 20 shift-clocks wide, giving a four-clock period setup time between data words.

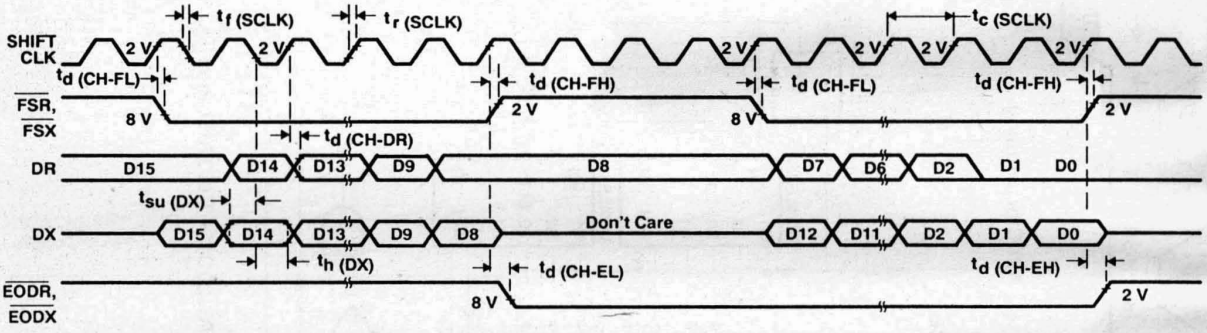


Figure 15. Byte–Mode Timing

† The time between falling edges of FSR is the A/D conversion period, and the time between fallling edges of $\overline{\text{FSX}}$ is the D/A conversion period.

‡ In the byte mode, when $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ is high, the first byte is transmitted or received, and when these signals are low, the second byte is transmitted or received. Each byte-cycle is 12 shift-clocks long, allowing for a four-shift-clock setup time between byte transmissions.

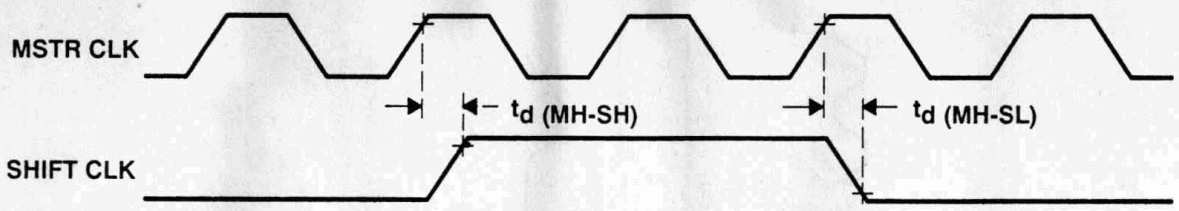


Figure 16. Shift-Clock Timing

TMS32047 – Processor Interface

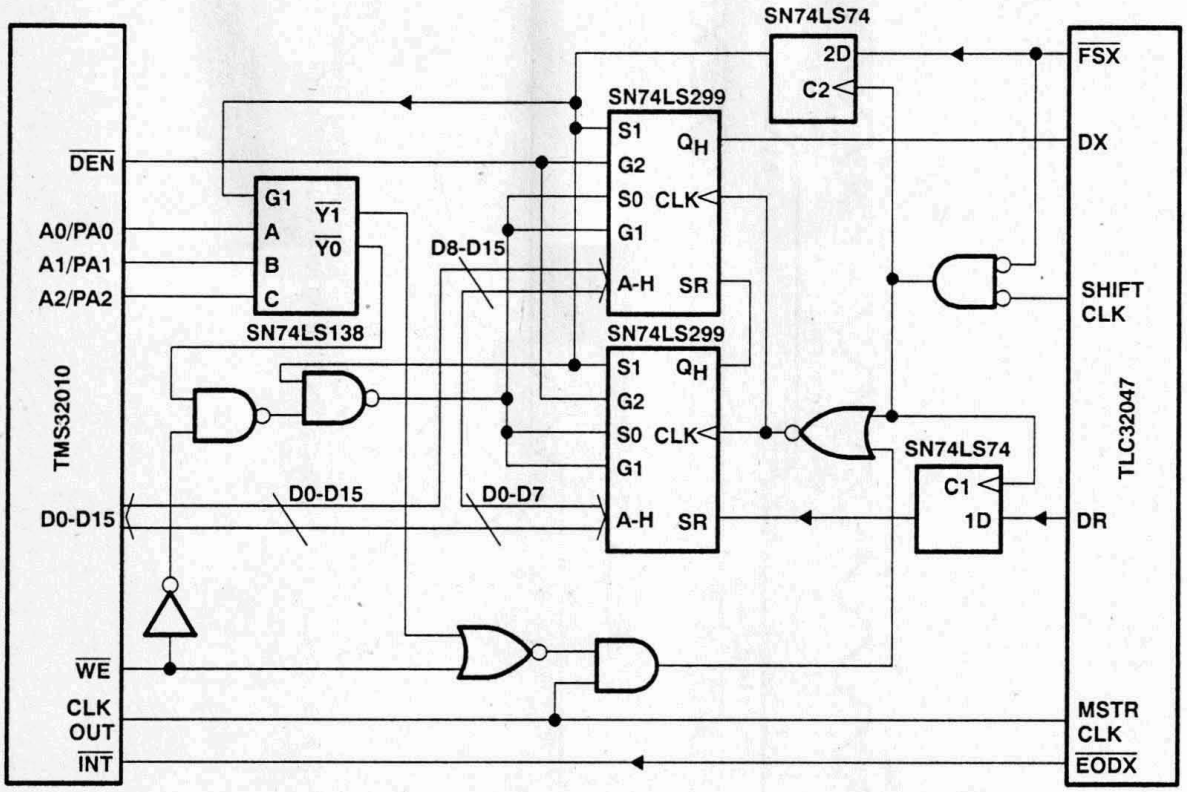
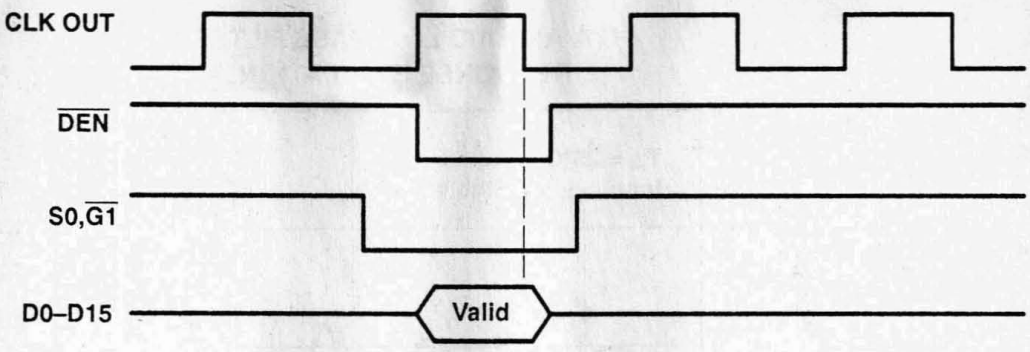


Figure 17. TMS32010/TMS320C15–TLC32047 Interface Circuit

IN instruction timing



OUT instruction timing

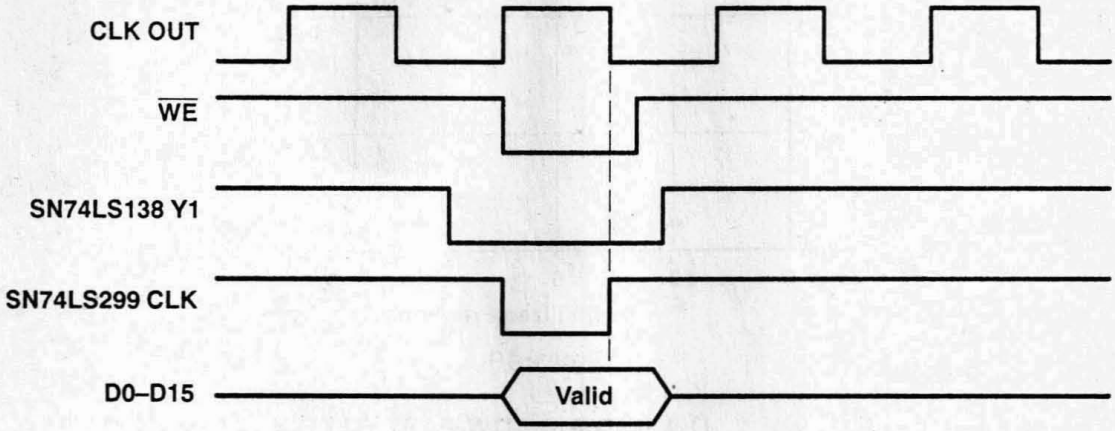


Figure 18. TMS32010/TMS320C15–TLC32047 Interface Timing

Typical Characteristics

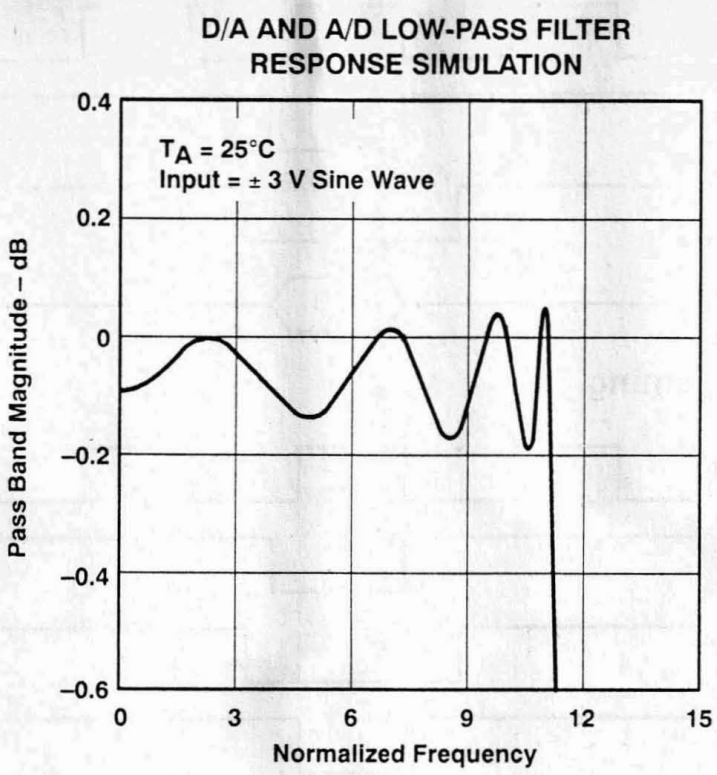


Figure 19

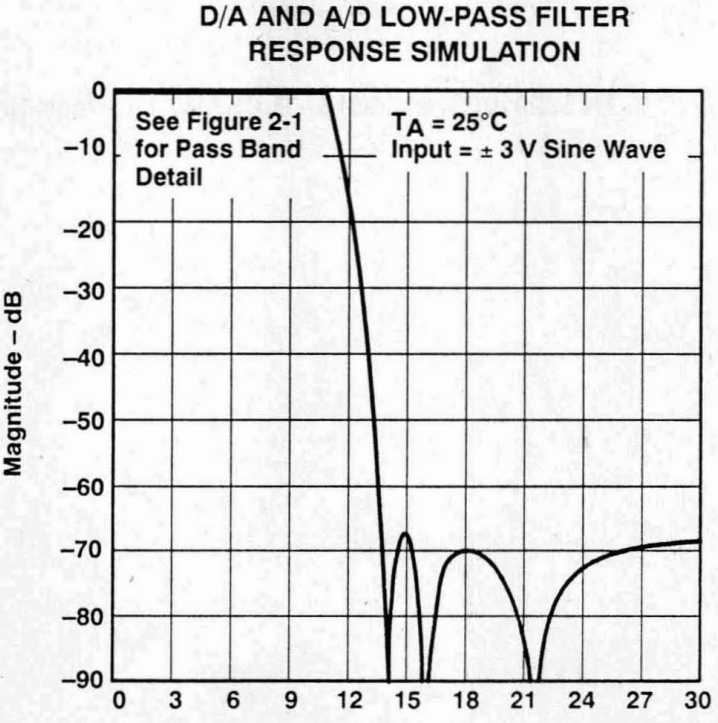


Figure 20

$$\text{NOTE : Absolute Frequency (kHz)} = \frac{\text{Normalized Frequency} \times \text{SCF } f_{clock} \text{ (kHz)}}{432}$$

D/A AND A/D LOW-PASS GROUP DELAY

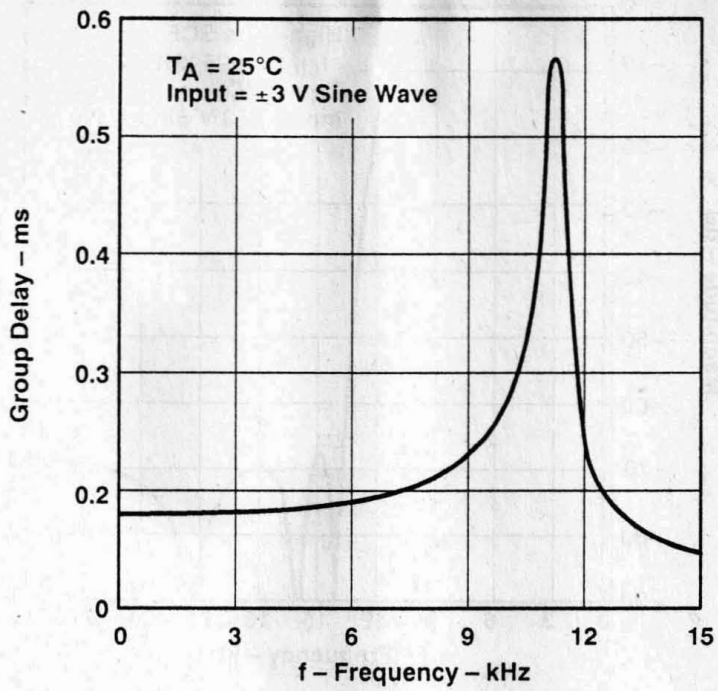


Figure 21

A/D BAND-PASS RESPONSE

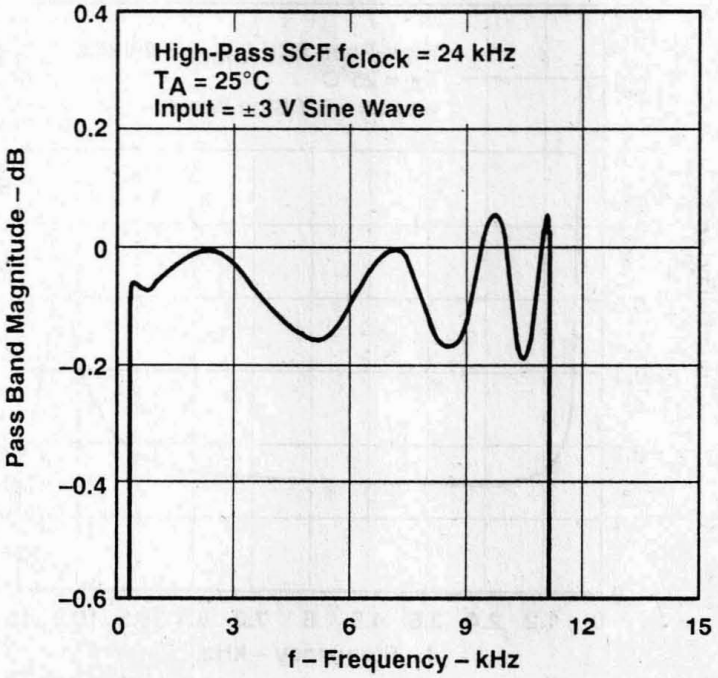


Figure 22

NOTE : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{SCF } f_{clock} \text{ (kHz)}}{432}$

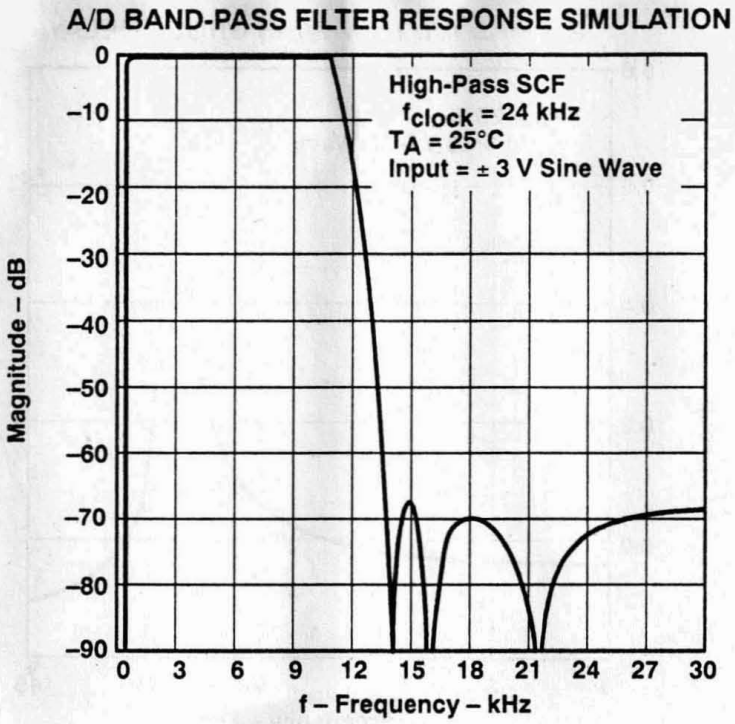


Figure 23

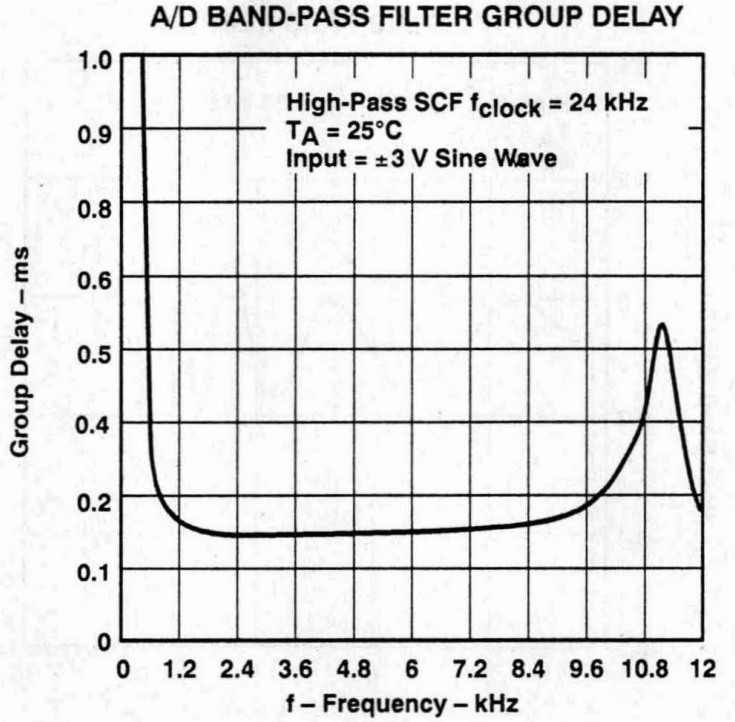


Figure 24

NOTE : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{SCF } f_{clock} \text{ (kHz)}}{432}$

A/D CHANNEL HIGH-PASS FILTER

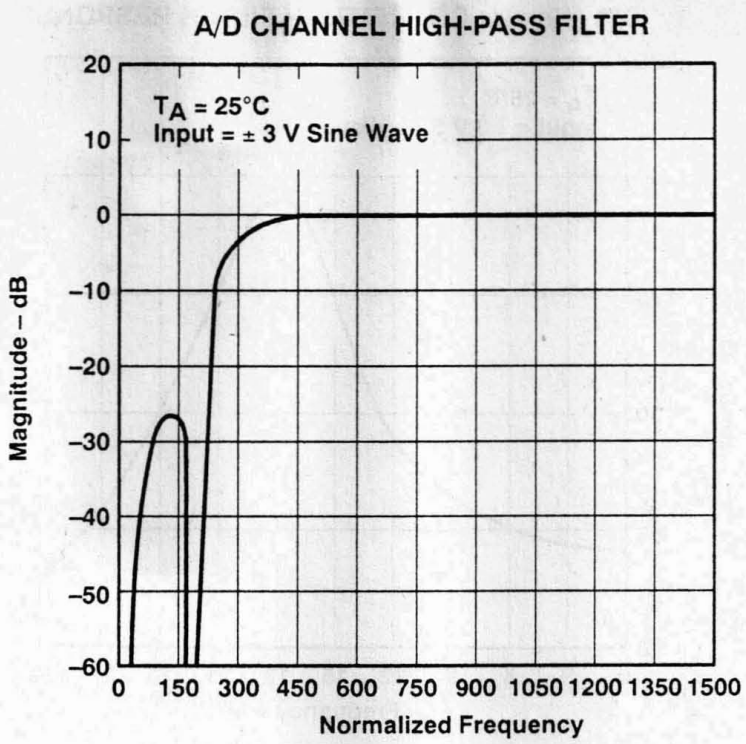


Figure 25

D/A (sin x)/x CORRECTION FILTER RESPONSE

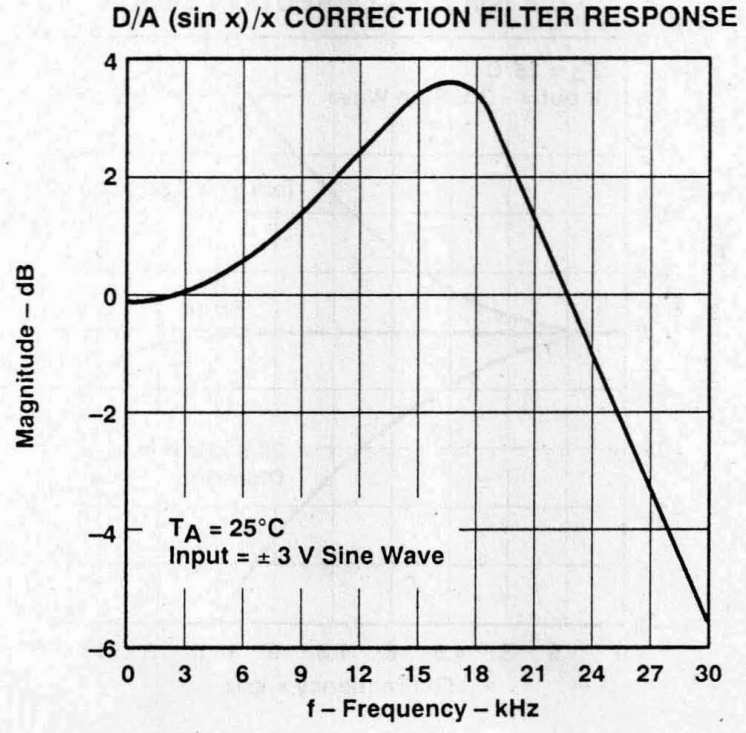


Figure 26

$$\text{NOTE : Absolute Frequency (kHz)} = \frac{\text{Normalized Frequency} \times \text{SCF } f_{clock} \text{ (kHz)}}{432}$$

D/A (sin x)/x CORRECTION FILTER RESPONSE

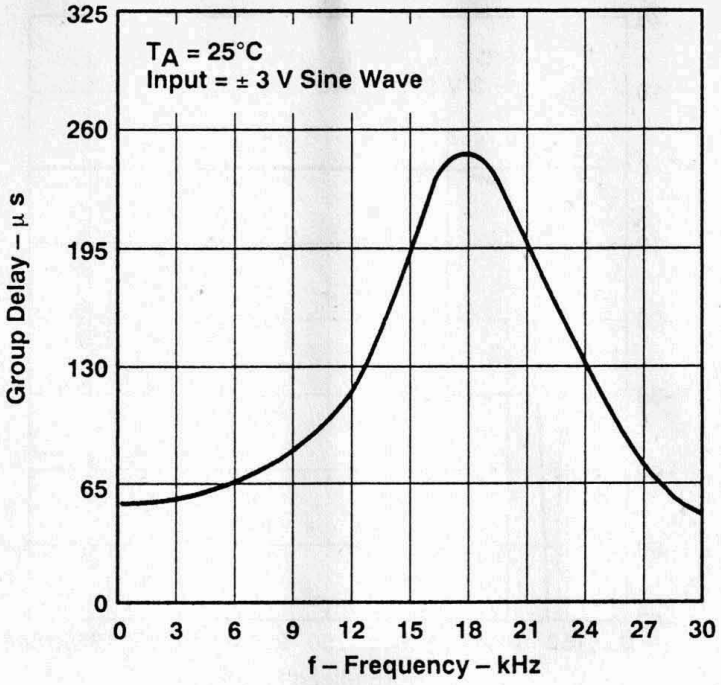


Figure 27

D/A (sin x)/x CORRECTION ERROR

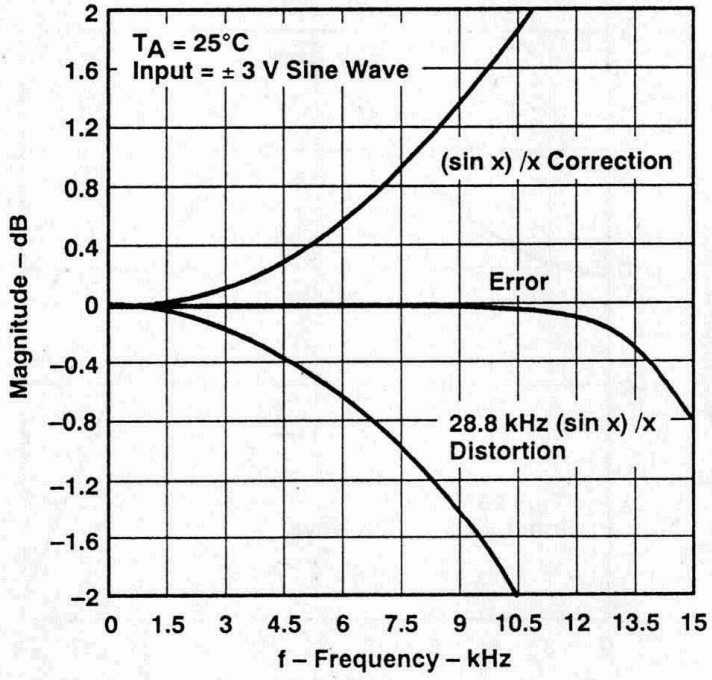


Figure 28

NOTE : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{SCF } f_{clock} \text{ (kHz)}}{432}$

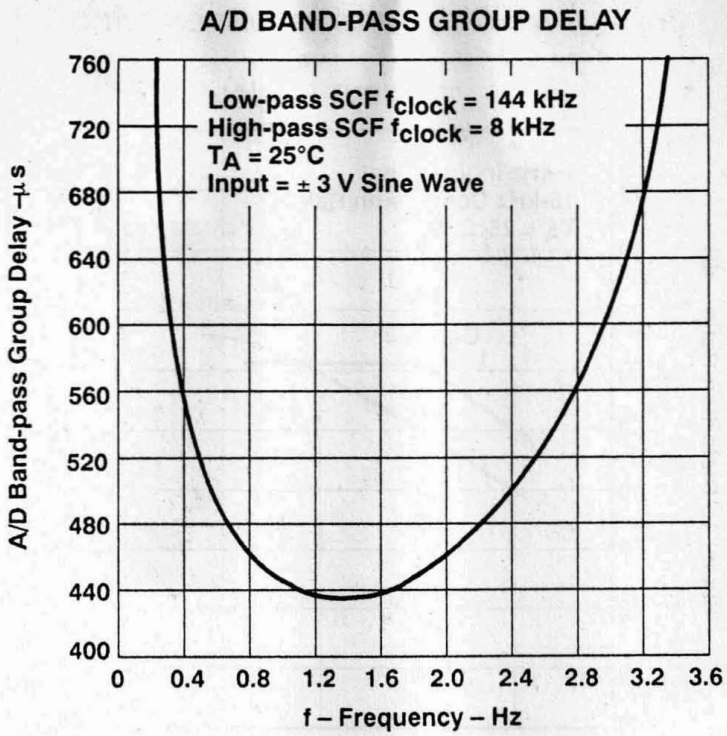


Figure 29

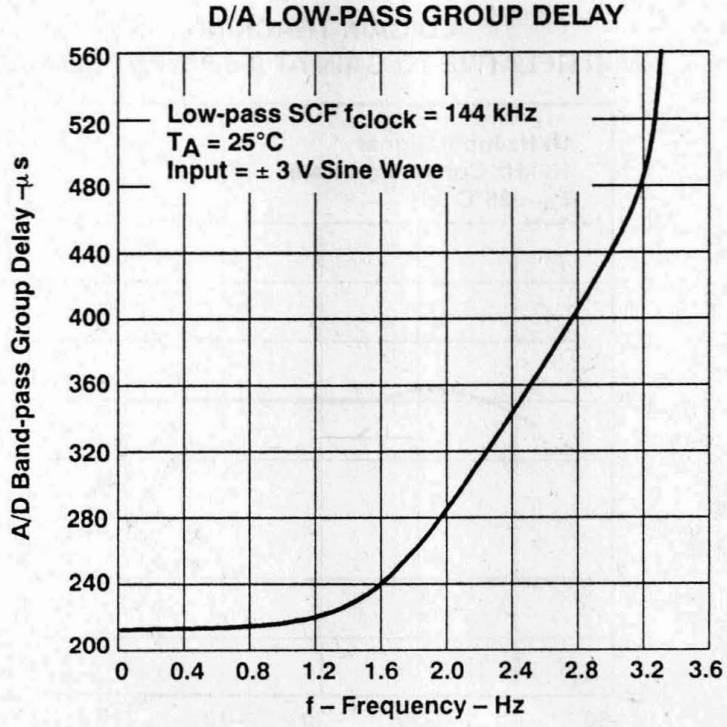


Figure 30

A/D SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL

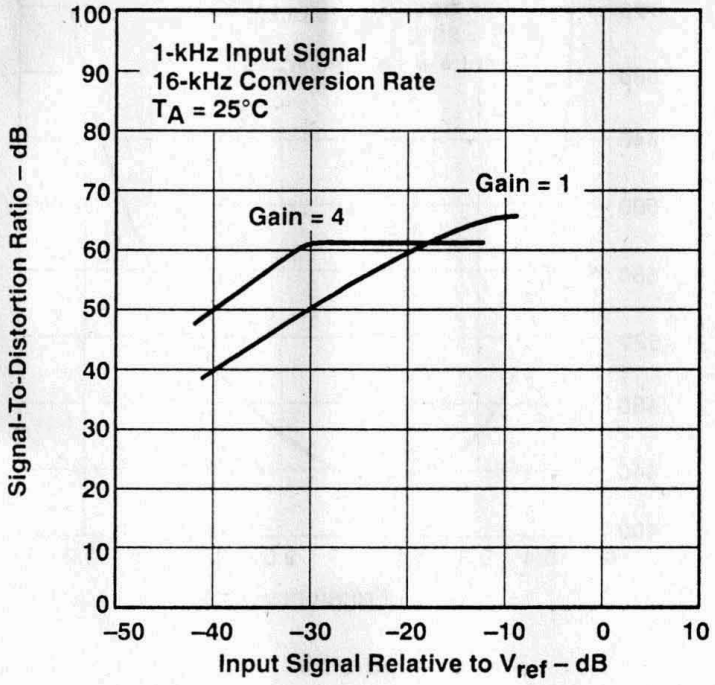


Figure 31

A/D GAIN TRACKING
(GAIN RELATIVE TO GAIN AT 0-dB INPUT SIGNAL)

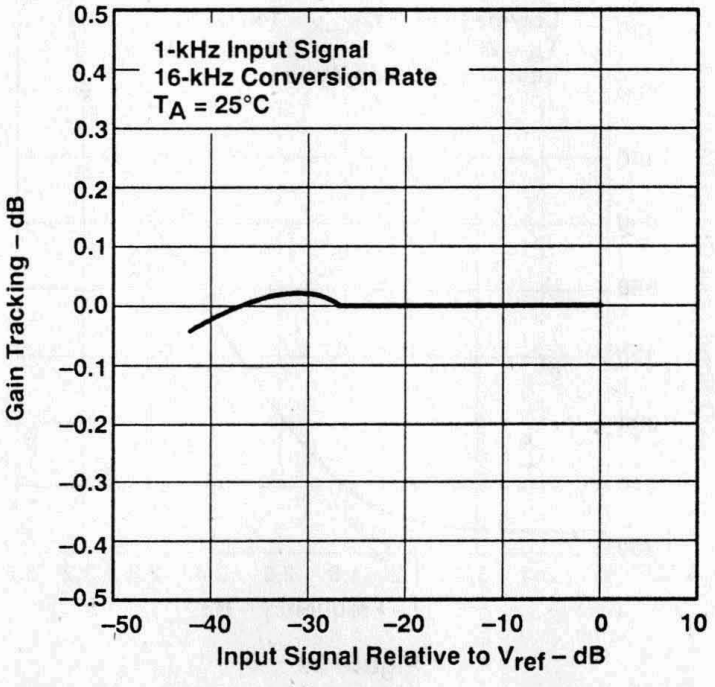


Figure 32

D/A CONVERTER SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL

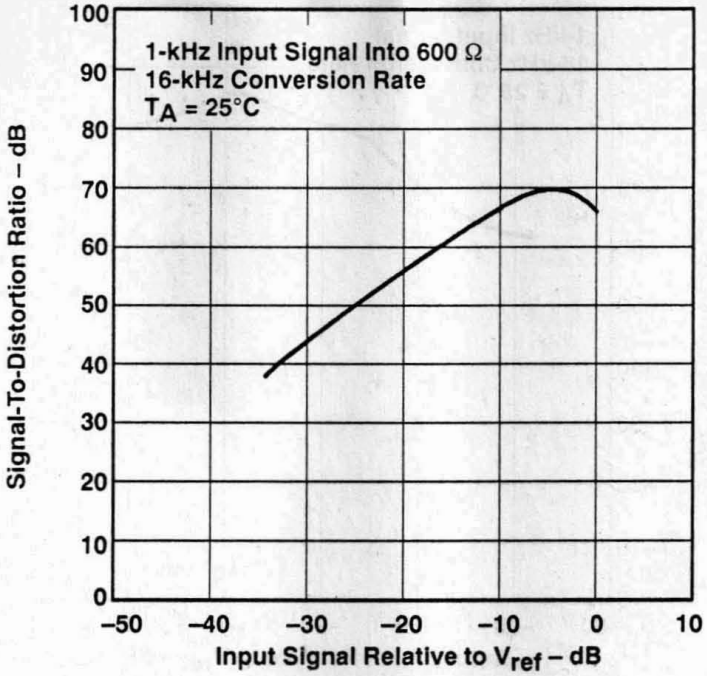


Figure 33

D/A GAIN TRACKING (GAIN RELATIVE TO GAIN
AT 0-dB INPUT SIGNAL)

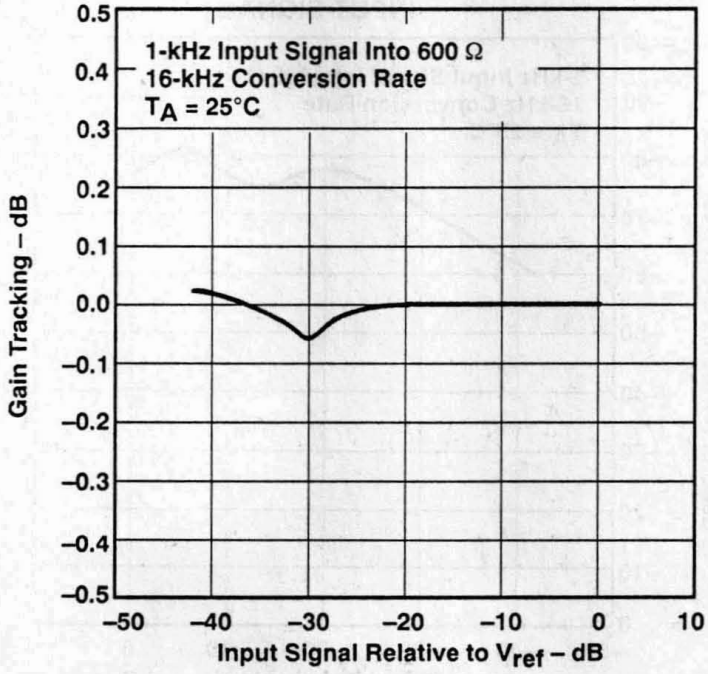


Figure 34

A/D SECOND HARMONIC DISTORTION
vs
INPUT SIGNAL

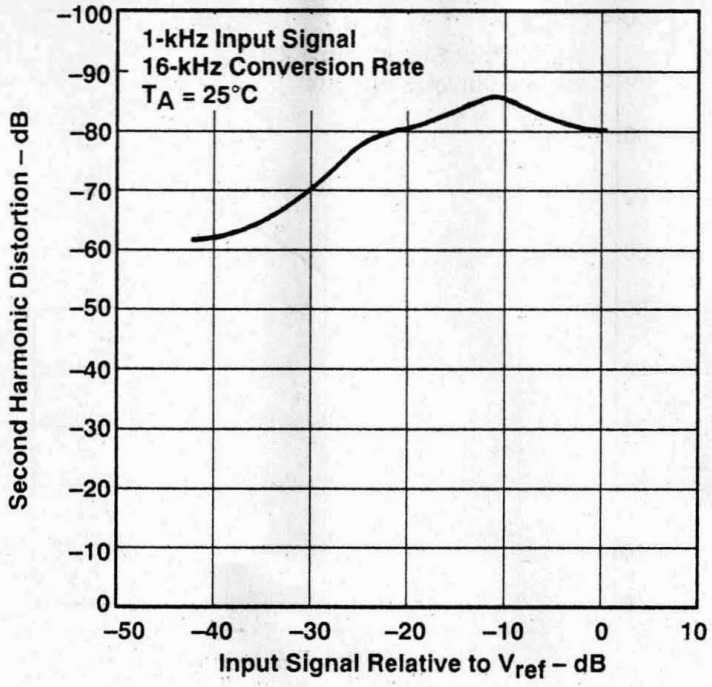


Figure 35

D/A SECOND HARMONIC DISTORTION
vs
INPUT SIGNAL

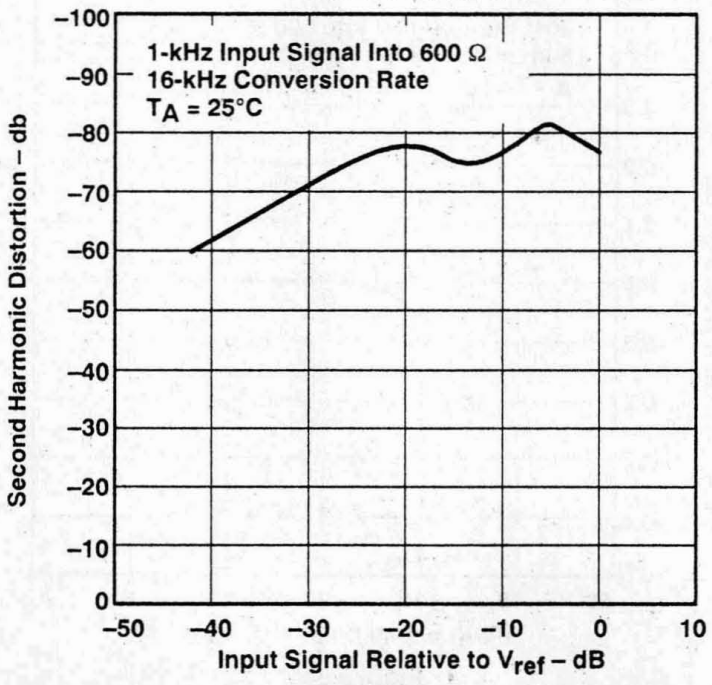


Figure 36

A/D THIRD HARMONIC DISTORTION
vs
INPUT SIGNAL

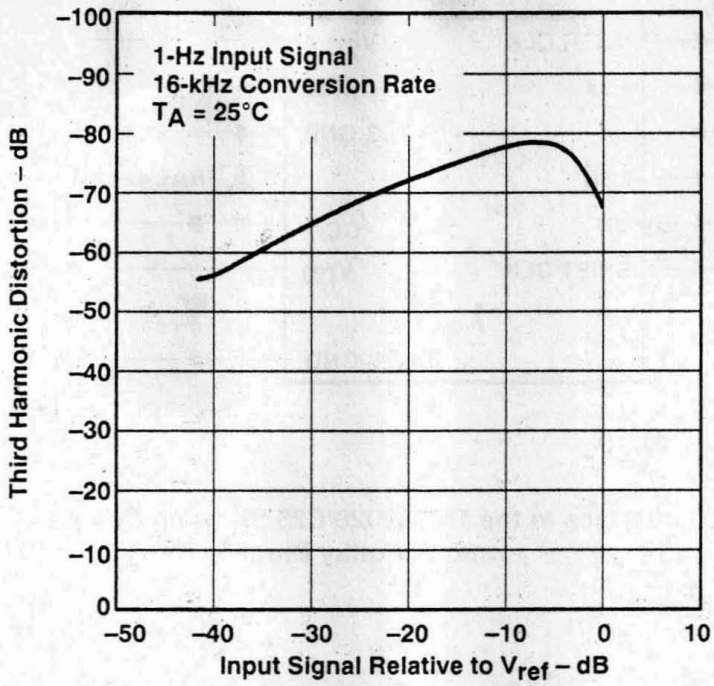


Figure 37

D/A THIRD HARMONIC DISTORTION
vs
INPUT SIGNAL

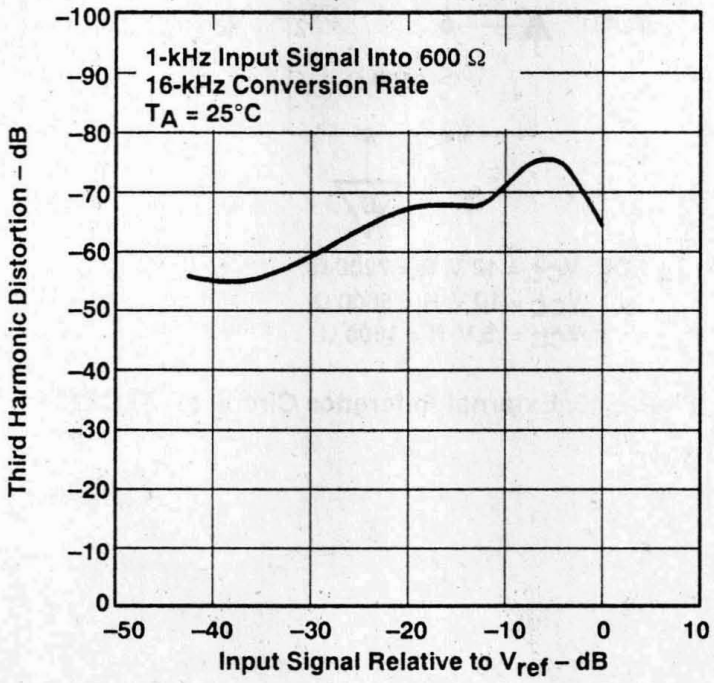


Figure 38

Application Information

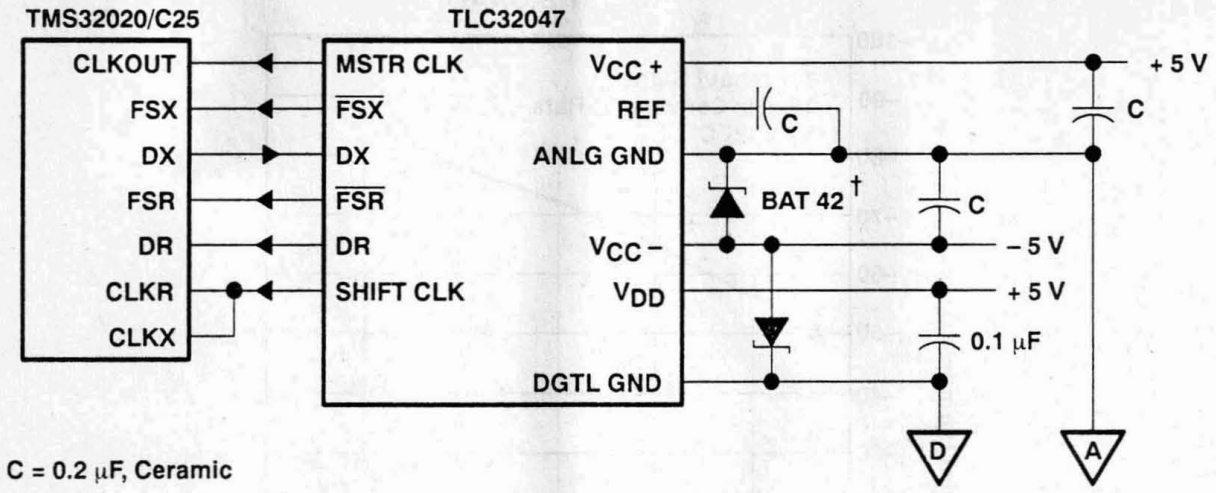
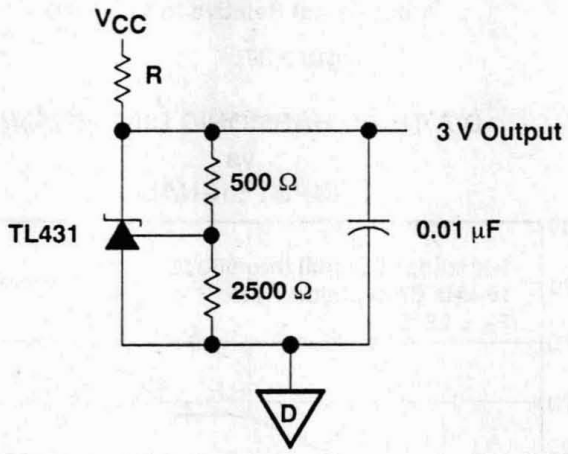


Figure 39. AIC Interface to the TMS32020/C25 Showing Decoupling Capacitors and Schottky Diode†

† Thomson Semiconductors



FOR: V_{CC} = 12 V, R = 7200 Ω
V_{CC} = 10 V, R = 5600 Ω
V_{CC} = 5 V, R = 1600 Ω

Figure 40. External Reference Circuit for TLC32047

TLC34075
Video Interface Palette

Data Manual

TEXAS INSTRUMENTS

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1 Introduction

The TLC34075 Video Interface Palette (VIP) is designed to provide lower system cost with a higher level of integration by incorporating all the high-speed timing, synchronizing, and multiplexing logic usually associated with graphics systems into one device, thus greatly reducing chip count. Since all high-speed signals (excluding the clock source) are contained on-chip, RF noise considerations are simplified. Maximum flexibility is provided through the pixel multiplexing scheme, which allows for 32-, 16-, 8-, and 4-bit pixel buses to be accommodated without any circuit modification. This enables the system to be easily reconfigured for varying amounts of available video RAM. Data can be split into 1, 2, 4, or 8 bit planes. The TLC34075 is software-compatible with the INMOS IMSG176/8 and Brooktree BT476/8 color palettes.

The TLC34075 features a separate VGA bus that allows data from the feature connector of most VGA-supported personal computers to be fed directly into the palette without the need for external data multiplexing. This allows a replacement graphics board to remain downward compatible by utilizing the existing graphics circuitry often located on the motherboard. The TLC34075 also provides a true color mode in which 24 (3 by 8) bits of color information are transferred directly from the pixel port to the DACs. This mode of operation supplies an overlay function using the 8 remaining bits of the pixel bus.

The TLC34075 has a 256-by-24 color lookup table with triple 8-bit video D/A converters capable of directly driving a doubly terminated 75-Ω line. Sync generation is incorporated on the green output channel. HSYNC and VSYNC are fed through the device and optionally inverted to indicate screen resolution to the monitor. A palette page register provides the additional bits of palette address when 1, 2, or 4 bit planes are used. This allows the screen colors to be changed with only one MPU write cycle.

Clocking is provided through one of four or five inputs (3 TTL- and either 1 ECL- or 2 TTL-compatible) and is software selectable. The video and shift clock outputs provide a software-selected divide ratio of the chosen clock input.

The TLC34075 can be connected directly to the serial port of VRAM devices, eliminating the need for any discrete logic. Support for split shift register transfers is also provided.

1.1 Features

- Versatile multiplexing interface allows lower pixel bus rate
- High level of integration provides lower system cost and complexity
- Direct VGA pass-through capability
- Directly interfaces to TMS34010/TMS34020 and other graphics processors
- Triple 8-bit D/A converters
- 66-, 85-, 110-, and 135-MHz versions
- 256-word color palette RAM
- Palette page register
- On-chip voltage reference
- RS-343A-compatible outputs
- TTL-compatible inputs
- Standard MPU interface
- Pixel word mask
- On-chip clock selection
- True color (direct addressing) mode
- Directly interfaces to video RAM
- Supports split shift register transfers
- Software downward-compatible with INMOS IMSG176/8 and Brooktree BT476/8 color palettes
- TIGA™-software-standard compatible
- LinEPIC™ 1-μm CMOS process

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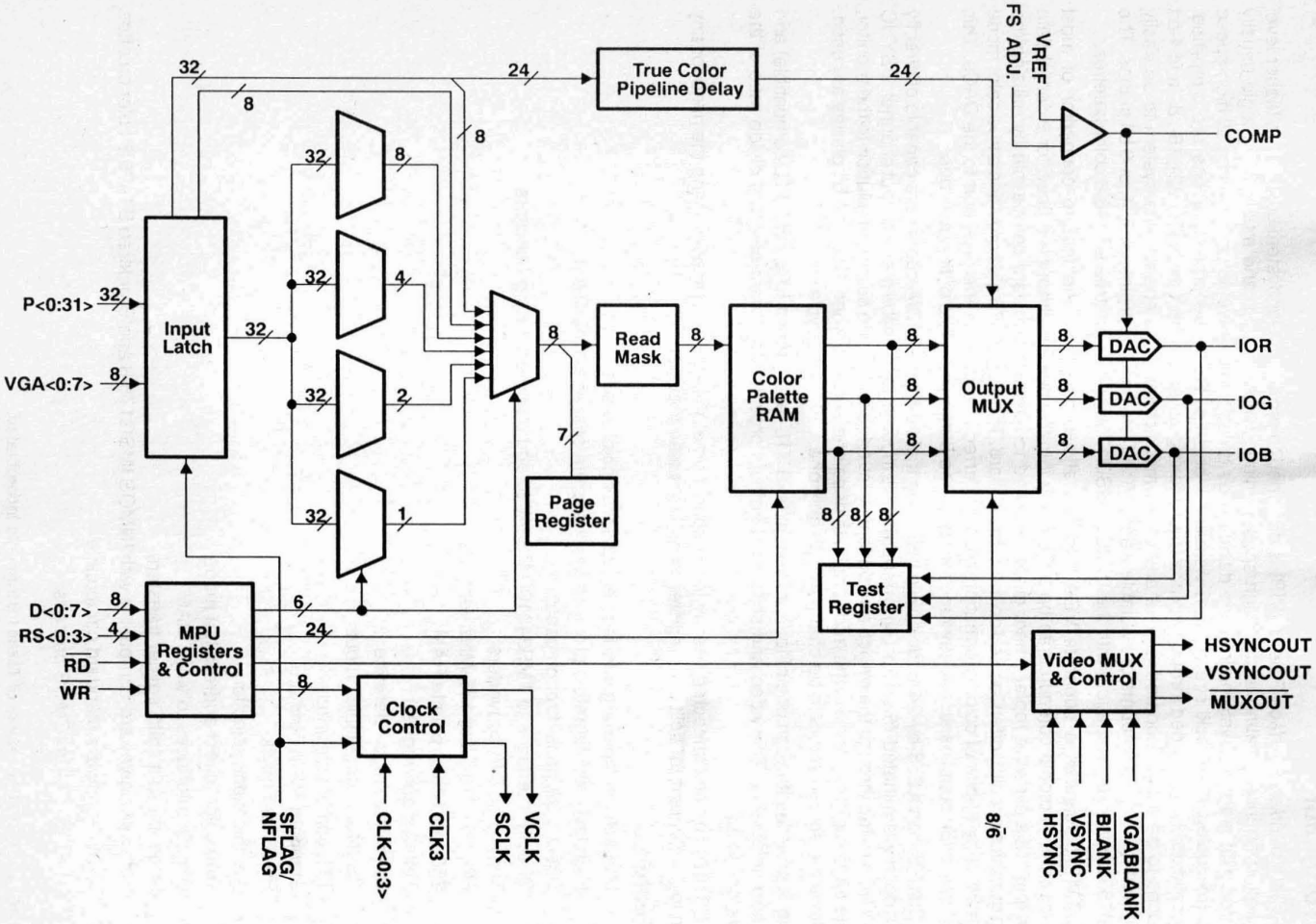


Figure 1. Functional Block Diagram

1.3 Terminal Assignments

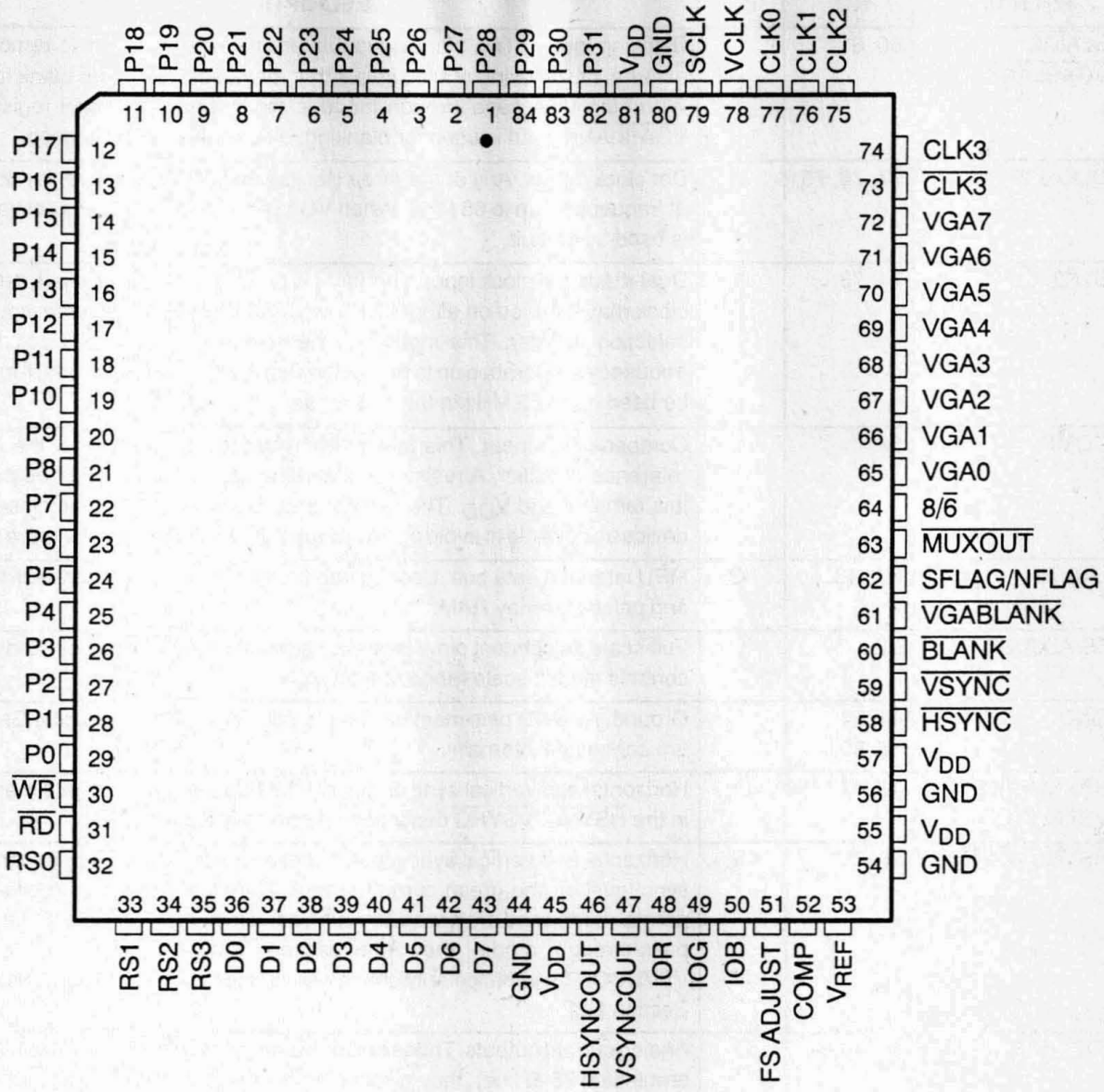


Figure 2. Terminal Assignments

1.4 Ordering Information

TLC34075 – (X)XX FN

Pixel clock frequency indicator

MUST CONTAIN TWO OR THREE CHARACTERS:

–66:	66-MHz pixel clock
–85:	85-MHz pixel clock
–110:	110-MHz pixel clock
–135:	135-MHz pixel clock

Package

MUST CONTAIN TWO LETTERS:

FN: plastic, square, leaded chip carrier (formed leads)

1.5 Terminal Functions

PIN NAME	NO.	I/O	DESCRIPTION
$\overline{\text{BLANK}}$, $\overline{\text{VGABLANK}}$	60, 61	I	Blanking inputs. Two blanking inputs are provided in order to remove any external multiplexing of the signals that may cause data and blank to skew. When the VGA pass-through mode is set in the mux control register, the $\overline{\text{VGABLANK}}$ input is used for blanking; otherwise, $\overline{\text{BLANK}}$ is used.
CLK<0:2>	77, 76, 75	I	Dot clock inputs. Any of the three clocks can be used to drive the dot clock at frequencies up to 85 MHz. When VGA pass-through mode is active, CLK0 is used by default.
CLK3, $\overline{\text{CLK3}}$	74, 73	I	Dual-mode dot clock input. This input is an ECL-compatible input, but a TTL clock may be used on either CLK3 or $\overline{\text{CLK3}}$ if so selected in the input clock selection register. This input may be selected as the dot clock for any frequency of operation up to the device limit while in the ECL mode; it may only be used up to 85 MHz in the TTL mode.
COMP	52	I	Compensation input. This terminal provides compensation for the internal reference amplifier. A resistor and ceramic capacitor are required between this terminal and V_{DD}. The resistor and capacitor must be as close to the device as possible to avoid noise pickup. Refer to Appendix B for more details.
D<0:7>	36–43	I/O	MPU interface data bus. Used to transfer data in and out of the register map and palette/overlay RAM.
FS ADJUST	51	I	Full-scale adjustment pin. A resistor connected between this pin and ground controls the full-scale range of the DACs.
GND	44, 54, 56, 80		Ground. All GND pins must be connected. The analog and digital GND pins are connected internally.
HSYNCOUT, VSYNCOUT	46, 47	O	Horizontal and vertical sync outputs of the true/complement gate mentioned in the $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$ description below (see Section 2.8).
$\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$	58, 59	I	Horizontal and vertical sync inputs. These signals are used to generate the sync level on the green current output. They are active-low inputs for the normal modes and are passed through a true/complement gate. For the VGA pass-through mode, they are passed through to HSYNCOUT and VSYNCOUT without polarity change as specified by the control register (see Section 2.8).
IOR, IOG, IOB	48, 49, 50	O	Analog current outputs. These outputs can drive a 37.5-Ω load directly (doubly terminated 75-Ω line), thus eliminating the need for any external buffering.
$\overline{\text{MUXOUT}}$	63	O	MUX output control. This output pin is software programmable. It is set low to indicate to external devices that VGA pass-through mode is being used when the MUX control register value is set to 2Dh. If bit 7 of the general control register is set high after the mode is set, this output goes high. This pin is only used for external control; it affects no internal circuitry.
P<0:31>	29–1, 84–82	I	Pixel input port. This port can be used in various modes as shown in the MUX control register. It is recommended that unused pins be tied to ground to lower the device's power consumption.
$\overline{\text{RD}}$	31	I	Read strobe input. A low logic level on this pin initiates a read from the TLC34075 register map. Reads are performed asynchronously and are initiated on the falling edge of $\overline{\text{RD}}$ (see Figure 3–1).
RS<0:3>	32–35	I	Register select inputs. These pins specify the location in the register map that is to be accessed, as shown in Table 2–1.
SCLK	79	O	Shift clock output. This output is selected as a submultiple of the dot clock input. SCLK is gated off during blanking.

PIN NAME	NO.	I/O	DESCRIPTION
SFLAG/NFLAG	62	I	Split shift register transfer flag or nibble flag input. This pin has two functions. When the general control register bit 3 = 0 and bit 2 = 1, split shift register transfer function is enabled and a low-to-high transition on this pin during a blank sequence initiates an extra SCLK cycle to allow a split shift register transfer in the VRAMs. When the general control register bit 3 = 1 and bit 2 = 0, special nibble mode is enabled and this input is sampled at the falling edge of VCLK. A high value sampled indicates that the next SCLK rising edge should latch the high nibble of each byte of the pixel data bus; a low value sampled indicates that the low nibble of each byte of the pixel data bus should be latched (see Section 2.9). When the general control register bit 3 = 0 and bit 2 = 0, this pin is ignored. The condition of bit 3 = 1, bit 2 = 1 is not allowed, and device operation is unpredictable if they are so set.
VCLK	78	O	Video clock output. User-programmable output for synchronization of the TLC34075 to a graphics processor.
V_{DD}	45, 55, 57, 81		Power. All V_{DD} pins must be connected. The analog and digital V_{DD} pins are connected internally.
VGA<0:7>	65–72	I	VGA pass-through bus. This bus can be selected as the pixel bus for VGA pass-through mode. It does not allow for any multiplexing.
V_{REF}	53		Voltage reference for DACs. An internal voltage reference of nominally 1.235 V is designed in. A 0.1-μf ceramic capacitor between this terminal and GND is recommended for noise filtering using either the internal or an external reference voltage. The internal reference voltage can be overridden by an externally supplied voltage. The typical connection is shown in Appendix B.
$\overline{WR}$	30	I	Write strobe input. A low logic level on this pin initiates a write to the TLC34075 register map. Write transfers are asynchronous. The data written to the register map is latched on the rising edge of $\overline{WR}$ (see Figure 3–1).
8/$\overline{6}$	64	I	DAC resolution selection. This pin is used to select the data bus width (8 or 6 bits) for the DACs and is provided to maintain compatibility with the INMOS IMSG176/8 color palette. When this pin is at a high logic level, 8-bit bus transfers are used, with D<7> being the MSB and D<0> the LSB. For 6-bit bus operation, while the color palette still has the 8-bit information, D<5> shifts to the bit 7 position, D<0> shifts to the bit 2 position, and the two LSBs are filled with zeros at the output MUX to the DAC. When read in the 6-bit mode, the palette-holding register zeroes out the two MSBs.

NOTES: 1. Although leaving unused pins floating will not adversely affect device operation, tying unused pins to ground lowers power consumption and, thus, is recommended.
2. All digital inputs and outputs are TTL-compatible, unless otherwise noted.

2 Detailed Description

2.1 MPU Interface

The processor interface is controlled via read and write strobes ($\overline{RD}$, $\overline{WR}$), four register select pins (RS<0:3>), and the 8/$\overline{6}$ select pin. The 8/$\overline{6}$ select pin is used to select between 8- or 6-bit operation and is provided in order to maintain compatibility with the IMSG176/8 color palette. This operation is carried out in order to utilize the maximum range of the DACs.

The internal register map is shown in Table 1. The MPU interface operates asynchronously, with data transfers being synchronized by internal logic. All the register locations support read and write operations.

Table 1. Internal Register Map

RS3	RS2	RS1	RS0	REGISTER ADDRESSED BY MPU
L	L	L	L	Palette address register – write mode
L	L	L	H	Color palette holding register
L	L	H	L	Pixel read mask
L	L	H	H	Palette address register – read mode
L	H	L	L	Reserved
L	H	L	H	Reserved
L	H	H	L	Reserved
L	H	H	H	Reserved
H	L	L	L	General control register
H	L	L	H	Input clock selection register
H	L	H	L	Output clock selection register
H	L	H	H	Mux control register
H	H	L	L	Palette page register
H	H	L	H	Reserved
H	H	H	L	Test register
H	H	H	H	Reset state

2.2 Color Palette RAM

The color palette RAM is addressed by two internal 8-bit registers, one for reading from the RAM and one for writing to the RAM. These registers are automatically incremented following a RAM transfer, allowing the entire palette to be read/written with only one access of the address register. When the address register increments beyond the last location in RAM, it is reset to the first location (address 0). Although all read and write accesses to the RAM are asynchronous to SCLK, VCLK, and the dot clock, they are performed within one dot clock and so do not cause any noticeable disturbance on the display.

The color palette RAM is 24 bits wide for each location (8 bits each for red, green, and blue). If 6-bit mode is chosen (8/$\overline{6}$ = low), the two MSBs are still written to the color palette RAM. However, if they are read back in the 6-bit mode, the two MSBs are set to 0 to maintain compatibility with the IMSG176/8 and BT476/8 color palettes. The output MUX shifts the six LSBs to the six MSB positions, fills the two LSBs with 0s, then feeds the eight bits to the DAC. With the 8/$\overline{6}$ pin held low, data on the lowest six bits of the data bus are internally shifted up by two bits to occupy the upper six bits at the output MUX, and the bottom two bits are then zeroed. The test register and the ones accumulation register both take data before the output MUX to give the user the maximum flexibility.

The color palette RAM access methodology is described in the following two sections and is fully compatible with the IMSG176/8 and BT476/8 color palettes.

2.2.1 Writing to the Color Palette RAM

To load the color palette RAM, the MPU must first write to the address register (write mode) with the address where the modification is to start. This action is followed by three successive writes to the palette-holding register with eight bits each of red, green, and blue data. After the blue data write cycle, the three bytes of color are concatenated into a 24-bit word and written to the color palette RAM location specified by the address register. The address register then increments to point to the next color palette RAM location, which the MPU may modify by simply writing another sequence of red, green, and blue data bytes. A block of color values in consecutive locations may be written to by writing the start address and performing continuous red, green, and blue write cycles until the entire block has been written.

2.2.2 Reading From the Color Palette RAM

Reading from the color palette RAM is performed by writing the location to be read to the address register. This action initiates a transfer from the color palette RAM into the holding register followed by an increment of the address register. Three successive MPU reads from the holding register produce red, green, and blue color data (six or eight bits, depending on the 8/$\overline{6}$ mode) for the specified location. Following the blue read cycle, the contents of the color palette RAM at the address specified by the address register are copied into the holding register and the address register is again incremented. As with writing to the color palette RAM, a block of color values in consecutive locations may be read by writing the start address and performing continuous red, green, and blue read cycles until the entire block has been read.

2.2.3 Palette Page Register

The 8-bit palette page register provides high-speed color changing by removing the need for color palette RAM reloading. When using 1, 2, or 4 bit planes, the additional planes are provided by the palette page register; e.g., when using four bit planes, the pixel inputs specify the lower four bits of the color palette RAM address with the upper four bits being specified by the palette register. This provides the capability of selecting from 16 palette pages with only one chip access, thus allowing all the screen colors to be changed at the line frequency. A bit-to-bit correspondence is used; therefore, in the above configuration, palette page register bits 7 through 4 map onto color palette RAM address bits 7 through 4, respectively. This is illustrated below.

NOTE: The additional bits from the palette page register are inserted before the read mask and hence, are subject to masking.

Table 2. Allocation of Palette Page Register Bits

NUMBER OF BIT PLANES	COLOR PALETTE RAM ADDRESS BITS							
	msb							isb
8	M	M	M	M	M	M	M	M
4	P7	P6	P5	P4	M	M	M	M
2	P7	P6	P5	P4	P3	P2	M	M
1	P7	P6	P5	P4	P3	P2	P1	M

Pn = nth bit from palette page register
M = bit from pixel port

2.3 Input/Output Clock Selection and Generation

The TLC34075 provides a maximum of five clock inputs. Three are dedicated to TTL inputs; the other two can be selected as either one ECL input or two extra TTL inputs. The TTL inputs can be used for video rates up to 85 MHz, above which an ECL clock source must be used (although the ECL clock may also be used at lower frequencies). The dual-mode clock input (ECL/TTL) is primarily an ECL input but can be used as a TTL-compatible input if the input clock selection register is so programmed. The clock source used at power-up is CLK0; an alternative source can be selected by software during normal operation. This chosen clock input is used unmodified as the dot clock (representing the pixel rate to the monitor). The device does,

however, allow for user programming of the SCLK and VCLK outputs (shift and video clocks) via the output clock selection register. The input/output clock selection registers are shown in Tables 5, 6, and 7.

SCLK is designed to drive the VRAMs directly, and VCLK is designed to work with video control signals such as $\overline{\text{BLANK}}$ and the SYNCs. While SCLK and VCLK are designed as general-purpose shift clock and video clock, respectively, they also interface directly with the TMS340x0 GSP family. While SCLK and VCLK can be selected independently, there is still a relationship between the two. Internally, both SCLK and VCLK are generated from a common clock counter that increments on the rising edge of the DOTCLK. When VCLK is enabled and the VCLK and SCLK frequencies are programmed to be the same submultiple of the DOTCLK frequency, then VCLK and SCLK are in phase. When VCLK is enabled and the VCLK and SCLK frequencies are programmed to be different submultiples of the DOTCLK frequency, then there are simultaneous rising edges on the two waveforms at times determined by their frequency ratio (see Figure 3).

Appendix A discusses the SCLK/VCLK relationship specific to the TMS340x0 GSP.

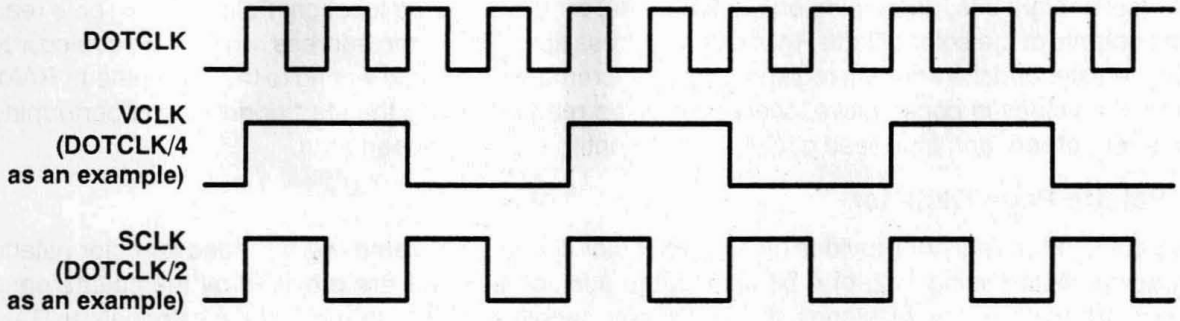


Figure 3. DOTCLK/VCLK/SCLK Relationship

Table 3. Input Clock Selection Register Format

BITS†				FUNCTION‡
3	2	1	0	
0	0	0	0	Select CLK0 as clock source§
0	0	0	1	Select CLK1 as clock source
0	0	1	0	Select CLK2 as clock source
0	0	1	1	Select CLK3 as TTL clock source
0	1	0	0	Select $\overline{\text{CLK3}}$ as TTL clock source
1	0	0	0	Select CLK3 and $\overline{\text{CLK3}}$ as ECL clock sources

† Register bits 4, 5, 6, and 7 are *don't care* bits.

‡ When the clock selection is altered, a minimum 30-ns delay is incurred before the new clocks are stabilized and running.

§ CLK0 is chosen at power-up to support the VGA pass-through mode.

Table 4. Output Clock Selection Register Format

BITS †						FUNCTION ‡
5	4	3	2	1	0	
0	0	0	X	X	X	VCLK frequency = DOTCLK frequency
0	0	1	X	X	X	VCLK frequency = DOTCLK frequency/2
0	1	0	X	X	X	VCLK frequency = DOTCLK frequency/4
0	1	1	X	X	X	VCLK frequency = DOTCLK frequency/8
1	0	0	X	X	X	VCLK frequency = DOTCLK frequency/16
1	0	1	X	X	X	VCLK frequency = DOTCLK frequency/32
1	1	X	X	X	X	VCLK output held at logic high level (default condition) §
X	X	X	0	0	0	SCLK frequency = DOTCLK frequency
X	X	X	0	0	1	SCLK frequency = DOTCLK frequency/2
X	X	X	0	1	0	SCLK frequency = DOTCLK frequency/4
X	X	X	0	1	1	SCLK frequency = DOTCLK frequency/8
X	X	X	1	0	0	SCLK frequency = DOTCLK frequency/16
X	X	X	1	0	1	SCLK frequency = DOTCLK frequency/32
X	X	X	1	1	X	SCLK output held at logic level low (default condition) §

† Register bits 6 and 7 are *don't care* bits.

‡ When the clock selection is altered, a minimum 30-ns delay is incurred before the new clocks are stabilized and running.

§ These lines indicate the power-up conditions required to support the VGA pass-through mode.

Table 5. VCLK/SCLK Divide Ratio Selection (Output Clock Selection Register Value in Hex)

SCLK / VCLK	BITS 2. . . 0¶	000	001	010	011	100	101
BITS 5. . .3¶	divide DOTCLK by / divide DOTCLK by	1	2	4	8	16	32
000	1	00	01	02	03	04	05
001	2	08	09	0A	0B	0C	0D
010	4	10	11	12	13	14	15
011	8	18	19	1A	1B	1C	1D
100	16	20	21	22	23	24	25
101	32	28	29	2A	2B	2C	2D

¶ Output clock selection register bits

2.3.1 SCLK

The TLC34075 latches data on the rising edge of the LOAD signal (LOAD is the same as SCLK but is not disabled while the $\overline{\text{BLANK}}$ signal is active). Therefore, SCLK must be set as a function of the pixel bus width and the number of bit planes. The SCLK frequency can be selected to be the same as the dot clock frequency or 1/2, 1/4, 1/8, 1/16, or 1/32 of the dot clock frequency. If SCLK is not used, the output is switched off and held low to protect against VRAM lock-up due to invalid SCLK frequencies. SCLK is also held low during the $\overline{\text{BLANK}}$ signal active period. The control timing has been designed to bring the first pixel data ready from the VRAM when $\overline{\text{BLANK}}$ is disabled and ready for the display. When split shift register transfer operation is used, SCLK is taken care of by working with SSRT input (see Section 2.9).

Refer to Figure 2–2 for the following timing explanation.

The falling edge of VCLK is used internally by the TLC34075 to sample and latch the $\overline{\text{BLANK}}$ input level. When $\overline{\text{BLANK}}$ goes low, SCLK is disabled as soon as possible. In other words, if the last SCLK pulse is at the high level while the sampled $\overline{\text{BLANK}}$ is low, SCLK is allowed to finish its cycle to low level, then SCLK is held low until the sampled $\overline{\text{BLANK}}$ goes back high to enable it again. The VRAM shift register should be updated during the $\overline{\text{BLANK}}$ active period, and the first SCLK pulse is used to clock the first valid pixel data from the VRAM. The internal pipeline delay of the $\overline{\text{BLANK}}$ input is designed to be in phase with data at the DAC output to the monitors. The logic described above works in situations wherein the SCLK period is shorter than, equal to, or longer than the VCLK period.

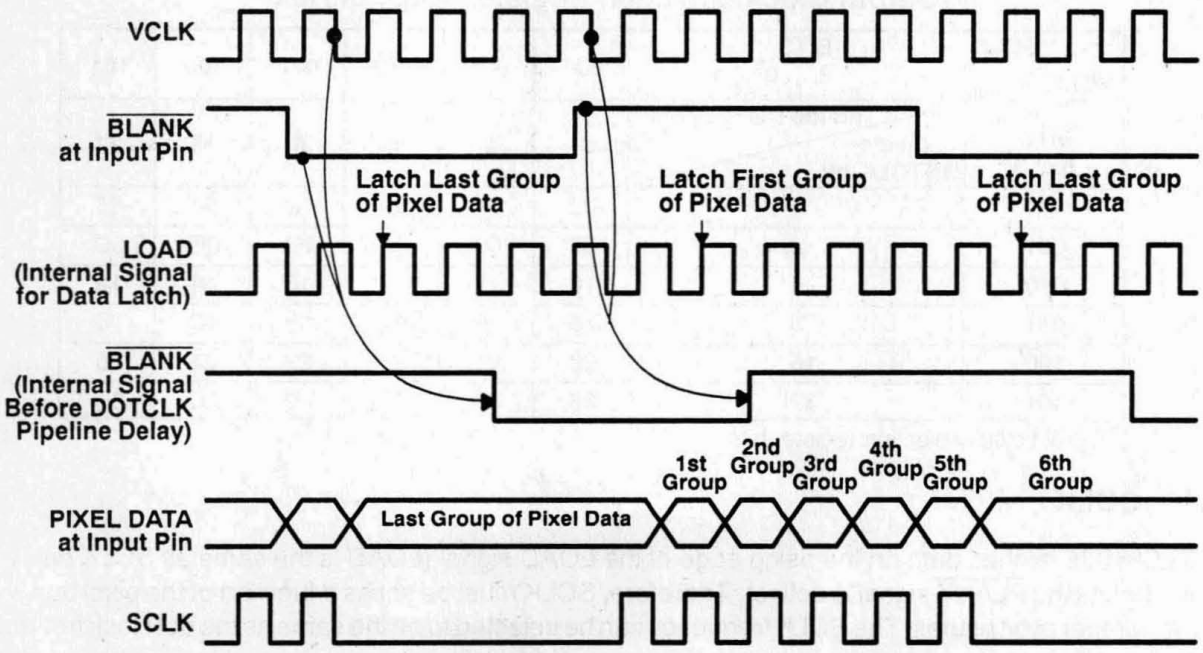
Figure 5 shows the case wherein the SSRT (split shift register transfer) function is enabled. One SCLK pulse with a minimum width of 15 ns is generated from the rising edge at the SFLAG input with specified delay. This is designed to meet the VRAM timing requirement, and this SCLK pulse replaces the first SCLK in the regular shift register transfer case as described above. Refer to Section 2.9 for the detailed explanation of the SSRT function.

The SCLK output waveform may vary at the time that the sampled $\overline{\text{BLANK}}$ input is low. Refer to Appendix C for details.

2.3.2 VCLK

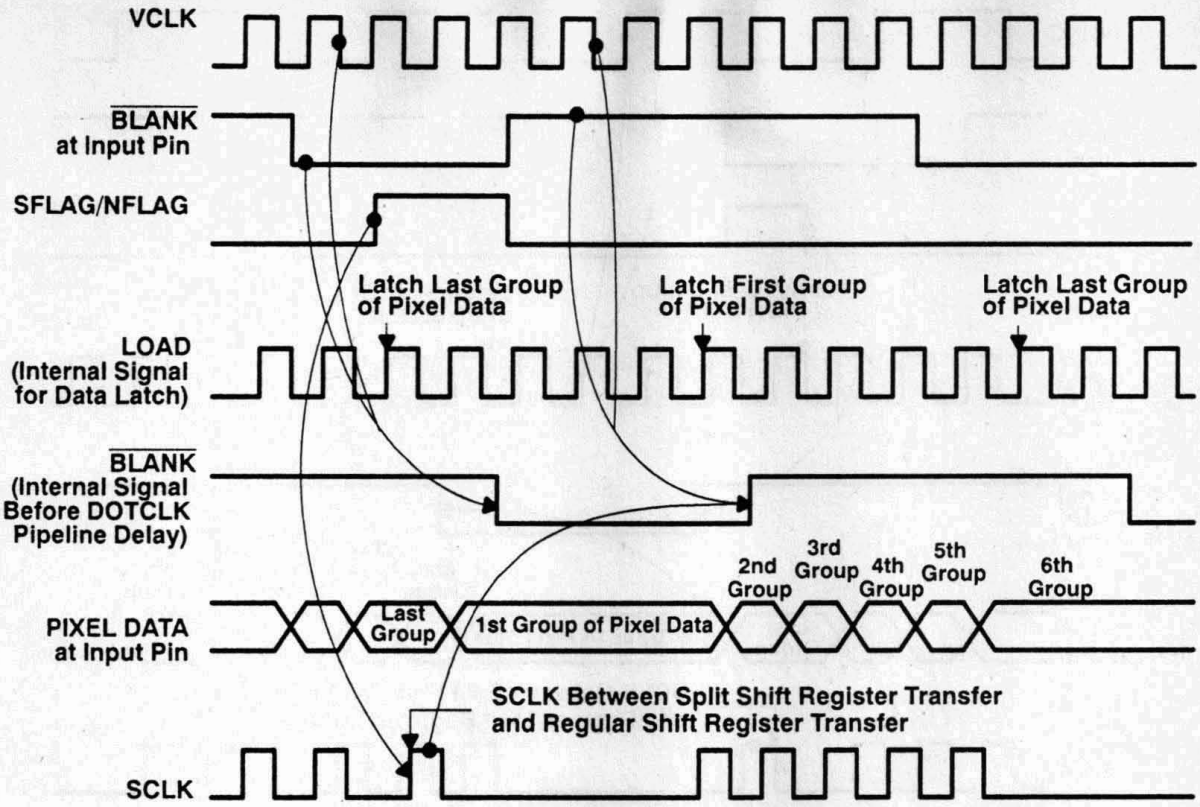
The VCLK frequency can be selected to be 1/1, 1/2, 1/4, 1/8, 1/16, or 1/32 of that of the dot clock, or it can be held at a high logic level. The default condition is for VCLK to be held at a high logic level. VCLK is not used in VGA pass-through mode.

VCLK is used by a GSP or custom-designed control logic to generate control signals ($\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, and $\overline{\text{VSYNC}}$). As can be seen from Figures 4, 5, 6, and 7, since the control signals are sampled by VCLK, it is obvious that VCLK has to be enabled.



NOTE: Either the SSRT function is disabled (general control register bit 2 = 0), or the SFLAG/NFLAG input is held low if the SSRT function is enabled (general control register bit 2 = 1).

Figure 4. SCLK/VCLK Control Timing (SSRT Disabled, SCLK Frequency = VCLK Frequency)



NOTE:The SSRT function is enabled (general control register bit 2 = 1).

Figure 5. SCLK/VCLK Control Timing (SSRT Enabled, SCLK Frequency = VCLK Frequency)

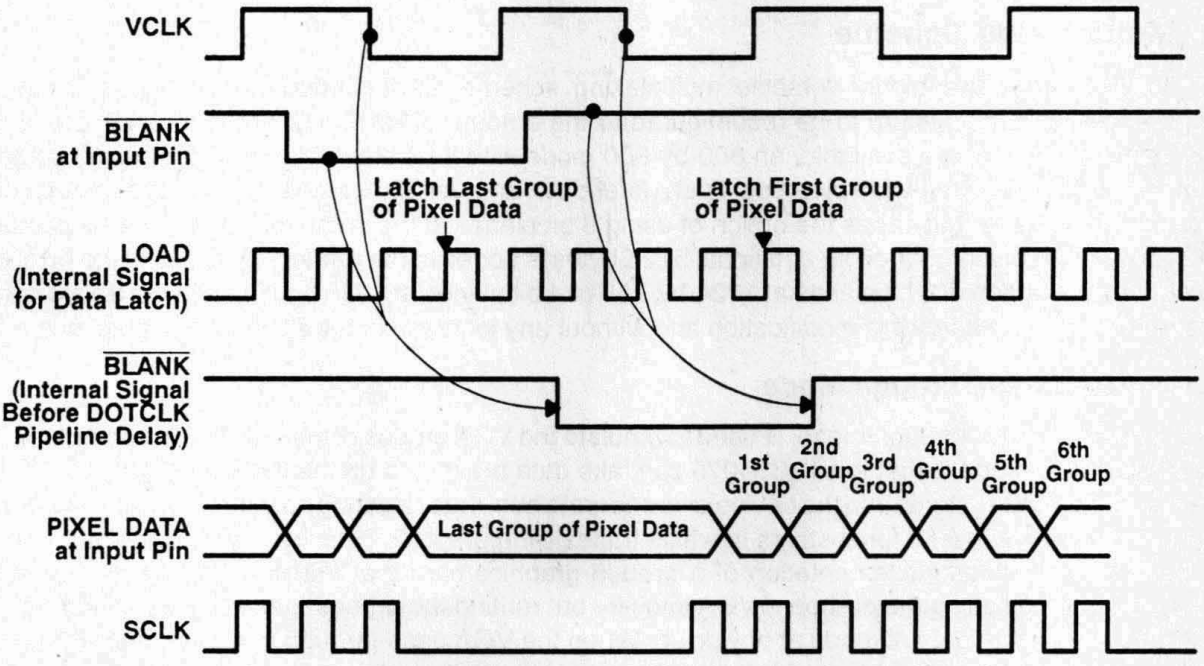


Figure 6. SCLK/VCLK Control Timing (SSRT Disabled, SCLK Frequency = 4 × VCLK Frequency)

NOTE: Either the SSRT function is disabled (general control register bit 2 = 0), or the SFLAG/NFLAG input is held low if the SSRT function is enabled (general control register bit 2 = 1).

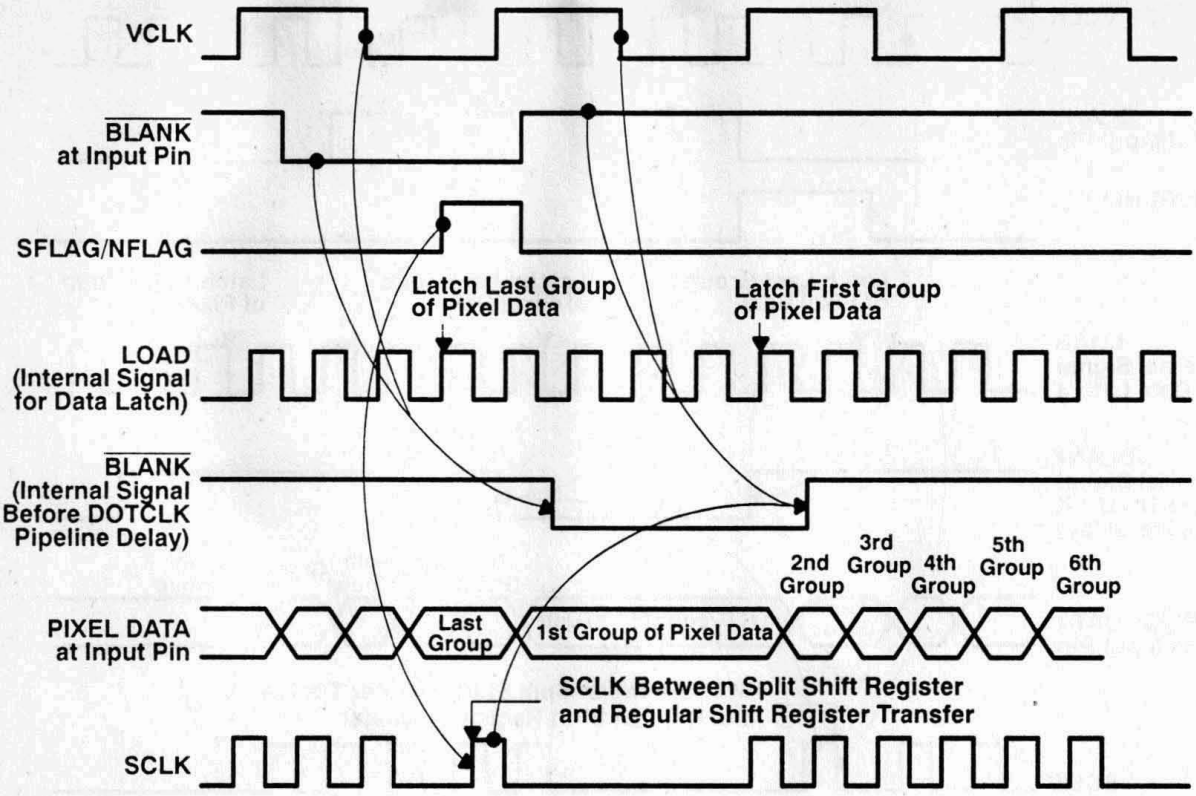


Figure 7. SCLK/VCLK Control Timing (SSRT Enabled, SCLK Frequency = 4 × VCLK Frequency)

2.4 Multiplexing Scheme

The TLC34075 offers a highly versatile multiplexing scheme as illustrated in Table 6. The on-chip multiplexing allows the system to be reconfigured to the amount of RAM available. For example, if only 256K bytes of memory are available, an 800-by-600 mode with 4 bit planes (four bits per pixel) could be implemented using an 8-bit-wide pixel bus. If, at a later date, another 256K bytes are added to another eight bits of the pixel bus, the user has the option of using 8 bit planes at the same resolution or 4 bit planes at a 1024-by-768 resolution. When an additional 512K bytes is added to the remaining 16 bits of the pixel bus, the user has the option of 8 bit planes at 1024-by-768 or 4 bit planes at 1280 by 1024. All the above can be achieved without any hardware modification and without any increase in the speed of the pixel bus.

2.4.1 VGA Pass-Through Mode

Mode 0, the VGA pass-through mode, is used to emulate the VGA modes of most personal computers. The advantage of this mode is that the TLC34075 can take data presented on the feature connectors of most VGA-compatible PC systems into the device on a separate bus, thus requiring no external multiplexing. This feature is particularly useful for systems in which the existing graphics circuitry is on the motherboard. In this instance, it enables implementation of a drop-in graphics card that maintains compatibility with all existing software by using the on-board VGA circuitry but routing the emerging bit-plane data through the TLC34075. This is the default mode at power-up. When the VGA pass-through mode is selected after the device is powered up, the clock selection register, the general control register, and the pixel read mask register are set to their default states automatically.

Since this mode is designed with the feature connector philosophy, all the timing is referenced to CLK0, which is used by default for VGA pass-through mode. For all the other normal modes, CLK <0:3> are the oscillator sources for DOTCLK, VCLK, and SCLK; all the data and control timing is referenced to SCLK.

2.4.2 Multiplexing Modes

In addition to the VGA pass-through mode, there are four multiplexing modes available, all of which are referred to as normal modes. In each normal mode, a pixel bus width of 8, 16, or 32 bits may be used. Modes 1, 2, and 3 also support a pixel bus width of 4 bits. Data should always be presented on the least significant bits of the pixel bus. For example, when a 16-bit-wide pixel bus is used and there are 8 bits per pixel, each 8-bit pixel should be presented on P<0:7>. All the unused pixel bus pins should be connected to GND.

Mode 1 uses a single bit plane to address the color palette. The pixel port bit is fed into bit 0 of the palette address, with the 7 high-order address bits being defined by the palette page register (see Section 2.2.3). This mode has uses in high-resolution monochrome applications such as desktop publishing. This mode allows the maximum amount of multiplexing (a 32:1 ratio), thus giving a pixel bus rate of only 4 MHz at a screen resolution of 1280 by 1024. Although only a single bit plane is used, alteration of the palette page register at the line frequency allows 256 different colors to be displayed simultaneously with 2 colors per line.

Mode 2 uses 2 bit planes to address the color palette. The 2 bits are fed into the low-order address bits of the palette with the 6 high-order address bits being defined by the palette page register (see Section 2.2.3). This mode allows a maximum divide ratio of 16:1 on the pixel bus and is a 4-color alternative to mode 1.

Mode 3 uses 4 bit planes to address the color palette. The 4 bits are fed into the low-order address bits of the palette with the 4 high-order address bits being defined by the palette page register (see Section 2.2.3). This mode provides 16 pages of 16 colors and can be used at SCLK divide ratios of 1 to 8.

Mode 4 uses 8 bit planes to address the color palette. Since all 8 bits of palette address are specified from the pixel port, the page register is not used. This mode allows dot-clock-to-SCLK ratios of 1:1 (8-bit bus), 2:1 (16-bit bus) or 4:1 (32-bit bus). Therefore, in a 32-bit configuration, a 1024-by-768 pixel screen can be implemented with an external data rate of only 16 MHz.

2.4.3 True Color Mode

Mode 5 is true color mode, in which 24 bits of data are transferred from the pixel port directly to the DACs with the same amount of pipeline delay as the overlay data and the control signals ($\overline{\text{BLANK}}$ and SYNCs). In this mode, overlay is provided by using the remaining 8 bits of the pixel bus to address the palette RAM, resulting in a 24-bit RAM output that is then used as overlay information to the DACs. When all the overlay inputs (P<0:7>) are at a low logic level or the pixel read mask register is loaded with the value 0, no overlay information is displayed; when a nonzero value is input with the pixel read mask enabled, the color palette RAM is addressed and the resulting data is then fed through to the DACs, receiving priority over the true color data.

The true-color-mode data input only works in the 8-bit mode. In other words, if only 6 bits are used, the 2 MSB inputs for each color should be tied to GND. However, the palette, which is used by the overlay input, is still governed by the 8/$\overline{6}$ input pin, and the output MUX selects 8 bits of data or 6 bits of data accordingly.

In the true color mode, P<15:8> pass red data, P<23:16> pass green data, and P<31:24> pass blue data.

2.4.4 Special Nibble Mode

Mode 6 is special nibble mode, which is enabled when the general control register SNM bit (bit 3) is set to 1 and the general control register SSRT bit (bit 2) is set to 0 (see Section 2.11). When special nibble mode is enabled, it takes precedence over the other modes, and the mux control register setup is ignored. The SFLAG/NFLAG input is then used as a nibble flag to indicate which nibble of each byte holds the pixel data. Special nibble mode is a variation of the 4-bit pixel mode with a 16-bit pixel width. All 32 inputs (P0 through P31) are connected as 4 bytes, but the 16-bit data bus is composed of either the lower or upper nibble of each of the 4 bytes. For more detailed information, refer to Section 2.9.2. Since this mode uses 4 bit planes for each pixel, they are fed into the low-order address bits of the palette, with the 4 high-order address bits being defined by the palette page register (see Section 2.2.3).

2.4.5 Multiplex Control Register

The multiplexer is controlled via the 8-bit multiplex control register. The bit fields of the register are in Table 6.

Table 6. Mode and Bus Width Selection

MODE	MUX CONTROL REGISTER BITS†						DATA BITS PER PIXEL‡	PIXEL BUS WIDTH	SCLK DIVIDE RATIO§	PIXEL LATCHING SEQUENCE¶
	5	4	3	2	1	0				
0#	1	0	1	1	0	1	8	8	1	1) VGA<7:0>
1	0	1	0	0	0	0	1	4	4	1) P<0> 2) P<1> 3) P<2> 4) P<3>
	0	1	0	0	0	1	1	8	8	1) P<0> 2) P<1> ⋮ 8) P<7>
	0	1	0	0	1	0	1	16	16	1) P<0> 2) P<1> ⋮ 16) P<15>
	0	1	0	0	1	1	1	32	32	1) P<0> 2) P<1> ⋮ 32) P<31>
2	0	1	0	1	0	0	2	4	2	1) P<1:0> 2) P<3:2>
	0	1	0	1	0	1	2	8	4	1) P<1:0> 2) P<3:2> 3) P<5:4> 4) P<7:6>
	0	1	0	1	1	0	2	16	8	1) P<1:0> 2) P<3:2> ⋮ 8) P<15:14>
	0	1	0	1	1	1	2	32	16	1) P<1:0> 2) P<3:2> ⋮ 16) P<31:30>
3	0	1	1	0	0	0	4	4	1	1) P<3:0>
	0	1	1	0	0	1	4	8	2	1) P<3:0> 2) P<7:4>
	0	1	1	0	1	0	4	16	4	1) P<3:0> 2) P<7:4> 3) P<11:8> 4) P<15:12>
	0	1	1	0	1	1	4	32	8	1) P<3:0> 2) P<7:4> ⋮ 8) P<31:28>

MODE	MUX CONTROL REGISTER BITS†						DATA BITS PER PIXEL‡	PIXEL BUS WIDTH	SCLK DIVIDE RATIO§	PIXEL LATCHING SEQUENCE¶
	5	4	3	2	1	0				
4	0	1	1	1	0	0	8	8	1	1) P<7:0>
	0	1	1	1	0	1	8	16	2	1) P<7:0> 2) P<15:8>
	0	1	1	1	1	0	8	32	4	1) P<7:0> 2) P<15:8> 3) P<23:16> 4) P<31:24>
5‖	0	0	1	1	0	1	24	32	1	1) P<31:8>
6	0	1	1	1	1	1	4	16	4	NFLAG = 0: 1) P<3:0> 2) P<11:8> 3) P<19:16> 4) P<27:24> NFLAG = 1: 1) P<7:4> 2) P<15:12> 3) P<23:20> 4) P<31:28>

† Bits 6 and 7 are *don't care* bits.

‡ This is the number of bits of pixel port (or VGA port in mode 1) information used as color data for each displayed pixel, often referred to as the number of bit planes. This may be color palette address data (Modes 0–4 and 6) or DAC data (mode 5).

§ The SCLK divide ratio is the number used for the output clock selection register. It indicates the number of pixels per bus load, or the number of pixels associated with each SCLK pulse. For example, with a 32-bit pixel bus width and 8 bit planes, 4 pixels comprise each bus load. The SCLK divide ratio is not automatically set by mode selection, but must be written to the output clock selection register.

¶ For each operating mode, the pixel latching sequence indicates the sequence in which pixel port or VGA port data are latched into the device. The latching sequence is initiated by a rising edge on SCLK. For modes in which multiple groups of data are latched, the SCLK rising edge latches all the groups, and the pixel clock shifts them out starting with the low-numbered group. For example, in mode 3 with a 16-bit pixel bus width, the rising edge of SCLK latches all the data groups, and the pixel clock shifts them out in the order P<3:0>, P<7:4>, P<11:8>, P<15:12>.

Mode 0 is VGA pass-through mode.

‖ Mode 5 is true color mode, in which 24 bits of color information are transferred directly from the pixel port to the DACs; overlay is implemented with the remaining 8 bits of the pixel bus. The distribution of pixel port data to the DACs is as follows: P<31:24> are passed to the blue DAC, P<23:16> are passed to the green DAC, and P<15:8> are passed to the red DAC. P<7:0> are used to generate overlay data; this operation can be disabled by either grounding P<7:0> or by clearing the read mask (see Section 1.4.5).

✡ Mode 6 is special nibble mode, the only mode in which the pixel bus width is not equal to the actual physical width, in bits, of the pixel bus. In this mode, the pixel bus is physically 32 bits wide; depending on the value of SFLAG/NFLAG, either the upper or lower nibble of each of the four physical bytes is selected to comprise the 16 bits of pixel data (equal to four 4-bit pixels).

NOTE: Although leaving unused pins floating will not adversely affect device operation, tying unused pins to ground lowers power consumption and, thus, is recommended.

As an example of how to use Table 6, suppose that the design goals specify a system with eight data bits per pixel and the lowest possible SCLK rate. Table 6 shows that, for non-VGA-pass-through operation, only mode 4 supports an eight-bit pixel depth. The lowest-possible SCLK rate within mode 4 is 1:4. This set of conditions is selected by writing the value 1Eh to the mux control register. The pixel latching sequence column shows that, in this mode, P<7:0> should be connected to the earliest-displayed pixel plane, followed by P<15:8>, P<23:16>, and then P<31:24> as the last displayed pixel plane. Assuming that VCLK is programmed as DOTCLK/4, Table 2–5 shows that the 1:4 SCLK ratio is selected by writing the value 12h to the output clock selection register. The special nibble mode should also be disabled (see Sections 2.9.2 and 2.11.2).

When the mux control register is loaded with 2Dh, the TLC34075 enters the VGA pass-through mode (the same condition as the default power-up mode). Please refer to Section 2.5.4 for more details.

2.4.6 Read Masking

The read mask register is used to enable or disable a pixel address bit from addressing the color palette RAM. Each palette address bit is logically ANDed with the corresponding bit from the read mask register before addressing the palette. This function is performed after the addition of the page register bits and, therefore, a zeroing of the read mask results in one unique palette location (location 0) and is not affected by the palette page register contents.

2.5 Reset

There are 3 ways to reset the TLC34075:

1. Power-on reset
2. Hardware reset
3. Software reset

2.5.1 Power-On Reset

The TLC34075 contains a power-on reset circuit. Once the voltage levels have stabilized following power-on reset, the device is in the VGA pass-through mode.

2.5.2 Hardware Reset

The TLC34075 resets whenever RS<3:0> = HHHH and a rising edge occurs on the $\overline{WR}$ input. The more rising $\overline{WR}$ edges occur, the more reliable the TLC34075 is reset. This scheme (bursting $\overline{WR}$ strobes until the power supply voltage stablizes) is suggested at power-up if a hardware reset approach is used.

The default reset condition is VGA pass-through mode, and the values for each register are shown in Section 2.5.4.

2.5.3 Software Reset

Whenever the mux control register is set for VGA pass-through mode after power-up, all registers are initialized accordingly. Since VGA pass-through mode is the default condition at power-up and hardware reset, the act of selecting the VGA pass-through mode through programming the mux control register is viewed as a software reset. Therefore, whenever mux control register bits <5:0> are set to 2Dh, the TLC34075 initiates a software reset.

2.5.4 VGA Pass-Through Mode Default Conditions

The value contained in each register after hardware or software reset is shown below:

Mux control register:	2Dh
Input clock selection register:	00h
Output clock selection register:	3Fh
Palette page register:	00h
General control register:	03h

Pixel read mask register:	FFh
Palette address register:	xxh
Palette holding register:	xxh
Test register:	(Pointing to color palette red value)

2.6 Frame Buffer Interface

The TLC34075 provides two clock signals for controlling the frame buffer interface: SCLK and VCLK. SCLK can be used to clock out data directly from the VRAM shift registers. Split shift register transfer functionality is also supported. VCLK is used to clock and synchronize control inputs like $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and $\overline{\text{BLANK}}$.

The pixel data presented at the inputs is latched at the rising edge of SCLK in normal mode or the rising edge of CLK0 in VGA pass-through mode. Control inputs $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and $\overline{\text{BLANK}}$ are sampled and latched at the falling edge of VCLK in normal mode, while $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and $\overline{\text{VGABLANK}}$ are latched at the rising edge of CLK0 in VGA pass-through mode. Both data and control signals are lined up at the DAC outputs to the monitors through the internal pipeline delay, so external glue logic is not required. The outputs of the DACs are capable of directly driving a 37.5-Ω load, as in the case of a doubly terminated 75-Ω cable. See Figures 9 and 10 for nominal output levels.

2.7 Analog Output Specifications

The DAC outputs are controlled by current sources (three for IOG and two each for IOR and IOB) as shown in Figure 8. In the normal case, there is a 7.5-IRE difference between blank and black levels, which is shown in Figure 9. If a 0-IRE pedestal is desired, it can be selected by resetting bit 4 of the general control register (see Section 2.11.3). The video output for a 0-IRE pedestal is shown in Figure 10.

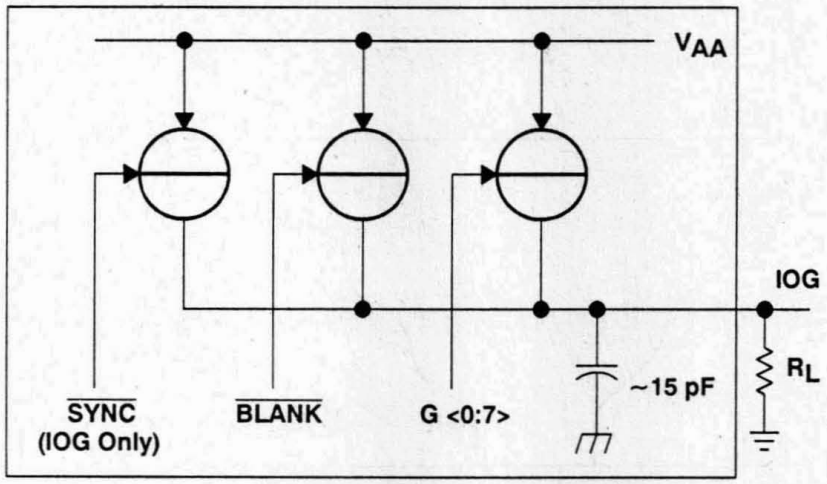


Figure 8. Equivalent Circuit of the IOG Current Output

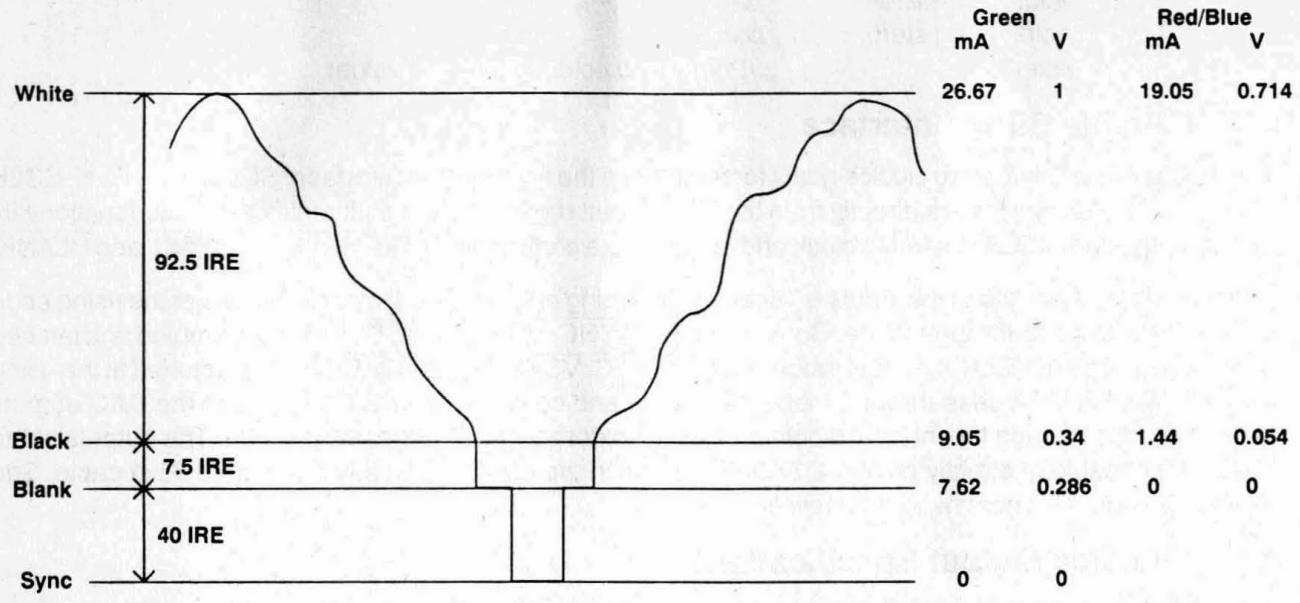


Figure 9. 7.5-IRE, 8-Bit Composite Video Output

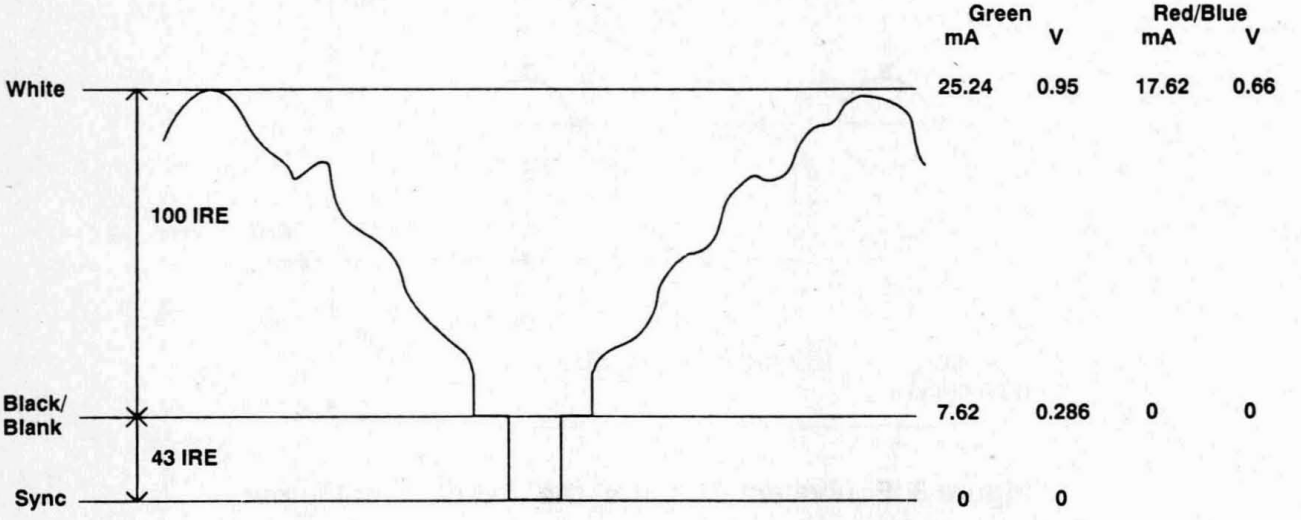


Figure 10. 0-IRE, 8-Bit Composite Video Output

NOTE: 75- Ω doubly terminated load. V_{REF} = 1.235 V, R_{SET} = 523 Ω. RS-343A levels and tolerances are assumed.

A resistor (R_{SET}) is needed to connect the FS ADJ pin to GND to control the magnitude of the full-scale video signal. The IRE relationships in Figures 9 and 10 are maintained regardless of the full-scale output current.

The relationship between R_{SET} and the full-scale output current IOG is:

$$R_{SET}\ (\Omega) = K1 \times V_{REF}\ (V) / IOG\ (mA)$$

The full-scale output current on IOR and IOB for a given R_{SET} is:

$$IOR, IOB\ (mA) = K2 \times V_{REF}\ (V) / R_{SET}\ (\Omega)$$

where K1 and K2 are defined as:

PEDESTAL	IOG		IOR, IOB	
	8-BIT OUTPUT	6-BIT OUTPUT	8-BIT OUTPUT	6-BIT OUTPUT
7.5-IRE	K1 = 11,294	K1 = 11,206	K2 = 8,067	K2 = 7,979
0-IRE	K1 = 10,684	K1 = 10,600	K2 = 7,462	K2 = 7,374

2.8 $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and $\overline{\text{BLANK}}$

For the normal modes, $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ are active-low pulses, and they are passed through true/complement gates to the HSYNCOUT and VSYNCOUT outputs. The output polarities of HSYNCOUT and VSYNCOUT can be programmed through the general control register. However, for the VGA pass-through mode, the polarities needed for monitors are already provided at the feature connector from which $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ are sourced, so the TLC34075 just passes $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ through to HSYNCOUT and VSYNCOUT without polarity change. As described in Section 2.3 and Figures 4 through 5, the $\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, and $\overline{\text{VSYNC}}$ inputs are sampled and latched on the falling edge of VCLK in the normal modes, and they are latched on the rising edge of the CLK0 input in the VGA pass-through mode. Refer to Figure 16 for the detailed timing.

The $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ inputs are used for both the VGA pass-through and normal modes. If the application uses both VGA pass-through and normal modes, an external multiplexer is needed to select $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ between VGA pass-through mode and normal mode. The $\overline{\text{MUXOUT}}$ signal is designed for this purpose (see Sections 2.10 and 2.11).

The $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and $\overline{\text{BLANK}}$ signals have internal pipeline delays to align the data at the outputs. Due to the sample and latch timing delay, it is possible to have active SCLK pulses after the $\overline{\text{BLANK}}$ input becomes active. The relationship between VCLK and SCLK and the internal VCLK sample and latch delay need to be carefully reviewed and programmed. See Section 2.3 and Figures 4 and 5 for more details.

As shown in Figure 18 for the IOG DAC output, active $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ signals turn off the sync current source (after the pipeline delay) independent of the $\overline{\text{BLANK}}$ signal level. In real applications, $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ should only be active (low) when $\overline{\text{BLANK}}$ is active (low).

To alter the polarity of the HSYNCOUT and VSYNCOUT outputs in the normal modes, the MPU must set or clear the corresponding bits in the general control register (see Section 2.11.1). Again, these two bits affect only the normal modes, not the VGA pass-through mode. These bits default to 1.

2.9 Split Shift Register Transfer VRAMs and Special Nibble Mode

2.9.1 Split Shift Register Transfer VRAMs

The TLC34075 directly supports split shift register transfer (SSRT) VRAMs. In order to allow the VRAMs to perform a split shift register transfer, an extra SCLK cycle must be inserted during the blank sequence. This is initiated when the SSRT enable bit (bit 2 in the general control register) is set to 1, the SNM bit (bit 3 in the general control register) is reset to 0 (see Section 2.11), and a rising edge on the SFLAG/NFLAG input pin is detected. An SCLK pulse is generated within 20 ns of the rising edge of the SFLAG/NFLAG signal. A minimum 15-ns high logic level duration is provided to satisfy all of the −15 VRAM requirements. By controlling the SFLAG/NFLAG rise time, the delay time from the rising edge of the VRAM TRG signal to SCLK can be satisfied. The relationship between the SCLK, SFLAG/NFLAG, and BLANK signals is as follows:

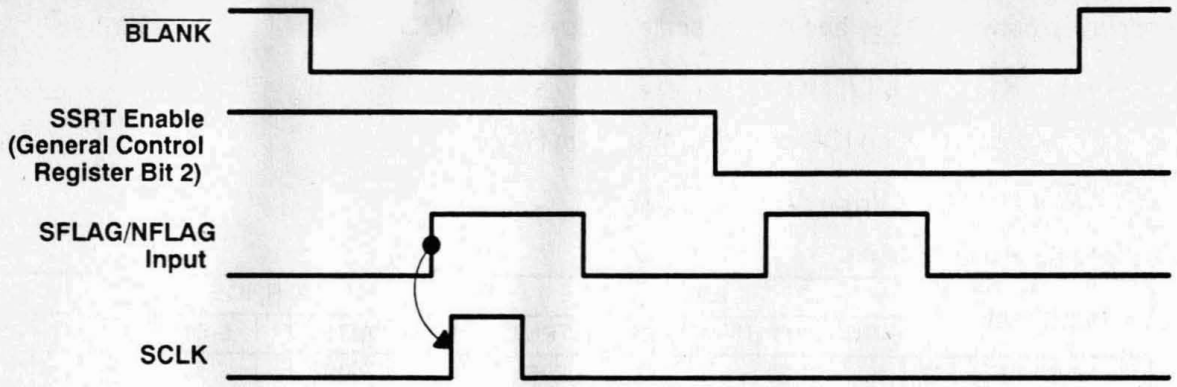


Figure 11. Relationship Between SFLAG/NFLAG, BLANK, and SCLK

If SFLAG/NFLAG is designed as an R-S latch set by split shift register transfer timing and reset by BLANK going high, the delay from BLANK high to SFLAG/NFLAG low cannot exceed one-half of one SCLK cycle; otherwise, the SCLK generation logic may fail.

If the SSRT function is enabled but SFLAG/NFLAG is held low, SCLK runs as if the SSRT function is disabled. The SFLAG/NFLAG input is not qualified by the BLANK signal and needs to be held low whenever an SSRT SCLK pulse is not desired. Refer to Section 2.3.1 and Figures 4 through 10 for more system details.

2.9.2 Special Nibble Mode

Special nibble mode is enabled when the SNM bit (bit 3 in the general control register) is set to 1 and the SSRT bit (bit 2 in the general control register) is reset to 0 (see Section 2.11). Special nibble mode provides a variation of the 4-bit pixel mode with a 16-bit bus width. While all 32 inputs (P<0:31>) are connected as 4 bytes, the 16-bit data bus is composed of the lower or upper nibble of each of the 4 bytes, depending on the level of the SFLAG/NFLAG input. The pixel data is distributed to 16-bit data bus as shown in Table 7.

Table 7. Pixel Data Distribution in Special Nibble Mode

SNM BIT = 1, SSRT BIT = 0	
SFLAG/NFLAG = 1	SFLAG/NFLAG = 0
P<7:4>	P<3:0>
P<15:12>	P<11:8>
P<23:20>	P<19:16>
P<31:28>	P<27:24>

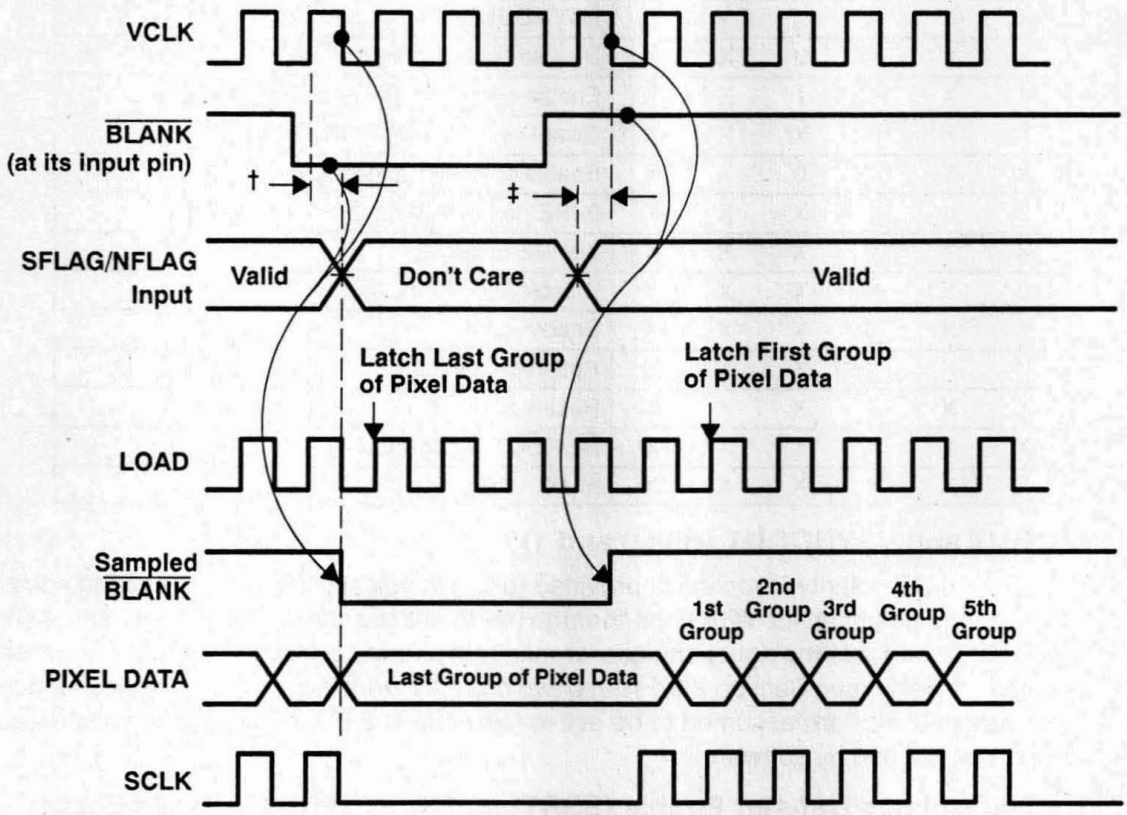
The SFLAG/NFLAG value is not latched by the TLC34075. Therefore, it should stay at the same level during the whole active display period, changing levels only during the BLANK signal active time. Refer to Figure 12, which is similar to Figure 4 except that the BLANK signal timing reference to SFLAG/NFLAG is explained. The SFLAG/NFLAG input has to meet the setup time and hold the data long enough to ensure that no pixel data is missed.

Special nibble mode operates at the line frequency when BLANK is active. However, the typical application of this mode is double frame buffers with pixel data width of 4 bits. While one frame buffer is being displayed on the monitor, the other frame buffer can be used to accept new picture information. SFLAG/NFLAG is used to indicate which frame buffer is being displayed.

SNM and SSRT must be mutually exclusive. Unpredictable operation occurs if both the SNM and SSRT bits are set to 1. The mux control register should be set up as shown in Table 6 (see Section 2.4.5). However, the SNM bit takes precedence over the other mux control register selections. In other words, if the mux control register is set up for another mode but special nibble mode is still enabled in the general control register, the input multiplex circuit takes whatever SCLK divide ratio the mux control register specifies and performs the nibble operation, causing operational failure.

During special nibble mode, the input mux circuit latches all 8-bit inputs but only passes on the specified nibble. The specified nibble is stored in the 4 LSBs of the next register pipe after the input latch, and the 4 MSBs are zeroed in that register. The register pipe contents are then passed to the read mask block. With this structure, the palette page register still functions normally, providing good flexibility to users.

If the general control register bit 3 = 0 and bit 2 = 0, both split shift register transfers and special nibble mode are disabled and the SFLAG/NFLAG input is ignored.



† **CAUTION:**
If the data is not held valid until SCLK and BLANK both go low, the last few pixels could be missed.

‡ **Setup time to next VCLK falling edge after BLANK high (must be met, otherwise the first pixel data could be missed).**

Figure 12. SFLAG/NFLAG Timing in Special Nibble Mode

2.10 MUXOUT Output

MUXOUT is a TTL-compatible output. It is software programmable and is used to control external devices. Its typical application is to select the HSYNC and VSYNC inputs between the VGA pass-through mode and the normal modes (see Section 2.8). This output is driven low at power-up or when VGA pass-through mode is selected; at any other time it can be programmed to the desired polarity via general control register bit 7.

2.11 General Control Register

The general control register is used to control HSYNC and VSYNC polarity, split shift register transfer enabling, special nibble mode, sync control, the ones accumulation clock source, and the VGA pass-through indicator. The bit field definitions are as follows:

Table 8. General Control Register Bit Functions

GENERAL CONTROL REGISTER BIT								FUNCTION
7	6	5	4	3	2	1	0	
X	X	X	X	X	X	X	0	HSYNCOUT is active-low
X	X	X	X	X	X	X	1	HSYNCOUT is active-high (default)
X	X	X	X	X	X	0	X	VSYNCOUT is active-low
X	X	X	X	X	X	1	X	VSYNCOUT is active-high (default)
X	X	X	X	X	0	X	X	Disable split shift register transfer (default)
X	X	X	X	0	1	X	X	Enable split shift register transfer
X	X	X	X	0	X	X	X	Disable special nibble mode (default)
X	X	X	X	1	0	X	X	Enable special nibble mode
X	X	X	0	X	X	X	X	0-IRE pedestal (default)
X	X	X	1	X	X	X	X	7.5-IRE pedestal
X	X	0	X	X	X	X	X	Disable sync (default)
X	X	1	X	X	X	X	X	Enable sync
X	0	X	X	X	X	X	X	Reserved (default)
X	1	X	X	X	X	X	X	Reserved
0	X	X	X	X	X	X	X	$\overline{\text{MUXOUT}}$ is low (default)
1	X	X	X	X	X	X	X	$\overline{\text{MUXOUT}}$ is high

2.11.1 HSYNCOUT and VSYNCOUT (Bits 0 and 1)

HSYNCOUT and VSYNCOUT polarity inversion is provided to allow indication to monitors of the current screen resolution. Since the polarities for VGA pass-through mode are provided at the feature connector, the inputs to the TLC34075 will have the right polarities for monitors already, so the TLC34075 just passes them through with pipeline delay (see Section 2.8). These two bits only work in the normal modes, and the input horizontal and vertical syncs are assumed to be active-low incoming pulses. These two bits default to the value 1 but can be changed by software.

2.11.2 Split Shift Register Transfer Enable (SSRT) and Special Nibble Mode Enable (SNM) (Bits 2 and 3)

See Section 2.9.

2.11.3 Pedestal Enable Control (Bit 4)

This bit specifies whether a 0- or 7.5-IRE blanking pedestal is to be generated on the video outputs. Having a 0-IRE blanking pedestal means that the black and blank levels are the same.

0: 0-IRE pedestal (default)
1: 7.5-IRE pedestal

2.11.4 Sync Enable Control (Bit 5)

This bit specifies whether or not SYNC information is to be output onto IOG.

0: Disable sync (default)
1: Enable sync

2.11.5 $\overline{\text{MUXOUT}}$ (Bit 7)

The MUXOUT bit indicates to external circuitry that the device is running in VGA pass-through mode. This bit does not affect the operation of the device (see Section 2.10).

0: $\overline{\text{MUXOUT}}$ is low (default in VGA pass-through mode)
1: $\overline{\text{MUXOUT}}$ is high

2.12 Test Register

There are three test functions provided in the TLC34075, and they are all controlled and monitored through the test register. They are data flow check, DAC analog test, and screen integrity test.

The test register has two ports: one for a control word, accessed by writing to the register location, and one for the data word, accessed by reading from the register location. Depending on the channel written in the control word, the data read presents the information for that channel.

The control word is three bits long and occupies D<2:0>. It specifies which of the eight channels to inspect. The following table and state machine diagrams show how each channel is addressed:

Table 9. Test Mode Selection

D2	D1	D0	CHANNEL
0	0	0	Color palette red value
0	0	1	Color palette green value
0	1	0	Color palette blue value
0	1	1	Identification code
1	0	0	Ones accumulation red value
1	0	1	Ones accumulation green value
1	1	0	Ones accumulation blue value
1	1	1	Analog test

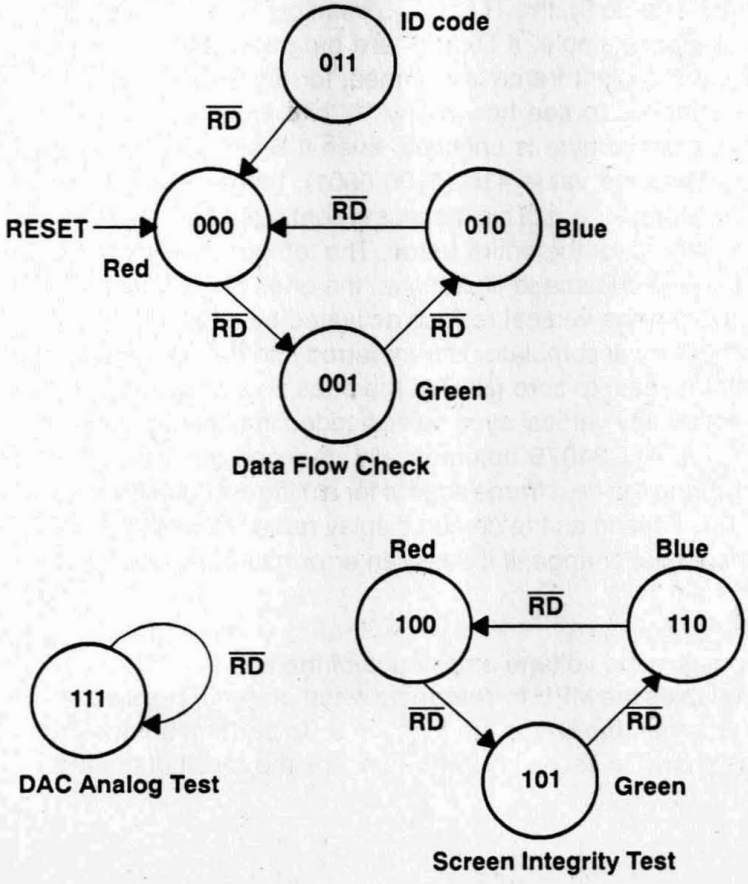


Figure 13. Test Register Control Word State Diagrams

2.12.1 Frame Buffer Data Flow Test

The TLC34075 provides a means to check all the data entering the DAC (but before the output multiplexer 8/$\overline{6}$ shift). When accessing these color channels, the data entering the DACs should be kept constant for the entire MPU read cycle. This can be done either by slowing down the dot clock or ensuring that the data is constant for a sufficiently long series of pixels. The value read is the one stored in the color palette RAM location pointed to by the input multiplexer. The read operation causes a post-increment to point to the next color channel, and the post-increment of blue wraps back to red as shown in the preceeding state diagram. For example, if D<2:0> is written as 001, then three succsessive reads are performed, the values read out are green, blue, and red in that sequence.

2.12.2 Identification Code

The ID code can be used for identification of different software versions. The ID code in the TLC34075 is static and may be read without consideration of the dot clock or video signals. To be user-friendly, the read postincrement also applies to the ID register, but once it falls into the color channel, it will not come back pointing to the ID unless the value 011 is written to D<2:0> again. So, if the test register is written as 011 in D<2:0>, then six successive reads are performed, the first value read is the ID and the last value read is green. The ID value defined here is 75h.

2.12.3 Ones Accumulation Screen Integrity Test

A technique called ones accumulation can be used to detect errors in fixed (not animated) screen displays. This type of error detection is useful for system checkout and field diagnostics.

Each of the 256 24-bit words in the TLC34075 internal color palette RAM is composed of three bytes, one each for the red, green, and blue components of the word. When D<2:0> are programmed with the appropriate binary value (see Table 9), the TLC34075 monitors the corresponding color byte that is output by the color palette RAM. For example, if D<2:0> are programmed with the value 100, the TLC34075 monitors the red byte. As the current frame is scanned, for each color palette RAM word accessed, the designated color byte is checked to see how many "1" bits it contains, and this number is added to a temporary accumulator (the entire byte is checked, even if 6-bit mode is selected). For example, if the designated color byte contains the value 41h (0100 0001), then the value 2 is added to the temporary accumulator, as 41h contains two "1" bits. This process is continued until an entire frame has been scanned; the same color byte is monitored for the entire frame. The temporary accumulator truncates any overflow above the value 255. Due to circuit speed limitations, the ones accumulation is calculated at a speed of (DOTCLK frequency)/2. During the vertical retrace activated by a falling edge on the TLC34075 $\overline{\text{VSYNC}}$ input, the value in the temporary accumulator is transferred into the ones accumulation register, and then the temporary accumulator is reset to zero (NOTE: the ones accumulation register is updated only on the falling edge of $\overline{\text{VSYNC}}$, not by any vertical sync pulses coded into the composite video signal). Before the next frame scan begins, the TLC34075 automatically changes the value in D<2:0> so that the ones accumulation performed during the next frame scan is for a different color byte (see the screen integrity test state diagram of Figure 13). As long as the screen display remains fixed, the ones accumulation value for a particular color byte should not change; if it does, an error has occurred.

2.12.4 Analog Test

Analog test is used to compare the voltage amplitudes of the analog RGB outputs to each other and to a 145-mV reference. This enables the MPU to determine whether the CRT monitor is connected to the analog RGB outputs or not and whether the DACs are functional. To perform an analog test, D<2:0> must be set to 111; D<7:4> are set as shown in Table 11. D<3> contains the result of the analog test.

Table 10. Test Register Bit Definitions for Analog Test

BIT DEFINITION	READ/WRITE
D7: Red select	R/W
D6: Green select	R/W
D5: Blue select	R/W
D4: 145-mV reference select	R/W
D3: Result	R

Table 11. D<7:4> Bit Coding for Analog Comparisons

D<7:4>	OPERATION	IF D3 = 1	IF D3 = 0
0000	Normal operation	Don't care	Don't care
1010	Red DAC compared to blue DAC	Red > blue	Red < blue
1001	Red DAC compared to 145-mV reference	Red > 145 mV	Red < 145 mV
0110	Green DAC compared to blue DAC	Green > blue	Green < blue
0101	Green DAC compared to 145-mV reference	Green > 145 mV	Green < 145 mV

NOTE: All the outputs have to be terminated to compare the voltage.

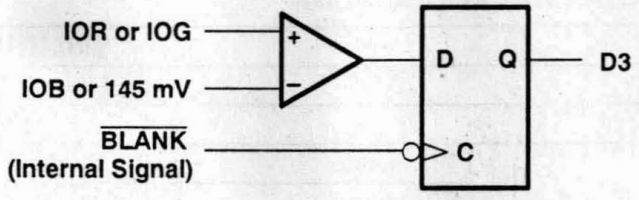


Figure 14. Internal Comparator Circuitry for Analog Test

The result of the analog comparison is strobed into D3 at the falling edge of an internal signal derived from the input $\overline{\text{BLANK}}$ signal. In order to have stable inputs to the comparator, the DAC should be set to a constant level between syncs. For normal operation, data flow check, and screen integrity test, D<7:4> must be set to zero.

3 Specifications

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 7 V
Input voltage range, V_I . . . . . −0.5 V to V_{DD} + 0.5 V
Analog output short-circuit duration to any power supply or common . . . . . unlimited
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Junction temperature . . . . . 175°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminal.

3.2 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.75	5	5.25	V
V_{REF}	Reference voltage		1.2	1.235	1.26	V
V_{IH}	High-level input voltage	TTL inputs	2.4		V_{DD} + 0.5	V
		ECL inputs	V_{DD} − 1		V_{DD} + 0.5	
V_{IL}	Low-level input voltage	TTL inputs			0.8	V
		ECL inputs	−0.5		V_{DD} − 1.6	
Output load resistance, R_L				37.5		Ω
FS ADJUST resistor, R_{SET}				523		Ω
Operating free-air temperature			0		70	°C

3.3 Electrical Characteristics

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = –800 μA	2.4			V
V_{OL}	Low-level output voltage	D<0:7>, $\overline{\text{MUXOUT}}$, VCLK	I_{OL} = 3.2 mA			0.4	V
		HSYNCOUT, VSYNCOUT	I_{OL} = 15 mA			0.4	
		SCLK	I_{OL} = 18 mA			0.4	
I_{IH}	High-level input current	TTL inputs	V_I = 2.4 V			1	μA
		ECL inputs	V_I = 4 V			1	
I_{IL}	Low-level input current	TTL inputs	V_I = 0.8 V			–1	μA
		ECL inputs	V_I = 0.4 V			–1	
I_{DD}	Supply current, pseudo-color mode	TLC34075-66	See Note 2			350	mA
		TLC34075-85				375	
		TLC34075-110				400	
		TLC34075-135				470	
I_{DD}	Supply current, true color mode	TLC34075-66				450	
		TLC34075-85				450	
		TLC34075-110				450	
		TLC34075-135				450	
I_{OZ}	High-impedance-state output currrent					10	μA
C_i	Input capacitance	TTL inputs	f = 1 MHz, V_I = 2.4 V		4		pF
		ECL inputs	f = 1 MHz, V_I = 4 V		4		

† All typical values are at V_{DD} = 5 V, T_A = 25°C.

NOTE 2: I_{DD} is measured with DOTCLK running at the maximum specified frequency, SCLK frequency = DOTCLK frequency/4, and the palette RAM loaded with full-range toggling patterns (00h/00h/FFh/FFh/00h/00h/FFh/FFh/ . . .). Pseudo-color mode is also known as color indexing mode.

3.4 Operating Characteristics

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution (each DAC)	8/$\overline{6}$ high		8		bits
		8/$\overline{6}$ low		6		
E_L	End-point linearity error (each DAC)	8/$\overline{6}$ high			1	LSB
		8/$\overline{6}$ low			1/4	
E_D	Differential linearity error (each DAC)	8/$\overline{6}$ high			1	LSB
		8/$\overline{6}$ low			1/4	
	Gray scale error				5%	
	Output current	White level relative to blank	17.69	19.05	20.4	mA
		White level relative to black (7.5 IRE only)	16.74	17.62	18.5	
		Black level relative to blank (7.5 IRE only)	0.95	1.44	1.9	
		Blank level on IOR, IOB	0	5	50	μA
		Blank level on IOG (with SYNC enabled)	6.29	7.6	8.96	mA
		Sync level on IOG (with SYNC enabled)	0	5	50	μA
		One LSB (8/$\overline{6}$ high)		69.1		μA
		One LSB (8/$\overline{6}$ low)		276.4		
	DAC-to-DAC matching			2%	5%	
	DAC-to-DAC crosstalk			–20		dB
V_{OC}	Output compliance		–1		1.2	V
	Output impedance			50		kΩ
	Output capacitance	f = 1 MHz, I_{OUT} = 0		13		pF
	Clock and data feedthrough			–20		dB
	Glitch impulse (see Note 2)			50		pV-s
	Pipeline delay	Normal mode	1 SCLK + 9 DOTCLK			periods
		VGA pass-through mode	7.5 DOTCLK			

NOTE 2: Glitch impulse does not include clock and data feedthrough. The –3-dB test bandwidth is twice the clock rate.

3.5 Timing Requirements

PARAMETER			TLC34075-66		TLC34075-85		TLC34075-110		TLC34075-135		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	DOTCLK frequency			66		85		110		135	MHz
	CLK0 frequency for VGA pass-through mode			66		85		85		85	MHz
t_{cyc}	Clock cycle time	TTL	15.2		11.8		9.1		7.4		ns
		ECL	15.2		11.8		9.1		7.4		
t_{su1}	Setup time, RS<0:3> valid before $\overline{RD}$ or $\overline{WR}$ ↓		10		10		10		10		ns
t_{h1}	Hold time, RS<0:3> valid after $\overline{RD}$ or $\overline{WR}$ ↓		10		10		10		10		ns
t_{su2}	Setup time, D<0:7> valid before $\overline{WR}$ ↑		35		35		35		35		ns
t_{h2}	Hold time, D<0:7> valid after $\overline{WR}$ ↑		0		0		0		0		ns
t_{su3}	Setup time, VGA<0:7> and $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{VGABLANK}$ valid before CLK0 ↑		2		2		2		2		ns
t_{h3}	Hold time, VGA<0:7> and $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{VGABLANK}$ valid after CLK0 ↑		2		2		2		2		ns
t_{su4}	Setup time, P<0:31> valid before SCLK ↑		2		2		2		0		ns
t_{h4}	Hold time, P<0:31> valid after SCLK ↑		5		5		5		5		ns
t_{su5}	Setup time, $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{BLANK}$ valid before VCLK ↓		5		5		5		5		ns
t_{h5}	Hold time, $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{BLANK}$ valid after VCLK ↓		2		2		2		2		ns
t_{w1}	Pulse duration, $\overline{RD}$ or $\overline{WR}$ low		50		50		50		50		ns
t_{w2}	Pulse duration, $\overline{RD}$ or $\overline{WR}$ high		30		30		30		30		ns
t_{w3}	Pulse duration, clock high	TTL	4.5		4		3.5		3		ns
		ECL	5.5		4		3.5		3		
t_{w4}	Pulse duration, clock low	TTL	4.5		4		3.5		3		ns
		ECL	5.5		4		3.5		3		
t_{w5}	Pulse duration, SFLAG/NFLAG high (see Note 4)		30		30		30		30		ns

NOTES: 3. TTL input signals are 0 to 3 V with less than 3 ns rise/fall time between the 10% and 90% levels unless otherwise specified. ECL input signals are $V_{DD}-1.8$ V to $V_{DD}-0.8$ V with less than 2 ns rise/fall time between the 20% and 80% levels. For input and output signals, timing reference points are at the 10% and 90% signal levels. Analog output loads are less than 10 pF. D<0:7> output loads are less than 50 pF. All other output loads are less than 50 pF unless otherwise specified.

4. This parameter applies when the split shift register transfer (SSRT) function is enabled. See Section 2.9.1 for details.

3.6 Switching Characteristics

TL34075-66, TLC34075-85

PARAMETER		TLC34075-66			TLC34075-85			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
	SCLK frequency (see Note 5)			66			85	MHz
	VCLK frequency			66			85	MHz
t_{en1}	Enable time, $\overline{RD}$ low to D<0:7> valid			40			40	ns
t_{dis1}	Disable time, $\overline{RD}$ high to D<0:7> disabled			17			17	ns
t_{v1}	Valid time, D<0:7> valid after $\overline{RD}$ high	5			5			ns
t_{PLH1}	Propagation delay, SFLAG/NFLAG ↑ to SCLK high (see Note 6)	0		20	0		20	ns
t_{d1}	Delay time, $\overline{RD}$ low to D<0:7> starting to turn on	5			5			ns
t_{d2}	Delay time, selected input clock high/low to DOTCLK (internal signal) high/low		7			7		ns
t_{d3}	Delay time, DOTCLK high/low to VCLK high/low		6			6		ns
t_{d4}	Delay time, VCLK high/low to SCLK high/low	0		5	0		5	ns
t_{d5}	Delay time, DOTCLK high/low to SCLK high/low		8			8		ns
t_{d6}	Delay time, DOTCLK high to IOR/IOG/IOB active (analog output delay time) (see Note 7)		20			20		ns
t_{d7}	Analog output settling time (see Note 8)			8			8	ns
t_{d8}	Delay time, DOTCLK high to HSYNCOUT and VSYNCOUT valid		5			5		ns
t_{w6}	Pulse duration, SCLK high (see Note 6)	15		55	15		55	ns
t_r	Analog output rise time (see Note 9)		2			2		ns
	Analog output skew	0		2	0		2	ns

NOTES: 5. SCLK can drive an output capacitive load up to 60 pF. The worst-case transition time between the 10% and 90% levels is less than 4 ns.

6. This parameter applies when the split shift register transfer (SSRT) function is enabled. See Section 2.9.1 for details.
7. Measured from the 90% point of the rising edge of DOTCLK to 50% of the full-scale transition.
8. Measured from the 50% point of the full-scale transition to the point at which the output has settled, within ± 1 LSB (settling time does not include clock and data feedthrough).
9. Measured between 10% and 90% of the full-scale transition.

3.6 Switching Characteristics (Cont'd.)

TL34075-110, TLC34075-135

PARAMETER		TLC34075-110			TLC34075-135			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
	SCLK frequency (see Note 10)			85			85	MHz
	VCLK frequency			85			85	MHz
t_{en1}	Enable time, $\overline{RD}$ low to D<0:7> valid			40			40	ns
t_{dis1}	Disable time, $\overline{RD}$ high to D<0:7> disabled			17			17	ns
t_{v1}	Valid time, D<0:7> valid after $\overline{RD}$ high	5			5			ns
t_{PLH1}	Propagation delay, SFLAG/NFLAG ↑ to SCLK high (see Note 11)	0		20	0		20	ns
t_{d1}	Delay time, $\overline{RD}$ low to D<0:7> starting to turn on	5			5			ns
t_{d2}	Delay time, selected input clock high/low to DOTCLK (internal signal) high/low		7			7		ns
t_{d3}	Delay time, DOTCLK high/low to VCLK high/low		6			6		ns
t_{d4}	Delay time, VCLK high/low to SCLK high/low	0		5	0		5	ns
t_{d5}	Delay time, DOTCLK high/low to SCLK high/low		8			8		ns
t_{d6}	Delay time, DOTCLK high to IOR/IOG/IOB active (analog output delay time) (see Note 12)		20			20		ns
t_{d7}	Analog output settling time (see Note 13)			6			6	ns
t_{d8}	Delay time, DOTCLK high to HSYNCOUT and VSYNCOUT valid		3			3		ns
t_{w6}	Pulse duration, SCLK high (see Note 11)	15		55	15		55	ns
t_r	Analog output rise time (see Note 14)		2			2		ns
	Analog output skew	0		2	0		2	ns

NOTES: 10. SCLK can drive an output capacitive load up to 60 pF. The worst-case transition time between the 10% and 90% levels is less than 4 ns.

11. This parameter applies when the split shift register transfer (SSRT) function is enabled. See Section 2.9.1 for details.

12. Measured from the 90% point of the rising edge of DOTCLK to 50% of the full-scale transition.

13. Measured from the 50% point of the full-scale transition to the point at which the output has settled, within ± 1 LSB (settling time does not include clock and data feedthrough).

14. Measured between 10% and 90% of the full-scale transition.

3.7 Timing Diagrams

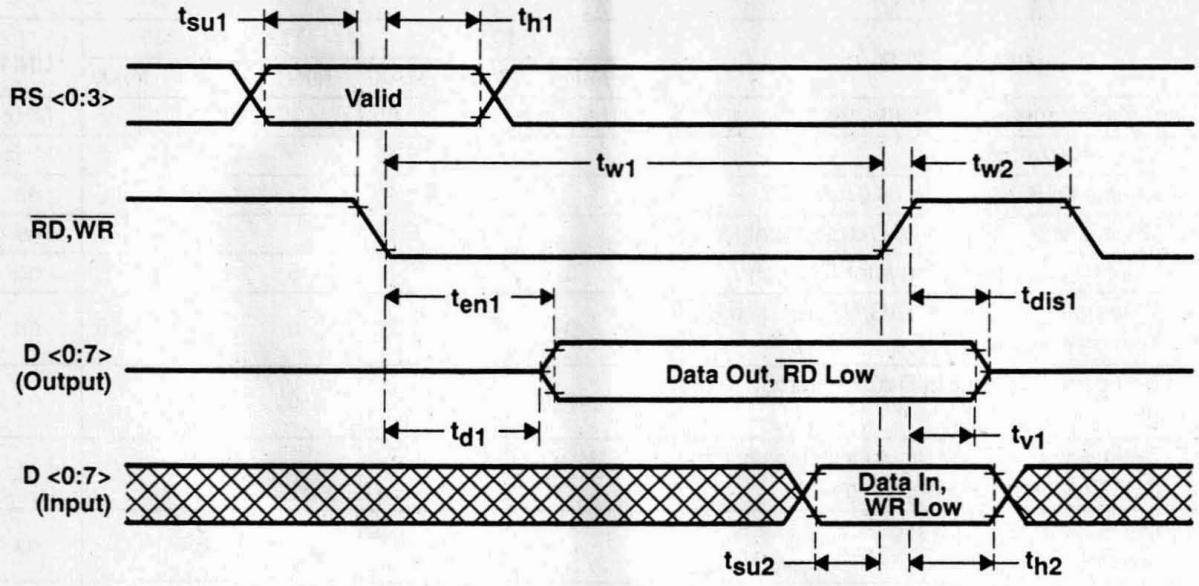


Figure 15. MPU Interface Timing

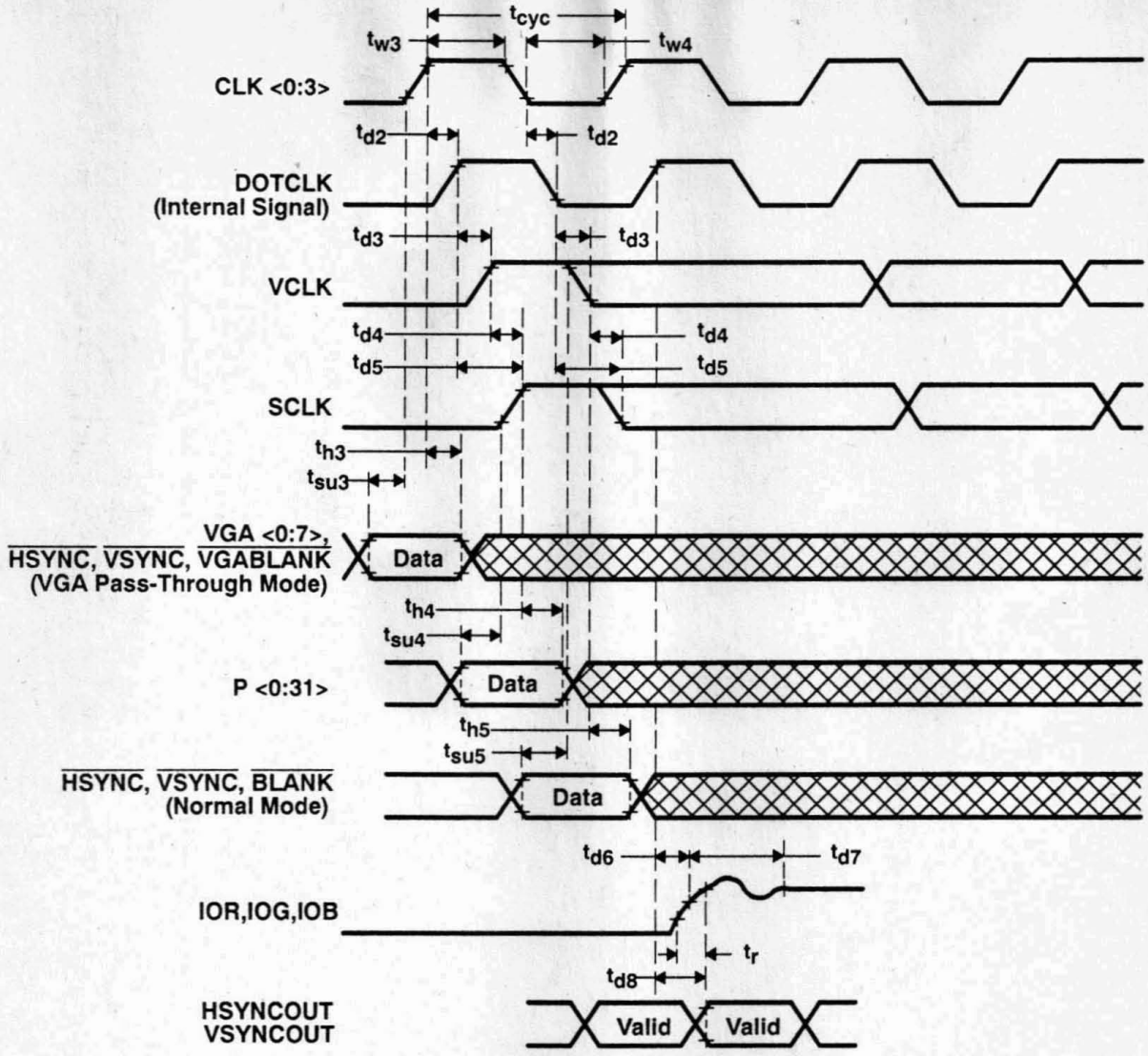


Figure 16. Video Input/Output

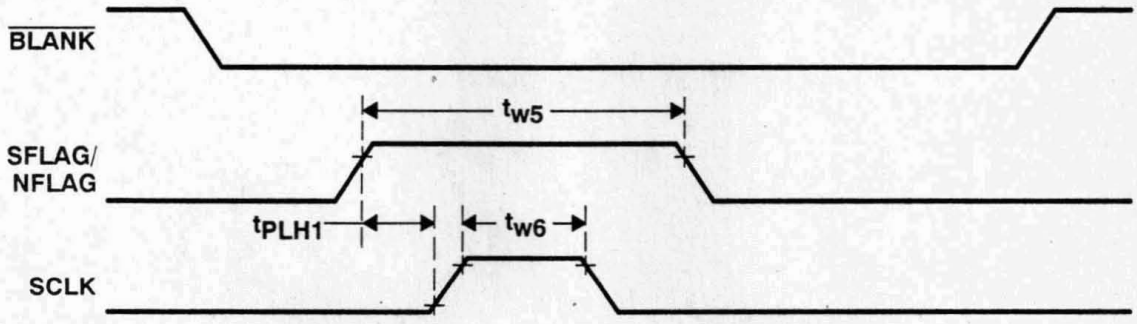


Figure 17. SFLAG/NFLAG Timing (When SSRT Function is Enabled)

Appendix A
SCLK/VCLK and the TMS340x0

While the TLC34075 SCLK and VCLK outputs are designed for compatibility with all graphics systems, they are also tightly coupled with the TMS340x0 Graphics System Processors. All the timing requirements of the TMS340x0 have been considered. However, there are a few points that need to be explained with regard to applications.

VCLK

All the video control signals in the TMS340x0 (i.e., $\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, and $\overline{\text{VSYNC}}$) are triggered and generated from the falling edge of VCLK. The fact that the TLC34075 uses the falling edge to sample and latch the $\overline{\text{BLANK}}$ input gives users maximum freedom to choose the frequency of VCLK and interconnect the TLC34075 with the TMS340x0 GSP without glue logic. Needless to say, the VCLK frequency needs to be selected to be compatible with the minimum VCLK period required by the TMS340x0.

In the TMS340x0, the same VCLK falling edge that generates $\overline{\text{BLANK}}$ requests a screen refresh. If the VCLK period is longer than 16 TQs (TQ is the period of the TMS340x0 CLKIN), it is possible that the last SCLK pulse could be used falsely to transfer the VRAM data from memory to the shift register along with the last pixel transfer. The first SCLK pulse for the next scan line would then shift the first pixel data out of the pipe and the screen would then falsely start from the second pixel.

SCLK and SFLAG

The TLC34075 SCLK signal is compatible with current -10 and slower VRAMs. When split shift register transfers are used, one SCLK pulse has to be generated between the regular shift register transfer and the split shift register transfer to ensure correct operation. The SFLAG input is designed for this purpose. SFLAG can be generated from a programmable logic array and triggered by the rising edge of the $\overline{\text{TR}}/\overline{\text{QE}}$ signal or the rising edge of the $\overline{\text{RAS}}$ signal of the regular shift register transfer cycle. $\overline{\text{TR}}/\overline{\text{QE}}$ can be used if the minimum delay from when the VRAM's $\overline{\text{TRG}}$ signal goes high to SCLK going high can be met by the programmable logic array delay; otherwise, $\overline{\text{RAS}}$ can be used.

Appendix B
PC Board Layout Considerations

PC Board Considerations

A four-layer PC board should be used with the TLC34075: one layer each for 5-V power and GND and two layers for signals. The layout should be optimized for the lowest-possible noise on the TLC34075 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{DD} and GND pins should be minimized so as to reduce inductive ringing. The terminal assignments for the TLC34075 P<0:31> inputs were selected for minimum interconnect lengths between these inputs and the VRAM pixel data outputs. The TLC34075 should be located as close to the output connectors as possible to minimize noise pickup and reflections due to impedance mismatching.

Ground Plane

A single ground plane is recommended for both the TLC34075 and the rest of the logic. Separate digital and analog ground planes are not needed.

Power Plane

Split power planes are recommended for the TLC34075 and the rest of the logic. The TLC34075 and its associated analog circuitry should have their own power plane (referred to as A_{VCC} in Figure 18). The two power planes should be connected at a single point through a ferrite bead as shown in Figures 18, 19, and 20. This bead should be located within three inches of the TLC34075.

Supply Decoupling

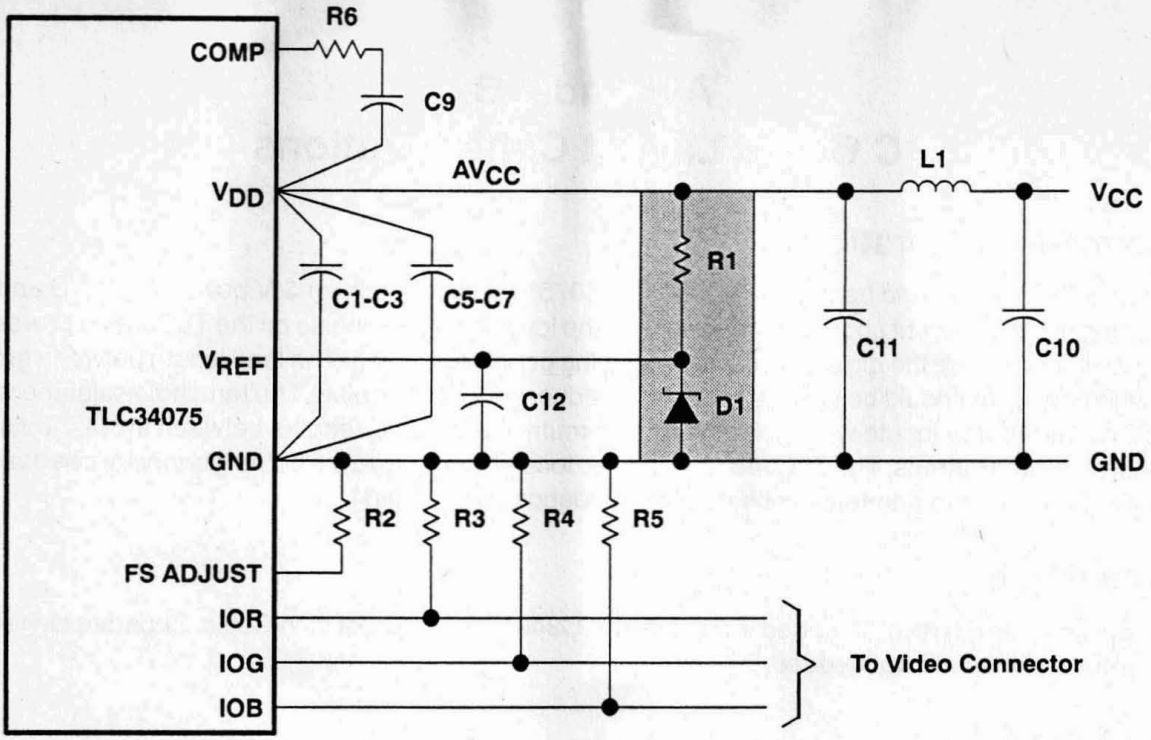
Bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

For the best performance, a 0.1-μF ceramic capacitor in parallel with a 0.01-μF chip capacitor should be used to decouple each of the three groups of power pins to GND. These capacitors should be placed as close as possible to the device as shown in Figure 19.

If a switching power supply is used, the designer should pay close attention to reducing power supply noise and should consider using a three-terminal voltage regulator for supplying power to A_{VCC}.

COMP and V_{REF} Terminals

A 100-Ω resistor and 0.1-μF ceramic capacitor (approximate values) should be connected in series between the device's COMP and V_{DD} terminals in order to avoid noise and color-smearing problems. Also, whether an internal or external voltage reference is used, a 0.1-μF capacitor should be connected between the device's V_{REF} and GND terminals to further stabilize the video image. These resistor and capacitor values may vary depending on the board layout; experimentation may be required in order to determine optimum values.



LOCATION	DESCRIPTION
C1-C3, C9-C10, C12	0.1-μF ceramic capacitor
C5-C7	0.01-μF ceramic chip capacitor
C11	33-μF tantalum capacitor
L1	ferrite bead
R1	1000-Ω 1% metal-film resistor
R2	523-Ω 1% metal-film resistor
R3, R4, R5	75-Ω 1% metal-film resistor
R6	100-Ω 5% resistor
D1	1.2-V voltage reference

Figure 18. Typical Connection Diagram and Components (Shaded Area is Optional)

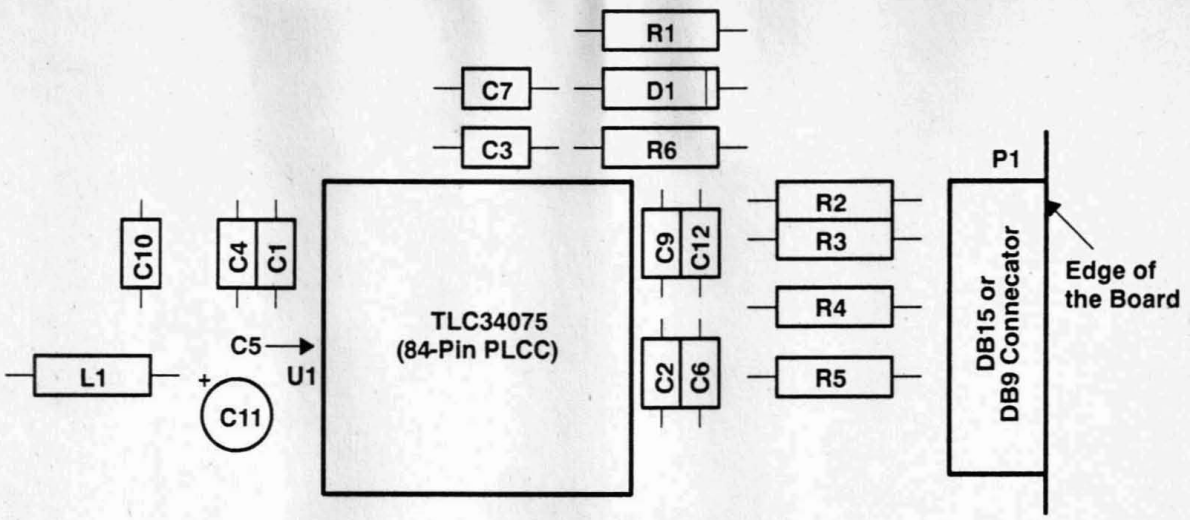


Figure 19. Typical Component Placement (Component Side)

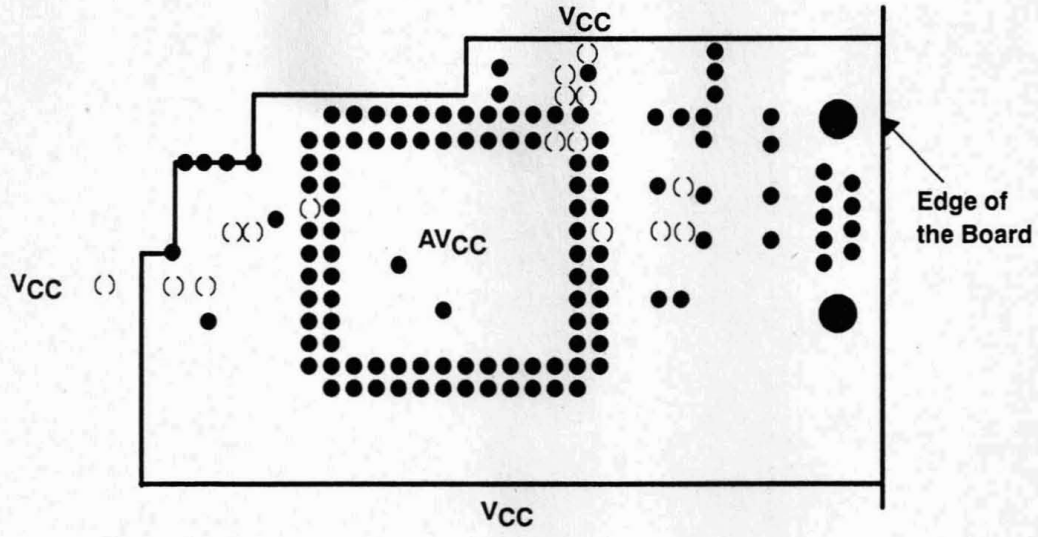


Figure 20. Typical Split Power Plane (Solder Side)

Appendix C
SCLK Frequency > VCLK Frequency

The VCLK and SCLK outputs generated by the TLC34075 are both free-running clocks. The video control signals (i.e., $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and $\overline{\text{BLANK}}$) are normally generated from VCLK, and a fixed relationship between the video control signals and VCLK can therefore be expected. The TLC34075 samples and latches the $\overline{\text{BLANK}}$ input on the falling edge of VCLK. It then looks at the LOAD signal to determine when to disable or enable SCLK at its output terminal. The decision is deterministic when the SCLK frequency is greater than or equal to the VCLK frequency. However, when the SCLK frequency is less than the VCLK frequency, the appearance of the SCLK waveform at its output terminal when $\overline{\text{BLANK}}$ is sampled low on the VCLK falling edge can vary (see Figures C–1 and C–2).

To avoid this variation in the SCLK output waveform, the SCLK and VCLK frequencies should be chosen so that HTOTAL is evenly divisible by the ratio of (VCLK frequency:SCLK frequency); that is,

$$\text{remainder of } \left[\frac{\text{HTOTAL}}{\left(\frac{\text{VCLK frequency}}{\text{SCLK frequency}} \right)} \right] = 0.$$

For example, if HTOTAL is even, VCLK frequency = DOTCLK frequency/8, and SCLK frequency = DOTCLK frequency/16, then the formula above is satisfied. NOTE: When HTOTAL starts at zero (as in the TMS340x0 GSP), then the formula becomes

$$\text{remainder of } \left[\frac{(\text{HTOTAL} + 1)}{\left(\frac{\text{VCLK frequency}}{\text{SCLK frequency}} \right)} \right] = 0.$$

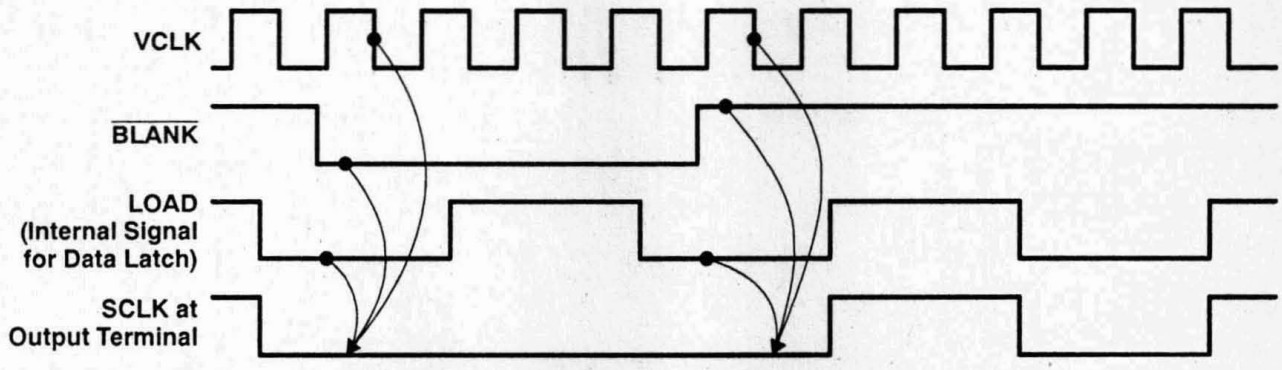


Figure 21. VCLK and SCLK Phase Relationship (Case 1)

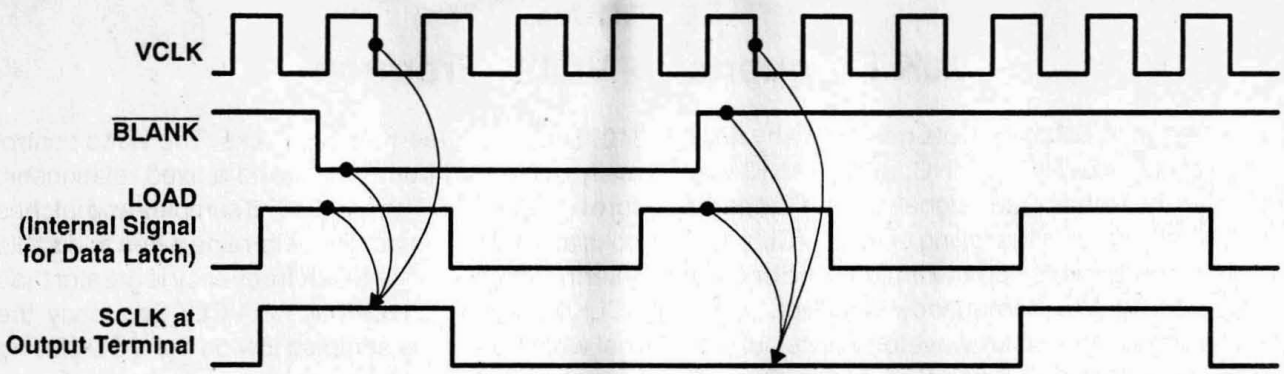


Figure 22. VCLK and SCLK Phase Relationship (Case 2)

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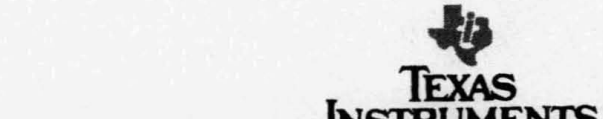

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1 Introduction

The TLC32040 and TLC32041 analog interface circuits are designed to provide a high level of system integration and performance. The analog interface circuits combine high resolution A/D and D/A converters, programmable filters, digital control and timing circuits as well as programmable input amplifiers and multiplexers. Emphasis is placed on making the interface to digital signal processors (the TMS320 family) and most microprocessors as simple as possible. This application report describes the software and circuits necessary to interface to numerous members of the TMS320 family. It presents three circuits for interfacing the TLC32040 Analog Interface Circuit to the TMS320 family of digital signal processors. Details of the hardware and software necessary for these interfaces are provided.

To facilitate the discussion of the software the following definitions and naming conventions are used:

1. >nnnn – a number represented in hexadecimal.
2. Interrupt service routine – a subroutine called in direct response to a processor interrupt.
3. Interrupt subroutine – any routine called by the interrupt service routine.
4. Application program (application routine) – the user's application dependent software (e.g., digital filtering routines, signal generation routines, etc.)

2 TLC32040 Interface to the TMS32010/E15

2.1 Hardware

Because the TLC32040 (Analog Interface Circuit) is a serial-I/O device, the interface to the TMS32010, which has no serial port, requires a small amount of glue-logic. The circuit shown in Figure 1 accomplishes the serial-to-parallel conversion for the AIC operating in synchronous mode.

2.1.1 Parts List

The interface circuit for the TMS32010 uses the following standard logic circuits:

1. One SN74LS138 3-to-8-line address decoder
2. One SN74LS02 Quad NOR-Gate
3. One SN74LS00 Quad NAND-Gate
4. One SN74LS04 Hex Inverter
5. One SN74LS74 Dual D-Flip-Flop
6. Two SN74LS299 8-bit Shift Registers

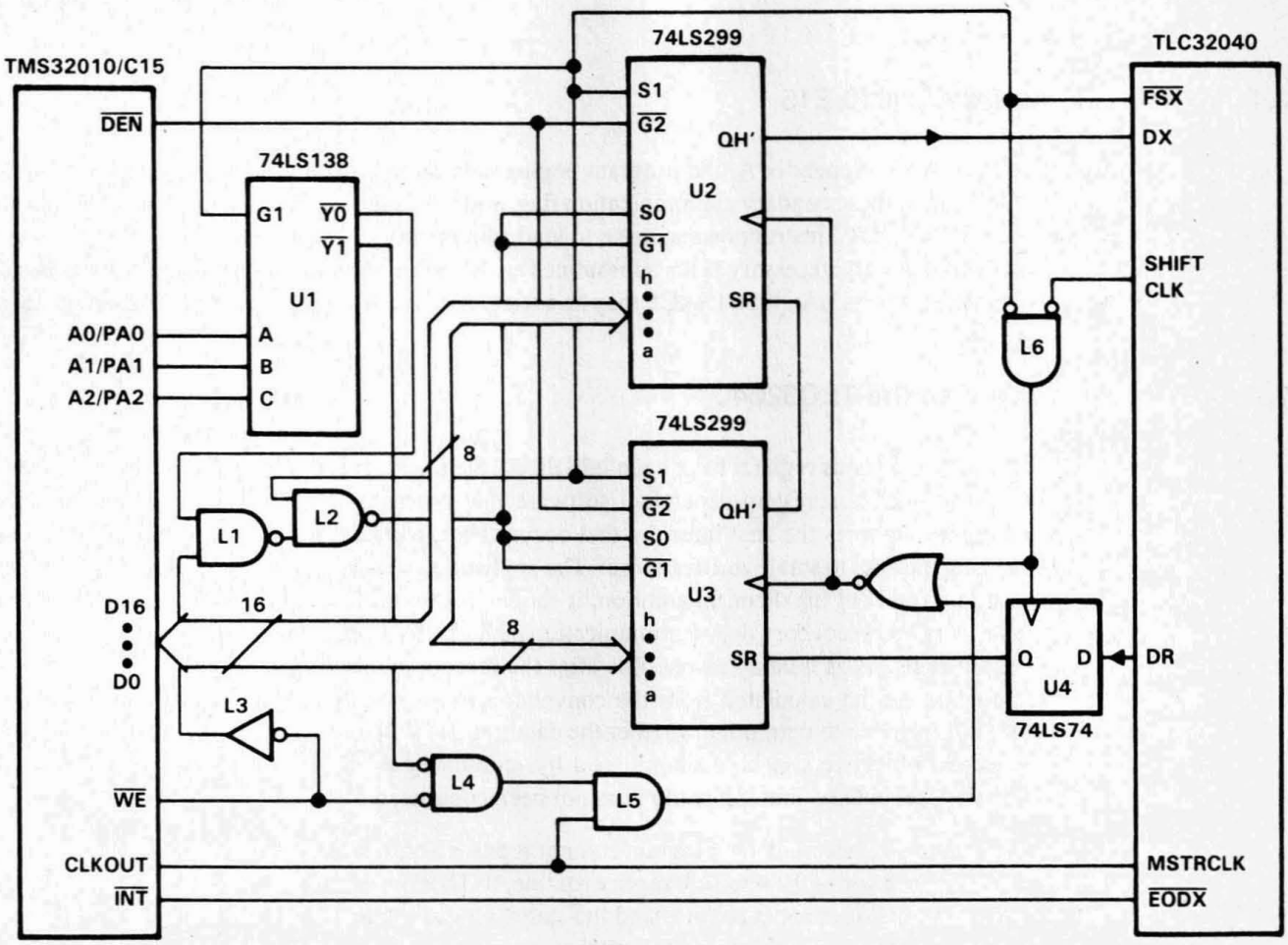


Figure 1. AIC Interface to TMS32010/E15

2.1.2 Hardware Description

The SN74LS138 is used to decode the addresses of the ports to which the TLC32040 and the interface logic have been mapped. If no other ports are needed in the development system, this device may be eliminated and the address lines of the TMS32010 used directly in place of $\overline{Y1}$ and $\overline{Y0}$ (see Figure 1).

Since the interface circuits are only addressed when the TMS32010 executes an IN or an OUT instruction, gates L1, L2, L3, L4, and L5 are required to enable reading and writing to the shift registers only on these instructions. The TBLW instruction is prohibited because it has the same timing as the OUT instruction. Flip-flop U4 ensures that the setup and hold times of SN74LS299 shift registers are met.

Although not shown in the circuit diagram, it is recommended that the $\overline{CLR}$ pins of the SN74LS299 shift registers as well as the $\overline{RESET}$ pin of the AIC be tied to the power-up reset circuit shown in the AIC data sheet. This ensures that the registers are clear when the AIC begins to transfer data and decrease the possibility that the AIC will shift in bad data which could cause the AIC to shut down or behave in an unexpected manner.

2.2 Software

The flowcharts for the communication program along with the TMS32010 program listing are presented in Appendix A. If this software is to be used, and application program that moves data into and out of the transmit and receive registers must be supplied.

2.2.1 Initializing the TMS320010/E15

As shown in the flowcharts in Appendix A, the program begins with an initialization routine which clears both the transmit/receive-end flag and the secondary communication flag, and stores the addresses of the interrupt subroutines. The program uses the MPYK..PAC instruction sequence to load data memory locations with the 12-bit address of the subroutines. This sequence is only necessary if the subroutines are to reside in program memory locations larger than >00FF. Otherwise, the instructions LACK and SACL may be used to initialize the subroutine-address storage locations.

2.2.2 Communicating with the TLC32040

After the storage registers and status register have been initialized, the interrupt is enabled and control is passed to the user's application routine (i.e., the system-dependent software that processes received data and prepares data for transmission). The program ignores the first interrupt that occurs after interrupts are enabled (page 10–28, line 207, IGINT routine), allowing the AIC to stabilize after a reset. The application routine should not write to the shift registers while data is moving into (and out of) them. In addition, it should ensure that no primary data is written to the shift registers between a primary and secondary data-communication pair. The first objecive can be accomplished by writing to the SN74LS299 shift registers as quickly as possible after the receive interrupt. The number of instruction cycles between the data transfers can be calculated from the conversion frequency. By counting instruction cycles in the application program, it is possible to determine whether the data transfer will conflict with the OUT instruction to the shift register. The second objective can be accomplished by monitoring SNDFLG in the application program. If SNDFLG is true (>00FF), secondary communication has not been completed.

When the processosr receives an interrupt, the program counter is pushed onto the hardware stack and then the program counter is set to > 0002, the location of the interrupt service routine, INTSVC (page 10–25, line 46). The interrupt service routine then saves the contents of the accumulator and the status register and calls the interrupt subroutine to which XVECT points. If secondary communication is to follow the upcoming primary communication, XVECT, is set by the application program to refer to SINT1, otherwise, XVECT defaults to NINT (i.e., the normal interrupt routine).

Because the interrupt subroutine makes one subroutine call and uses two levels of the hardware stack, the application program can only use two levels of nesting (i.e., if stack extension is not used). This means that any subroutine called by the application program can only call subroutines containing no instructions that use the hardware stack (e.g., TBLW) and that make no other subroutine calls. In addition, if the application program and communication program are being implemented on an XDS series emulator, the emulator consumes one level of the hardware stack and allows the application program only one level of nesting (i.e., one level of subroutine calls).

As shown in the flowcharts in Appendix A, the normal interrupt routine reads the A/D data from the shift registers and then sets the receive/transmit end-flag (RXEFLG). The application program must write the outgoing D/A data word to the shift registers at a time convenient to the application routine. It should have the restriction that the data be written before the next data transfer.

2.2.3 TLC32040 Secondary Communication

If it is necessary to write to the control register of the AIC or configure any of the AIC internal counters, the application program must initiate a primary/secondary communication pair. This can be accomplished by placing a data word in which bits 0 and 1 are both high into DXMT, placing the secondary control word (see program listing page 10–25) in D2ND, and placing the address of the secondary communication subroutine, SINT1, in XVECT. When the next interrupt occurs, the interrupt subroutine will call routine SINT1. SINT1 reads the A/D information from the shift registers and writes the secondary communication word to the shift registers.

3 TLC32040 Interface to the TMS32020

3.1 Hardware Description

Because the TLC32040 is designed specifically to interface with the serial port of the TMS32020/C25, the interface requires no external hardware. Except for CLKR and CLKX, there is a one-to-one correspondence between the serial port control and data pins of TMS32020 and TLC32040. CLKR and CLKX are tied together since both the transmit and the receive operations are synchronized with SHIFT CLK of the TLC32040. The interface circuit, along with the communication program (page 10–33), allows the AIC to communicate with the TMS32020/C25 in both synchronous and asynchronous modes. See Figures 2, 3, and 4.

3.2 Software

The program listed in Appendix B allows the AIC to communicate with the TMS32020 in synchronous or asynchronous mode. Although originally written for the TMS32020, it will work just as well for the TMS320C25.

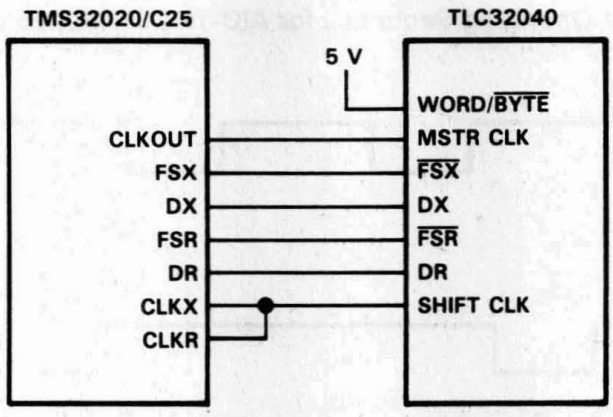
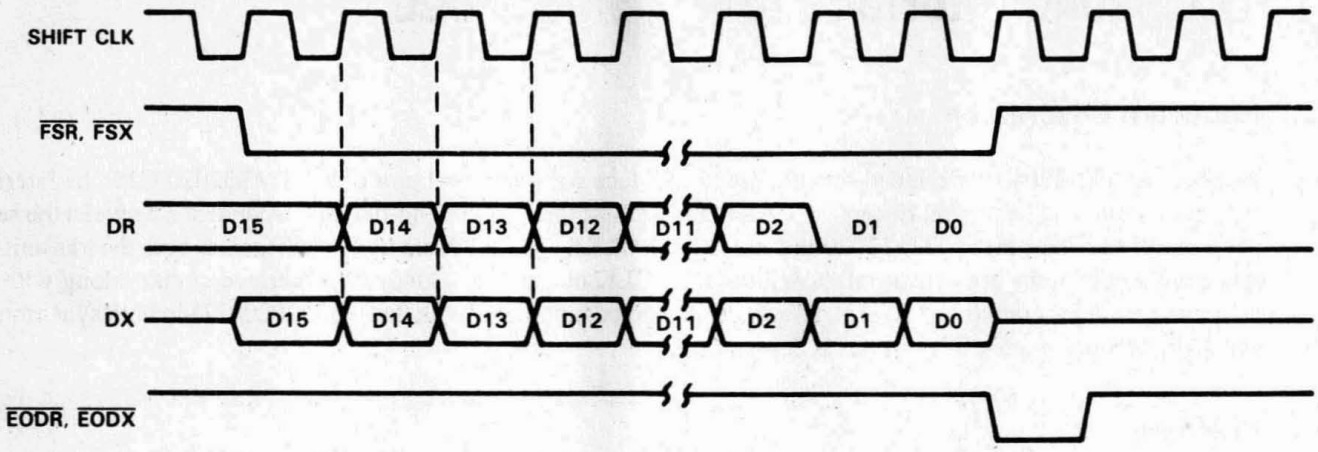


Figure 2. AIC Interface to TMS32020/C25



The sequence of operation is:

1. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought low.
2. One 16-bit word is transmitted or one 16-bit byte is received.
3. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought high.
4. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pin emits a low-going pulse as shown.

Figure 3. Operating Sequence for AIC-TMC32020/C25 Interface

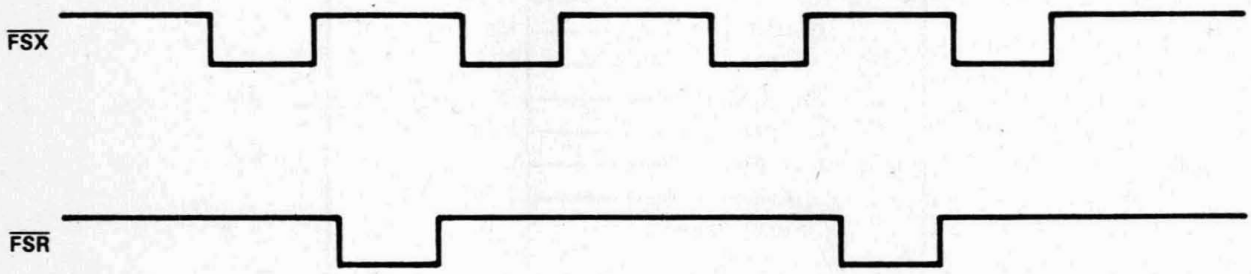


Figure 4. Asynchronous Communication AIC-TMS32020/C25 Interface

3.2.1 Initializing the TMS32020/C25

This program starts by calling the initialization routine. The working storage registers for the communication program and the transmit and receive registers of the DSP are cleared, and the status registers and interrupt mask register of the TMS32020/C25 are set (see program flow charts in Appendix B). The addresses of the transmit and receive interrupt subroutines are placed in their storage locations, and the addresses of the routines which ignore the first transmit and receive interrupts are placed in the transmit and receive subroutine pointers (XVECT and RVECT). The TMS32020/C25 serial port is configured to allow transmission of 16-bit data words (FO), the serial port format bit of the TMS32020/C25 must be set to zero) with an externally generated frame synchronization ($\overline{\text{FSX}}$ and $\overline{\text{FXR}}$ arae inputs, TXM bit is set to 0).

3.2.2 Communicating with the TLC32040

After the TMS32020/C25 has been initialized, interrupts are enabled and the program calls subroutine IGR. The processor is instructed to wait for the first transmit and receive interrupts (XINT and RINT) and ignore them. After the TMS32020 has received both a receive and a transmit interrupt, the IGR routine will transfer control back to the main program and IGR will not be called again.

If the transmit interrupt is enabled, the processor branches to location 28 in program memory at the end of a serial transmission. This is the location of the transmit interrupt service routine. The program context is saved by storing the status registers and the contents of the accumulator. Then the interrupt service routine calls the interrupt subroutine whose address is stored in the transmit interrupt pointer (XVECT).

A similar procedure occurs on completion of a serial receive. If the receive interrupt is enabled, the processor branches to location 26 in program memory. As with the transmit interrupt service routine (XINT, page 10–36, line 226), the receive interrupt service routine (page 10–36, line 194) saves context and then calls the interrupt subroutine whose address is stored in the receive interrupt pointer (RVECT). It is important that during the execution of either the receive or transmit interrupt service routines, all interrupts are disabled and must be re-enabled when the interrupt service routine ends.

The main program is the application program. Procedures such as digital filtering, tone-generation and detection, and secondary communication judgment can be placed in the application program. In the program listing shown in Appendix B, a subroutine (C2ND) is provided which will prepare for secondary communication. If secondary communication is required, the user must first write the data with the secondary code to the DXMT register. This data word should have the two least significant bits set high (e.g., >0003). The first 14 bits transmitted will go to the D/A converter and the last two bits indicate to the AIC that secondary communication will follow. After writing to the SXMT register, the secondary communication word should be written to the D2ND register.

This data may be used to program the AIC internal counters or to reconfigure the AIC (e.g., to change from synchronous to asynchronous mode or to bypass the bandpass filter). After both data words are stored in their respective registers, the application program can then call the subroutine C2ND which will prepare the TMS32020 to transmit the secondary communication word immediately after primary communication.

3.2.3 Secondary Communicating – Special Considerations

This communication program disables the receive interrupt (RINT) when secondary communication is requested. Because of the critical timing between the primary and secondary communication words and because RINT carries a higher priority than the transmit interrupt, the receive interrupt cannot be allowed to interrupt the processor before the secondary data word can be written to the data-transmit register. If this situation were to occur, the AIC would not receive the correct secondary control word and the AIC could be shut down.

In many applications, the AIC internal registers need only be set at the beginning of operation, (i.e., just after initialization). Thereafter, the DSP only communicates with the AIC using primary Communication. In cases such as these, the communication program can be greatly simplified.

4 Interfacing the TMS32040 to the TMS320C17

4.1 Hardware Description

As shown in Figure 5, the TMS320C17 interfaces directly with the TLC32040. However, because the TMSs320C17 responds more slowly to interrupts than the TMS32010/E15 or the TMS32020/C25, additional circuit connections are necessary to ensure that the TMS320C17 can respond to the interrupt, accomplish the context-switching that is required when an interrupt is serviced, and proceed with the interrupt vector. This must all be accomplished within the strict timing requirements imposed by the TLC32040. To meet these requirements, $\overline{\text{FSX}}$ of the TLC32040 is connected to the $\overline{\text{EXINT}}$ pin of the TMS320C17. This allows the TMS320C17 to recognize the transmit interrupt before the transmission is complete. This allows the interrupt service routine to complete its context-switching while the data is being transferred. The interrupt service routine branches to the interrupt subroutines only after the FSX flag bit has been set. This signals the end of data transmission.

The other hardware modification involves connecting the $\overline{\text{EODX}}$ pin of the TLC32040 to the $\overline{\text{BIO}}$ pin of the TMS320C17. Because the TMS320C17 serial port accepts data in 8-bit bytes (see Figure 6) and the TLC32040 controls the byte sequence (i.e., which byte is transmitted first, the high-order byte or the low-order byte) it is important that the TMS320C17 be able to distinguish between the two transmitted bytes. The $\overline{\text{EODX}}$ signal is asserted only once during each transmission pair, making it useful for marking the end of a transmission pair and synchronizing the TMS320C17 with the AIC byte sequence. After synchronism has been established, the $\overline{\text{BIO}}$ line is no longer needed by the interface program and may be used elsewhere.

Because he TMS320C17 serial port operates only in byte mode, 16-bit transmit data should be separated into two 8-bit bytes and stored in separate registers before a transmit interrupt is acknowledged. Alternatively, the data can be prepared inside the interrupt service routine before the interrupt subroutine is called. From the time that the interrupt is recognized to the end of the data transmission is equivalent to 28 TMS320C17 instruction cycles.

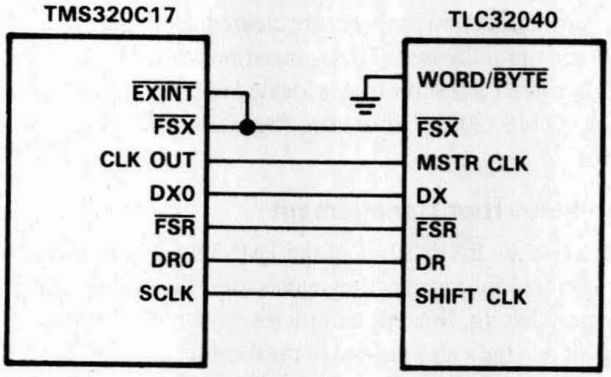
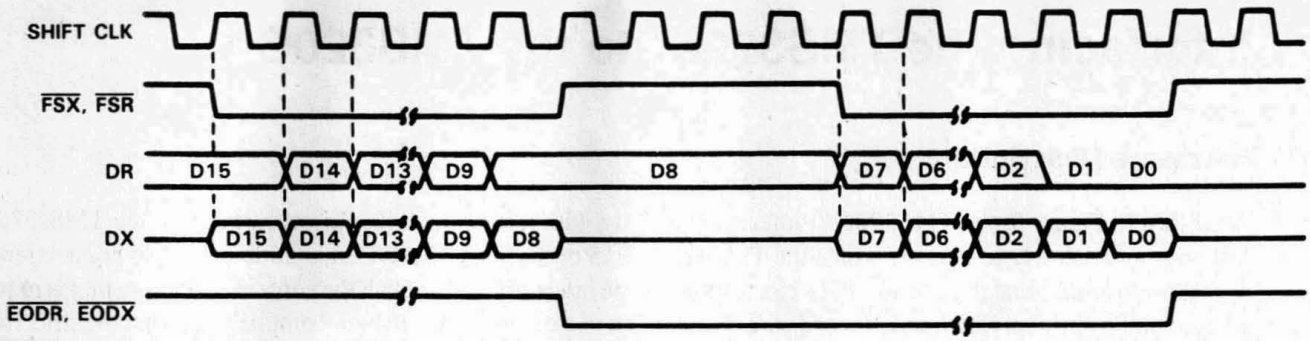


Figure 5. AIC Interface to TMS320C17



The sequence of operation is:

1. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought low.
2. One 8-bit word is transmitted or one 8-bit byte is received.
3. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pins are brought low.
4. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ emit a positive frame-sync pulse that is four shift clock cycles wide.
5. One 8-bit byte is transmitted and one 8-bit byte is received.
6. The $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ pins are brought high.
7. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought high

Figure 6. Operating Sequence for AIC-TMS320C17

4.2 Software

The software listed in Appendix C only allows the AIC to communicaet with the TMS320C17 in synchronous mode. This communication program is supplied with an application routine, DLB (Appendix C, program listing line 253), which returns the most recently received data word back to the AIC (digital loopback).

4.2.1 Initializing the TMS320C17

The program begins with an initialization routine (INIT, page 10–45, line 120). Interrupts are disabled and all the working storage registers used by the communication program are cleared. Both transmit registers are cleared, the constants used by the program are initialized and the addresses of the subroutines called by the program are placed in data memory. This enables the interrupt service routine to call subroutines located in program-memory addresses higher than 255. After the initialization is complete, the TMS320C17 monitors the $\overline{\text{FSX}}$ interrupt flag in the control register to establish synchronization with the AIC.

4.2.2 AIC Communications and Interrupt Management

Because the AIC $\overline{\text{FSX}}$ pin is tied to the $\overline{\text{EXINT}}$ line of the TMS320C17 and the delay through the interrupt multiplexer, the interrupt service routine is called four instruction cycles after the falling edge of $\overline{\text{FSX}}$. The interrupt service routine (INTSVC, Appendix C, program listing, line 90) completes its context switching and then monitors the lower control register, polling the FSX flag bit that indicates the end of the 8-bit serial data transfer. If the $\overline{\text{FSX}}$ flag bit is set, the transfer is complete. After this bit is set, control is transferred to the interrupt subroutine whose address is stored in VECT. The serial communication must be complete before data is read from the data receive register.

When no secondary communication is to follow, the interrupt subroutines, NINT1 and NINT2, are called. If data has ben stored in DXMT2 (the low-order eight bits of the transmit data word), which does not indicate that secondary communication is to follow, the interrupt service routine calls NINT1 when the first 8-bit serial transfer is complete. NINT1 immediately writes the second byte of transmit data, (i.e., the contents of DXMT2) to transmit data register 0 (TR0). It then moves the first byte of the received data (i.e., the high-order byte of the A/D conversion result) into DRCV1. NINT1 then stores in VECT the address of NINT2. NINT2 is called at the end of the next 8-bit data transfer and resets the $\overline{\text{FSX}}$ interrupt flag bit by writing a logic high to it. The next interrupt (a falling edge of $\overline{\text{EXINT}}$) occurs before the interrupt service routine returns control to the main program. THis is an acceptable situation since the TMS320C17, on leaving the interrupt service routine, recognizes that an interrupt has occurred and immediately responds by servicing the interrupt.

The interrupt subroutine NINT2 is similar in operation to NINT1. It stores the low-order byte of receive data (bits 7 through 0 of the A/D conversion result) and stores the address of the next interrupt subroutine in VECT. NINT2 does not write to the transmit data register, TR0. This task has been left to the application program. After the transmit data has been prepared by the main program and the data has been stored in DXMT1 and DXMT2, the main program stores the first byte of the transmit data in transmit data register 0 (TR0).

4.2.3 Secondary Communications

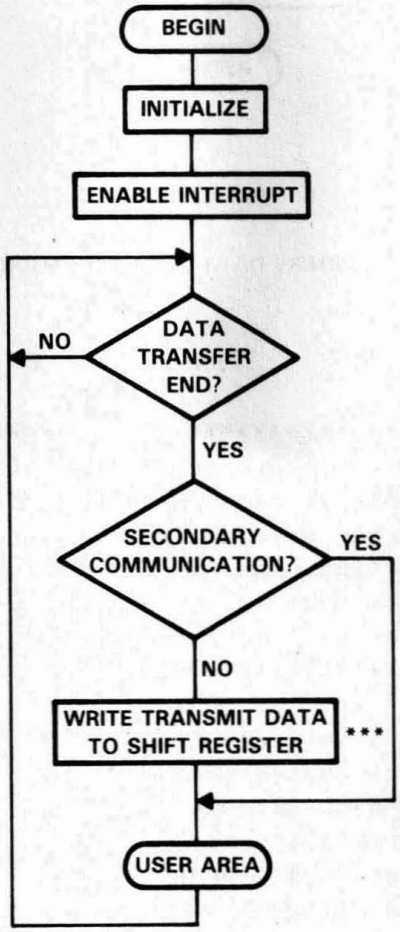
The interrupt subroutines SINT1 through SINT4 are called when secondary communication is required. For secondary communication, DXMT1 and DXMT2 will hold the primary communication word. DXMT3 and DXMT4 will hold the secondary communication word. VECT, the subroutine pointer should then be initialized to the address of SINT1. As with the normal (primary communication only) interrupt subroutines (i.e., NINT1 and NINT2), the secondary communication routines will change VECT to point to the succeeding routine (e.g., SINT1 will point to SINT2, SINT2 will point to SINT3, etc.).

5 Summary

The TLC32040 is an excellent choice for many digital signal processing applications such as speech recognition/storage systems and industrial process control. The different serial modes of the AIC (synchronous, asynchronous, 8- and 16-bit) allow it to interface easily with all of the serial port members of the TMS320 family as well as other processors.

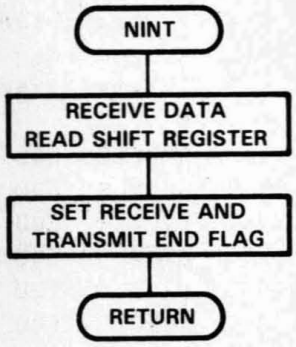
A TLC32040 and TMS32010 Flowcharts and Communication Program

A.1 Flowcharts

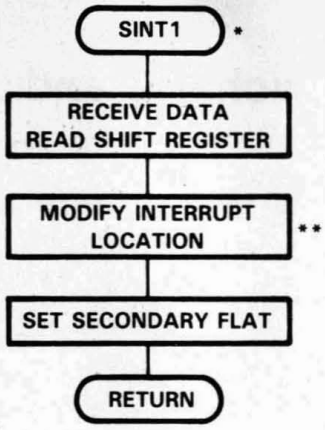


***Modified to call NINT.

a. MAIN

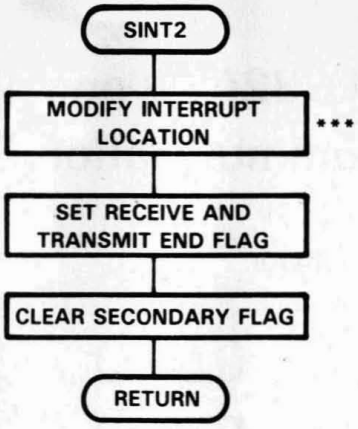


b. PRIMARY INTERRUPT ROUTINE



*Set, if need secondary.
**Modify to call SINT2.
***Modify to call NINT.
****Must execute before transfer beginning.

c. SECONDARY DATA COMMUNICATIONS 1



d. SECONDARY DATA COMMUNICATION 2

A.2 Communication Program List

```
0001            ********************************************************************
0002            *   When using this program, the circuit in the TLC32040   *
0003            *  data sheet or its  equivalent circuit must be used.     *
0004            *  TMS32010 port 0 and port 1 are reserved for data        *
0005            *  receiving and data  transmitting. The TBLW command is   *
0006            *  prohibited because it has the same timing as the OUT    *
0007            *  command. TLC32040 is used only in synchronous mode.     *
0008            ********************************************************************
0009            *
0010      0002  RXEFLG  EQU   >02      receive & xmit end flag.
0011      0003  SNDFLG  EQU   >03      secondary communication flag.
0012      0004  DRCV    EQU   >04      receive data storage.
0013      0005  DXMT    EQU   >05      xmit    data storage.
0014      0006  D2ND    EQU   >06      secondary data storage.
0015      0007  XVECT   EQU   >07      interrupt address storage.
0016      0008  ACHSTK  EQU   >08      ACCH stack.
0017      0009  ACLSTK  EQU   >09      ACCL stack.
0018      000A  SSTSTK  EQU   >0A      Status stack.
0019      000C  ANINT   EQU   >0C      interrupt address 1
0020      000D  ASINT1  EQU   >0D      interrupt address 2
0021      000E  ASINT2  EQU   >0E      interrupt address 3
0022      000F  TMP0    EQU   >0F      temporary register.
0023            *
0024      00FF  SET     EQU   >FF
0025      0001  ONE     EQU   >01
0026            *    =================
0027            *      Reset vector.
0028            *    =================
0029 0000             AORG  >0000    program start address.
0030 0000 F900        B     EPIL     jump to Initialization.
     0001 000D
```

```
0031            ********************************************************************
0032            *     ==================                                           *
0033            *      Interrupt vector.                                           *
0034            *     ==================                                           *
0035            *      When secondary communication, modify the content            *
0036            *     of XVECT to the address of secondary communication           *
0037            *     and store secondry data in D2ND.                             *
0038            *   ex.                                                            *
0039            *        LAC   ASINT1,0  modify XVECT.                             *
0040            *        SACL  XVECT,0                                             *
0041            *            |                                                     *
0042            *        LAC   D2ND,0    store secondary data.                     *
0043            ********************************************************************
0044 0002              AORG  >0002    interrupt vector.
0045 0002
0046 0002 7C0A  INTSVC SST   SSTSTK   push status register.
0047 0003 6E01         LDPK  ONE      set data pointer one.
0048 0004 5808         SACH  ACHSTK   push ACCH.
0049 0005 5009         SACL  ACLSTK   push ACCL.
0050 0006 2007         LAC   XVECT,0  load interrupt address.
0051 0007 7F8C         CALA           branch to interrupt routine.
0052 0008 6508         ZALH  ACHSTK   pop ACCH
0053 0009 7A09         OR    ACLSTK   pop ACCL.
0054 000A 7B0A         LST   SSTSTK   pop stack register.
0055 000B 7F82         EINT           enable interrupt.
0056 000C 7F8D         RET            return from interrupt routine.
0057            ********************************************************
0058            *     ============================                     *
0059            *      Initialization after reset.                     *
0060            *     ============================                     *
0061            *                                                      *
0062            *   Data RAM locations 82H(130) through 8FH(143),      *
0063            *   12 words of Page 1, are reserved for this          *
0064            *   program. The user must set the status register     *
0065            *   by adding the SST command at the end of the        *
0066            *   the initialization routine.                        *
0067            ********************************************************
0068            *
0069            *
0070            *
0071 000D              AORG  $        initial program.
0072 000D
0073 000D 6E01  EPIL   LDPK  ONE      set Data page pointer one.
0074 000E
0075 000E 7E01         LACK  ONE      save normal communication address
0076 000F 500F         SACL  TMP0     to its storage.
0077 0010 6A0F         LT    TMP0
0078 0011 802C         MPYK  NINT
0079 0012 7F8E         PAC
0080 0013 500C         SACL  ANINT
0081 0014
0082 0014 8030         MPYK  SINT1    save secondary communication addressl
0083 0015 7F8E         PAC            to its storage.
0084 0016 500D         SACL  ASINT1
```

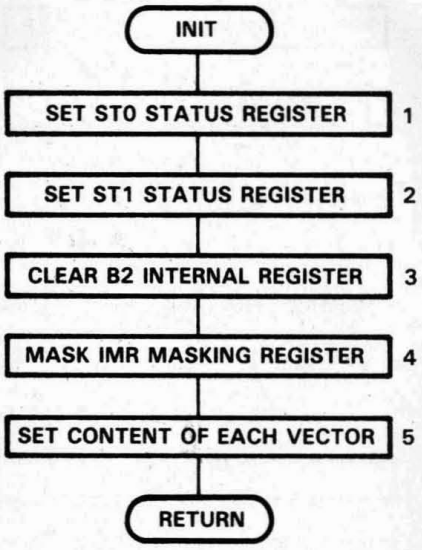
```
0085 0017
0086 0017 8037          MPYK  SINT2    save secondary communication address2
0087 0018 7F8E          PAC             to its storage.
0088 0019 500E          SACL  ASINT2
0089 001A
0090 001A 803E          MPYK  IGINT     ignore interrupt once after master
0091 001B 7F8E          PAC             reset.
0092 001C 5007          SACL  XVECT
0093 001D
0094 001D 7F89          ZAC             clear flags.
0095 001E 5002          SACL  RXEFLG,0
0096 001F
0097 001F 5003          SACL  SNDFLG,0
0098 0020
0099 0020
0100 0020
0101 0020 7F82          EINT            enable interrupt.
0102              *
0103              ********************************************************************
0104              *           ====================                                   *
0105              *             Main program.                                        *
0106              *           ====================                                   *
0107              *                                                                  *
0108              *  This program allows the user two levels of nesting              *
0109              * since one level is used as stack for the interrupt.              *
0110              * When the RXEFLG flag is false then no data transfer has          *
0111              * occurred, if it is true then data transfer has finished.         *
0112              * User routines such as digital filter, secondary-data-            *
0113              * communication judgement etc. must be placed in this              *
0114              * location. Depending on the sampling rate (conversion             *
0115              * rate), these user routines must write the xmit data to           *
0116              * the shift registers within approximately 500 instruction         *
0117              * cycles. If the user requires secondary communication, it         *
0118              * will be necessary to delay the OUT instruction until the         *
0119              * secondary data transfer has finished.                            *
0120              ********************************************************************
0121 0021
0122 0021 2002  MAIN    LAC   RXEFLG,0 wait for interrupt.
0123 0022 FF00          BZ    MAIN
     0023 0021
0124 0024
0125 0024 2003          LAC   SNDFLG,0 skip OUT instruction during secondary
0126 0025 FE00          BNZ   MAIN1    communication.
     0026 0028
0127 0027
0128 0027 4905          OUT   DXMT,PA1 write xmit data to shift register.
0129 0028
0130 0028 7F89  MAIN1   ZAC             clear flags.
0131 0029 5002          SACL  RXEFLG
0132 002A
0133 002A F900          B     MAIN      loop.
     002B 0021
```

```
                *
                ***********************************************************
                *    ============================                         *
                *      Normal interrupt routine.                          *
                *    ============================                         *
                *                        destroy ACC,DP.                  *
                *                                                         *
                *   Write the contents of DXMT to the 'LS299s, receive    *
                *   DAC data in DRCV, and set RXEFLG flag.                *
                ***********************************************************
002C
002C 4004  NINT    IN    DRCV,PA0 Receive data from shift register.
002D
002D 7EFF          LACK  SET      set receive and xmit ended flag.
002E 5002          SACL  RXEFLG
002F
002F 7F8D          RET            return.
                *
                ***********************************************************
                *     ==============================================     *
                *       Secondary communication interrupt routine 1.      *
                *     ==============================================     *
                *                          destroy ACC,DP                 *
                *                                                         *
                *   Write the contents of D2ND to the 'LS299s, receive    *
                *  data in DRCV, and modify XVECT for secondary communi   *
                *  -cation  interrupt.                                    *
                ***********************************************************
0030
0030 4004  SINT1   IN    DRCV,PA0 receive data from shift register.
0031
0031 4906          OUT   D2ND,PA1 write secondary data to shift
                *                                          register.
0032 200E          LAC   ASINT2,0 modify interrupt location.
0033 5007          SACL  XVECT    secondary communication 2
0034
0034 7EFF          LACK  SET      set secondary communication flag.
0035 5003          SACL  SNDFLG,0
0036
0036 7F8D          RET            return.
0037
                ***********************************************************
                *     ==============================================     *
                *       Secondary communication interrupt routine 2.      *
                *     ==============================================     *
                *                          destroy ACC,DP                 *
                *                                                         *
                *   Modify XVECT for normal communication, and set RXEFLG*
                *  flag.                                                  *
                ***********************************************************
0037
0037 200C  SINT2   LAC   ANINT    modify interrupt location
0038 5007          SACL  XVECT    normal communication.
0039
```

```
0188 0039 7EFF          LACK  SET       set receive and xmit ended flag.
0189 003A 5002          SACL  RXEFLG
0190 003B
0191 003B 7F89          ZAC             Clear secondary communication flag.
0192 003C 5003          SACL  SNDFLG,0
0193 003D
0194 003D 7F8D          RET             return.
0195 003E
0196            ********************************************************
0197            *     ========================================         *
0198            *      Ignoring the first interrupt after reset.       *
0199            *     ========================================         *
0200            *                              destroy ACC,DP.         *
0201            *                                                      *
0202            *   Ignore the first interrupt after reset. the TLC32040  *
0203            * receives zero as DAC data but no ADC data in DRCV.   *
0204            *                                                      *
0205            ********************************************************
0206 003E
0207 003E 200C  IGINT   LAC   ANINT     modify interrupt location
0208 003F 5007          SACL  XVECT     normal communication.
0209 0040
0210 0040 7F8D          RET             return.
0211 0041
0212                    END
NO ERRORS, NO WARNINGS
```

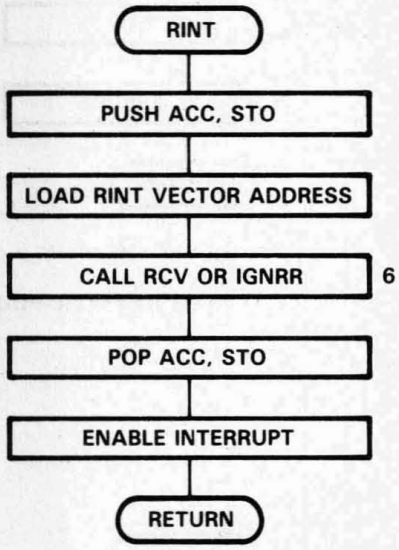
B TLC32040 and TMS32020 Flowcharts and Communication Program

B.1 Flowcharts

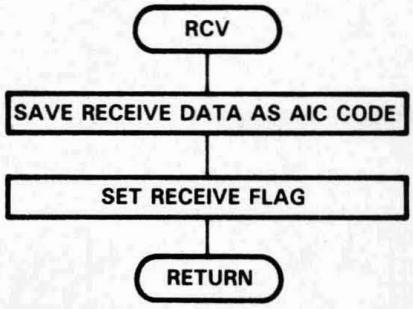


1 – Alterable AR pointer and OVM.
2 – Alterable CNF, SXM and XF.
3 – Must clear at least 108 through 127, 19 of internal RAM.
4 – If IMR is changed by user program, INST must be changed.
5 – Their contents will be changed by their routine locations.
6 – IGNRR is executed only once after reset.

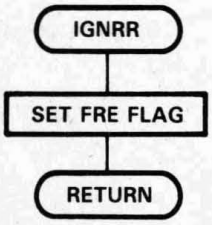
a. INITIALIZATION



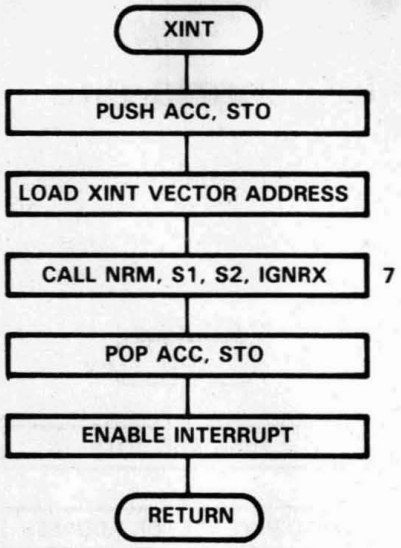
b. RECEIVE INTERRUPT SERVICE ROUTINE



c. RECEIVE SUBROUTINE

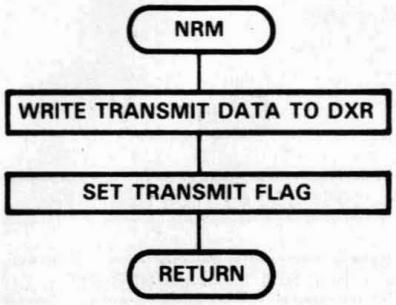


d. IGNORE INTERRUPT

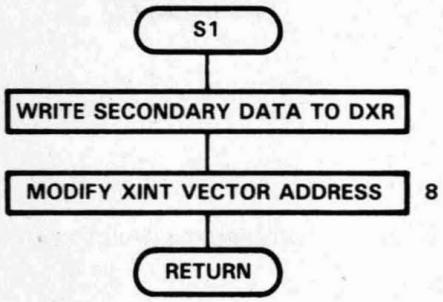


7 – IGNRX is executed only once after reset.

e. **TRANSMIT INTERRUPT SERVICE ROUTINE**

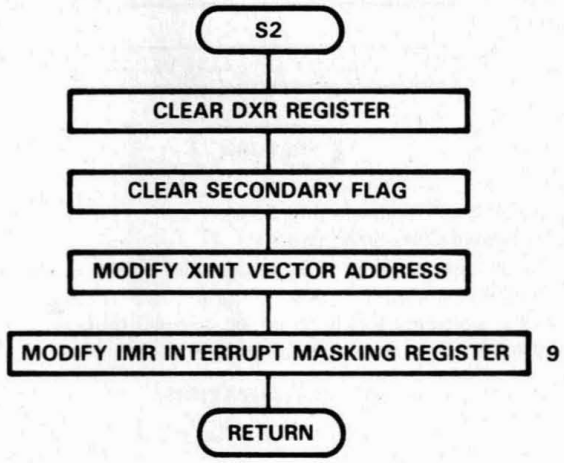


f. **PRIMARY TRANSMISSION ROUTINE**

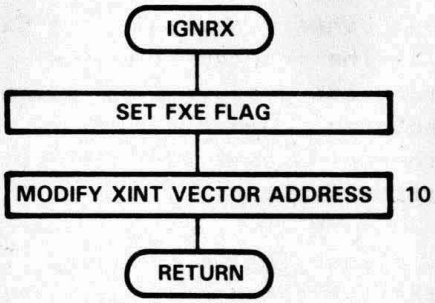


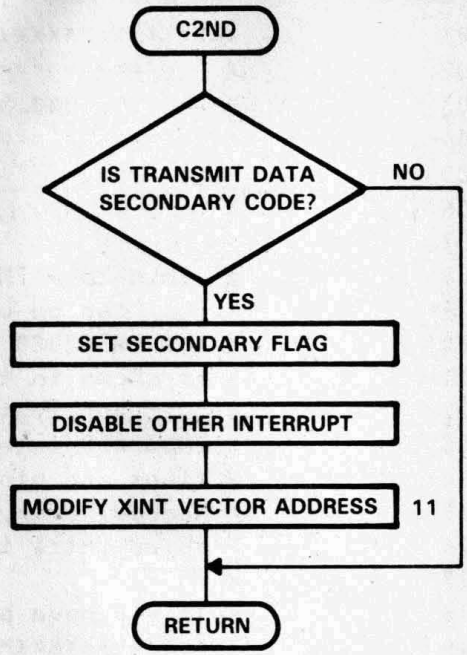
8 – Modify to S2 address.
9 – Modify to NRM address.

g. **PRIMARY-SECONDARY COMMUNICATIONS 1**



h. **PRIMARY-SECONDARY COMMUNICATIONS 2**

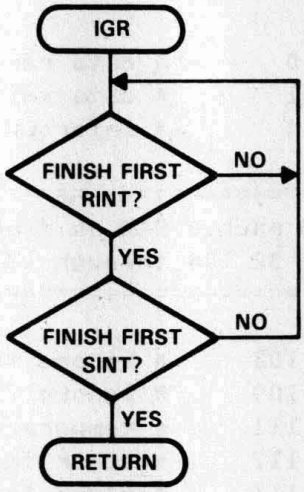




10 – Modify to NRM address.
11 – Modify to S1 address.

i. IGNORE TRANSMIT INTERRUPT

j. SECONDARY COMMUNICATION JUDGMENT



k. IGNORE FIRST INTERRUPTS

B.2 Communication Program List

```
0001            ************************************************************
0002            *   ========================================               *
0003            *    TLC32040 & TMS32020 communication program.            *
0004            *   ========================================               *
0005            *              by H.Okubo & W.Rowand                       *
0006            *                 version 1.1      7/22/88.                *
0007            *                                                          *
0008            *  This is a TMS32020 - TLC32040 communication program     *
0009            * that can be used in many systems. To use this program,   *
0010            * the TMS32020 and the TLC32040 (AIC) must be connected    *
0011            * as shown in the publication: Linear and Interface Cir-   *
0012            * cuit Applications, Volume 3. The program reserves        *
0013            * TMS32020 internal data memory 108 through 127 (B2) as    *
0014            * flags and storage. When secondary communication is       *
0015            * needed, every maskable interrupt except XINT is dis-     *
0016            * abled until that communication finishes.                 *
0017            *                                                          *
0018            * If you have any questions, please let us know.           *
0019            ************************************************************
0020            *
0021            *
0022            * ==========================
0023            *   Memory mapped register.
0024            * ==========================
0025            *
0026      0000  DRR     EQU  0       * data receive register address.
0027      0001  DXR     EQU  1       * data xmit    register address.
0028      0004  IMR     EQU  4       * interrupt mask register address.
0029            *
0030            *  ========================================
0031            *    Reserved onchip RAM as flags and storages.
0032            *      (block B2 108 through 127.)
0033            *  ========================================
0034            *
0035      006C  FXE     EQU  108     * ignore first XINT flag.
0036      006D  FRE     EQU  109     * ignore first RINT flag.
0037      006F  TMP0    EQU  111     * temporary register.
0038      0070  ACCHST  EQU  112     * stack for ACCH.
0039      0071  ACCLST  EQU  113     * stack for ACCL.
0040      0072  SSTST   EQU  114     * stack for ST0 register.
0041      0073  INTST   EQU  115     * stack for IMR register.
0042      0074  RVECT   EQU  116     * vector for RINT.
0043      0075  XVECT   EQU  117     * vector for XINT.
0044      0076  VRCV    EQU  118     * RINT vector storage.
0045      0077  VNRM    EQU  119     * XINT vector storage.
0046      0078  VS1     EQU  120     * secondary vector storagel.
0047      0079  VS2     EQU  121     * secondary vector storage2.
0048      007A  DRCV    EQU  122     * receive data storage.
0049      007B  DXMT    EQU  123     * xmit data storage.
0050      007C  D2ND    EQU  124     * secondary data storage.
0051      007D  FRCV    EQU  125     * receive flag.
0052      007E  FXMT    EQU  126     * xmit flag.
0053      007F  F2ND    EQU  127     * secondary communication flag.
0054            *
```

```
0055                ********************************************************************
0056                *   Processor starts at this address after reset.                  *
0057                *                                                                  *
0058 0000                   AORG 0       *  program start address.                    *
0059 0000 FF80              B  STRT      *  jump to Initialization routine.           *
     0001 0020
0060                ********************************************************************
0061                *
0062                ********************************************************************
0063                *   Receive interrupt location.                                    *
0064                *                                                                  *
0065 001A                   AORG 26      * Rint vector.                               *
0066 001A FF80              B  RINT      * jump to receive interrupt routine.        *
     001B 004A
0067                ********************************************************************
0068                *
0069                ********************************************************************
0070                *   Transmit interrupt location.                                   *
0071                *                                                                  *
0072 001C                   AORG 28      * Xint vector.                               *
0073 001C FF80              B  XINT      * jump to xmit interrupt routine.           *
     001D 005A
0074                ********************************************************************
0075                *
0076 0020                   AORG 32      * start initial program.
0077                *
0078                ********************************************************************
0079                *  User must initialize DSP with the routine INIT.  The            *
0080                * user may modify this routine to suit his system require-         *
0081                * ments as he likes.                                               *
0082                ********************************************************************
0083 0020 FE80      STRT    CALL INIT    *
     0021 0025
0084 0022 CE00              EINT         * enable interrupt.
0085 0023 FE80              CALL IGR
     0024 008D
0086                *
```

```
                ***********************************************************
                *                ==============                           *
                *                  User area                              *
                *                ==============                           *
                *                                                         *
                *  This program allows the user two levels of nesting,    *
                * since two levels are used as stack for the interrupt.   *
                * When the FXMT flag is false no data transmit has oc-    *
                * curred. When the FRCV flag is false, no data has been   *
                * received. As those flags are not reset by any routine in *
                * this program, the user must reset the flags if he       *
                * chooses to use them and note that >00ff means true,     *
                * >0000 means false. User routines such as digital        *
                * filtering, FFTs etc. must be placed in this location.   *
                * Depending on the sampling rate (conversion rate), these *
                * user routines must write the xmit data to the DXMT      *
                * registers within approximately 500 instruction cycles.  *
                * If the user requires secondary communication, data      *
                * with the secondary code (xxxx xxxx xxxx xx11) should    *
                * first be written to DXMT and then secondary data should *
                * be written to D2ND. Next, a call should be made to C2ND *
                * to set up XVECT and the F2ND flag to perform the secon- *
                * dary communication. Note that all maskable interrupts   *
                * except XINT are disabled until secondary communication  *
                * has completed.                                          *
                ***********************************************************
                *
                ***********************************************************
                *      =======================                            *
                *       Initialization routine.                           *
                *      =======================                            *
                *  This routine initializes the status registers, flags,  *
                * vector storage contents and internal data locations     *
                * 96 through 107. Note that the User can modify these     *
                * registers (i.e. ST0 ST1 IMR), as long as the contents do *
                * not conflict with the operation of the AIC.             *
                ***********************************************************
0025 C800   INIT    LDPK 0          * set status0 register.
0026 D001           LALK >0E00,0    * 0000 1110 0000 0000B
0027 0E00
0028 606F           SACL TMP0,0     * ARP=0  AR pointer 0
0029 506F           LST  TMP0       * OV =0 (Overflow reg.clear)
                *                   * OVM=1 (Overflow mode set to 1)
                *                   * ?  =1  Not affected.
                *                   * INTM=1 Not affected
                *                   * DP 000000000 page 0
                *
                *                   * set status1 register.
                *                   *
002A D001           LALK  >03F0     * 0000 0011 1111 0000B
002B 03F0
002C 606F           SACL  TMP0,0    * APB=0
002D 516F           LST1  TMP0      * CNF=0 (Set B0 data memory)
002E
```

```
0139                    *                       * TC =0
0140                    *                       * SXM=1 (enable sign extend mode.)
0141                    *                       * D9-D5=111111 not affected.
0142                    *                       * XF=1 (XF pin status.)
0143                    *                       * F0=0 (16bit data transfer mode.)
0144                    *                       * TXM=0 (FSX input)
0145                    *
0146                    *                       *
0147                    *
0148 002E CA00                 ZAC                     * clear  registers
0149 002F 6001                 SACL    DXR,0           *
0150 0030 6000                 SACL    DRR,0           *
0151 0031 C060                 LARK    AR0,96          * clear Block B2.
0152 0032 CB1F                 RPTK    31              *
0153 0033 60A0                 SACL    *+,0            *
0154                    *
0155                    *   Interrupt masking
0156                    *
0157 0034 CA30                 LACK    >30             * 0000 0000 0011 0000B
0158 0035 6004                 SACL    IMR,0           * XINT________|| ||||
0159 0036 6073                 SACL    INTST,0         * RINT_________| ||||
0160                    *                               * TINT__________||||
0161                    *                               * INT2___________|||
0162                    *                               * INT1____________||
0163                    *                               * INT0_____________|
0164                    *
0165 0037 D001                 LALK    NRM,0           * normal xint routine address.
     0038 0067
0166 0039 6077                 SACL    VNRM,0          *
0167                    *
0168 003A D001                 LALK    S1,0            * secondary xint routine address 1.
     003B 006C
0169 003C 6078                 SACL    VS1,0           *
0170                    *
0171 003D D001                 LALK    S2,0            * secondary xint routine address 2.
     003E 0071
0172 003F 6079                 SACL    VS2,0           *
0173                    *
0174 0040 D001                 LALK    RCV,0           * rint routine address.
     0041 0055
0175 0042 6076                 SACL    VRCV,0
0176                    *
0177 0043 D001                 LALK    IGNRR,0         * set ignore first rint address.
     0044 0094
0178 0045 6074                 SACL    RVECT,0
0179                    *
0180 0046 D001                 LALK    IGNRX,0         * set ignore first xint address.
     0047 0099
0181 0048 6075                 SACL    XVECT,0
0182 0049 CE26                 RET                     * return.
0183 004A
```

```
                *
                ***************************************************************
                *      ================================                       *
                *          Receive interrupt routine.                         *
                *      ================================                       *
                *  This routine stores receive data in its storage            *
                * DRCV (112 page0) and sets the receive flag FRCV (125        *
                * page0). As two levels of nesting are used, this routine     *
                * allows the user two levels, without stack extension.        *
                ***************************************************************
004A 7872       RINT    SST SSTST       * push ST0 register.
004B C800               LDPK 0          * data pointer page 0.
004C 6071               SACL ACCLST,0   * push ACCL.
004D 6870               SACH ACCHST,0   * push ACCH.
004E 2074               LAC  RVECT,0    * load ACC vector address.
004F CE24               CALA
0050 4171               ZALS ACCLST     * pop ACC
0051 4870               ADDH ACCHST
0052 5072               LST SSTST       * pop ST register.
0053 CE00               EINT            * enable interrupts.
0054 CE26               RET             * return.
                *
0055 2000       RCV     LAC DRR,0       * load data from DRR.
0056 607A               SACL DRCV,0     * save it to its storage.
0057 CAFF               LACK >FF        * set receive flag.
0058 607D               SACL FRCV       *
0059 CE26               RET             * return.
                *
                ***************************************************************
                *     ==================================                      *
                *          Xmit interrupt routine.                            *
                *     ==================================                      *
                *  This routine writes xmit data (the contents of DXMT        *
                * (123 page0)) to the DXR register according to the type      *
                * of communication, i.e. normal communication or secondary    *
                * communication. For normal communication, call the normal    *
                * communication routine (NRM). For secondary, call the        *
                * secondary communication routines (S1 and S2). Because       *
                * these routines use two levels of nesting, the user is       *
                * allowed two levels of nesting if stack extension is not     *
                * used.                                                       *
                ***************************************************************
005A 7872       XINT    SST SSTST       * push ST register.
005B C800               LDPK 0          * data pointer page 0.
005C 6071               SACL ACCLST,0   * push ACCL.
005D 6870               SACH ACCHST,0   * push ACCH.
005E 207C               LAC D2ND,0      * preload dxr with secondary
005F 6001               SACL DXR,0      * communication data.
0060 2075               LAC XVECT,0     * load vector address.
0061 CE24               CALA            * call xmit routine.
0062 4171               ZALS ACCLST     * pop ACC
0063 4870               ADDH ACCHST
0064 5072               LST SSTST       * pop ST register.
0065 CE00               EINT            * enable interrupt.
0066 CE26               RET             * return.
```

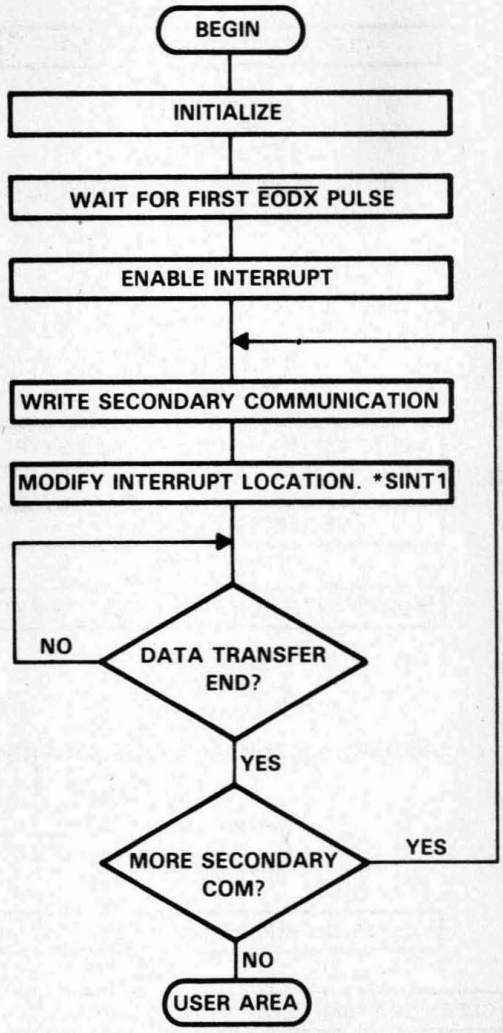
```
0239                ********************************************************************
0240                *      ==================================                          *
0241                *        Normal data write routine.                                *
0242                *      ==================================                          *
0243                *  This routine is called when normal communication occurs.*
0244                * This routine writes xmit data to DXR, and sets the trans-*
0245                * mit flag (126 page0).                                             *
0246                ********************************************************************
0247                *
0248 0067 207B     NRM     LAC DXMT,0      * write DXR data.
0249 0068 6001             SACL DXR,0
0250 0069 CAFF             LACK >FF        * set flag.
0251 006A 607E             SACL FXMT
0252 006B CE26             RET             * return.
0253                ********************************************************************
0254                *      ====================================                        *
0255                *        Secondary data write routine 1.                           *
0256                *      ====================================                        *
0257                *  This routine is called when secondary communication           *
0258                * occurs. It writes secondary data to DXR, and and modifies*
0259                * the content of XVECT(117 page0) for continuing secondary *
0260                * communication.                                                    *
0261                ********************************************************************
0262 006C 207C     S1      LAC D2ND,0      * write DXR 2nd data.
0263 006D 6001             SACL DXR,0
0264 006E 2079             LAC VS2,0       * modify for next XINT.
0265 006F 6075             SACL XVECT,0
0266 0070 CE26             RET             * return.
0267                *
0268                ********************************************************************
0269                *      ====================================                        *
0270                *        Secondary data writing routine 2.                         *
0271                *      ====================================                        *
0272                *                                                                  *
0273                *  This routine is called when secondary communication           *
0274                *  occurs. It writes dummy data to DXR to ensure that            *
0275                *  secondary communication is not inadvertently initiated        *
0276                *  on the next XINT. It also modifies the content of XVECT       *
0277                *  for normal communication.                                     *
0278                ********************************************************************
0279 0071 CA00     S2      ZAC             * clear data for protection.
0280 0072 6001             SACL DXR,0      * of double secondary communication.
0281 0073 607F             SACL F2ND       * clear secondary flag.
0282 0074 CAFF             LACK >FF        * set xmit end flag.
0283 0075 607E             SACL FXMT,0
0284 0076 2077             LAC  VNRM,0     * set normal communication vector.
0285 0077 6075             SACL XVECT,0
0286 0078 2073             LAC  INTST,0    * enable all interrupts.
0287 0079 6004             SACL IMR,0
0288 007A CE26             RET             * return.
```

```
0289                    *
0290                    ************************************************************
0291                    *     ======================                               *
0292                    *      Check  secondary code.    destroy DP pointer.       *
0293                    *     ======================            ACC.               *
0294                    *                                                          *
0295                    *  This routine checks whether the data in DXMT (123 page0)*
0296                    * has secondary code or not. If secondary code exists,     *
0297                    * then disable maskable interrupts except XINT, modify the *
0298                    * contents of XVECT(117 page0) for secondary communication,*
0299                    * and set secondary flag. Note that we recommend calling   *
0300                    * this routine to send control words to the AIC.           *
0301                    ************************************************************
0302 007B C800  C2ND    LDPK 0          * data page pointer 0.
0303 007C CA03          LACK 03
0304 007D 606F          SACL TMP0
0305 007E 207B          LAC  DXMT,0     * is this data secondary code ?
0306 007F 4E6F          AND TMP0
0307 0080 106F          SUB TMP0,0      *
0308 0081 F680          BZ   C2ND1      * if yes, then next.
     0082 0084
0309 0083 CE26          RET             * else return.
0310                    *
0311 0084 CAFF  C2ND1   LACK >FF        * set secondary flag.
0312 0085 607F          SACL F2ND,0
0313 0086 CA20          LACK >20        * enable only XINT.
0314 0087 6004          SACL IMR,0
0315 0088 2078          LAC VS1,0       *modify vector address for secondary
0316 0089 6075          SACL XVECT,0    * communication.
0317 008A 207B          LAC  DXMT,0     * write primary data to DXR.
0318 008B 6001          SACL DXR,0
0319 008C CE26          RET             * return.
0320                    *
0321                    ************************************************************
0322                    *                                                          *
0323                    *   ======================                                 *
0324                    *    Check first interrupt                                 *
0325                    *   ======================                                 *
0326                    *                                                          *
0327                    *   This routine checks if both first interrupts have      *
0328                    *  occurred. If this routine is called after reset, it     *
0329                    *  waits for both interrupts then returns.                 *
0330                    ************************************************************
0331 008D 206D  IGR     LAC  FRE,0    * check first interrupt after
0332 008E F680          BZ   IGR      * master reset.
     008F 008D
0333 0090 206C          LAC  FXE,0
0334 0091 F680          BZ   IGR
     0092 008D
0335 0093 CE26          RET
0336 0094
```

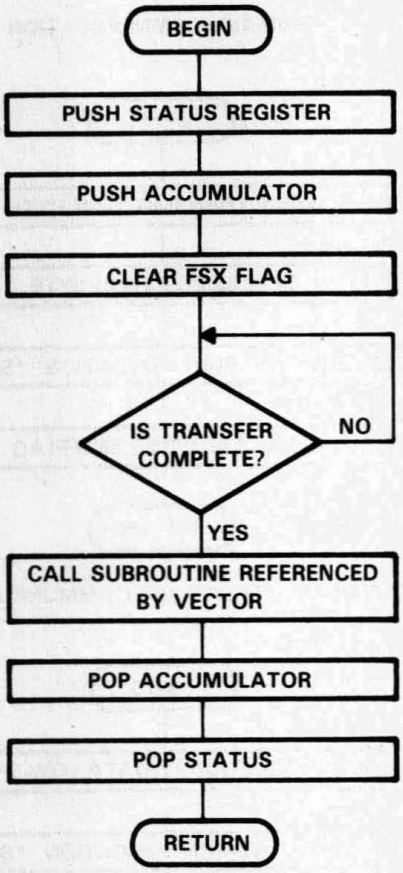
```
0337                *
0338                ******************************************************************
0339                *      ==============================                            *
0340                *        Ignore interrupt routine.                               *
0341                *      ==============================                            *
0342                *  These routines are used so that the first RINT and XINT       *
0343                * after the DSP reset can be ignored. They set flags and         *
0344                * modify each vector address to the normal interrupt             *
0345                * address but do not read or write to the serial ports.          *
0346                * Note that the first data that the AIC will receive after       *
0347                * the DSP reset is >0000.                                        *
0348                ******************************************************************
0349 0094 CAFF   IGNRR   LACK >FF
0350 0095 606D           SACL FRE,0
0351 0096 2076           LAC  VRCV,0      * set normal receive address.
0352 0097 6074           SACL RVECT,0     *
0353 0098 CE26           RET               * return.
0354                *
0355 0099 CAFF   IGNRX   LACK >FF
0356 009A 606C           SACL FXE,0
0357 009B 2077           LAC  VNRM,0      * set normal xmit address.
0358 009C 6075           SACL XVECT,0     *
0359 009D CE26           RET               * return.
0360                *
0361                     END
NO ERRORS, NO WARNINGS
```

C TLC32040 and TMS320C17 Flowcharts and Communication Program

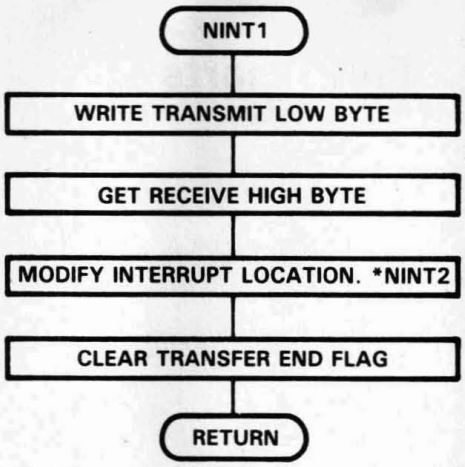
C.1 Flowcharts



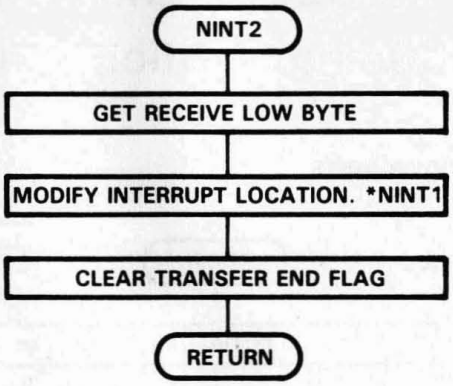
a. MAIN



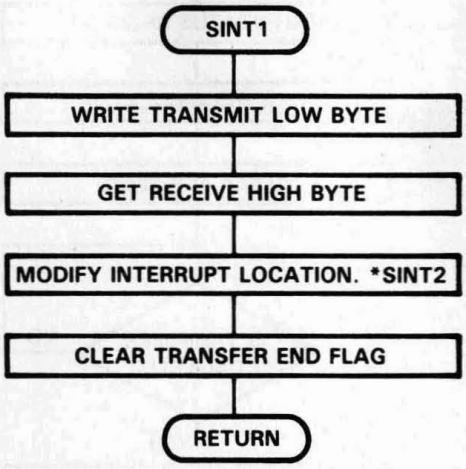
b. INTERRUPT SERVICE ROUTINE



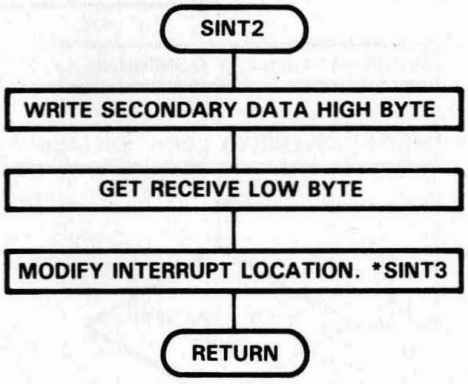
c. PRIMARY COMMUNICATION 1



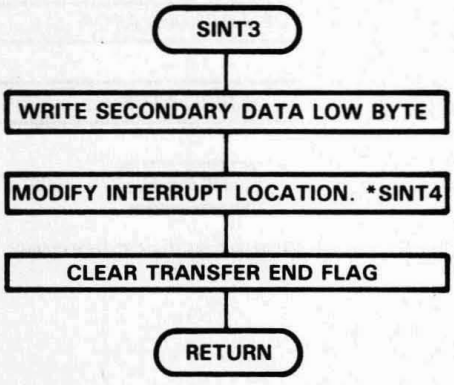
d. PRIMARY COMMUNICATION 2



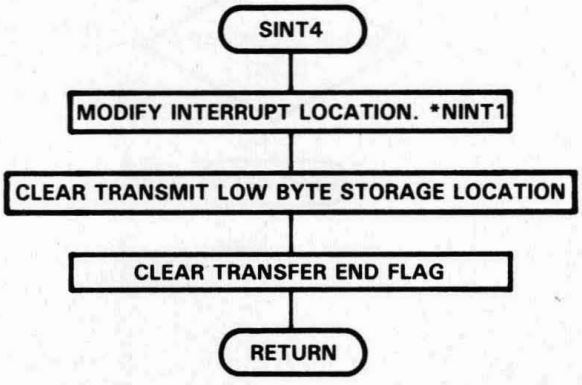
e. PRIMARY-SECONDARY COMMUNICATION 1



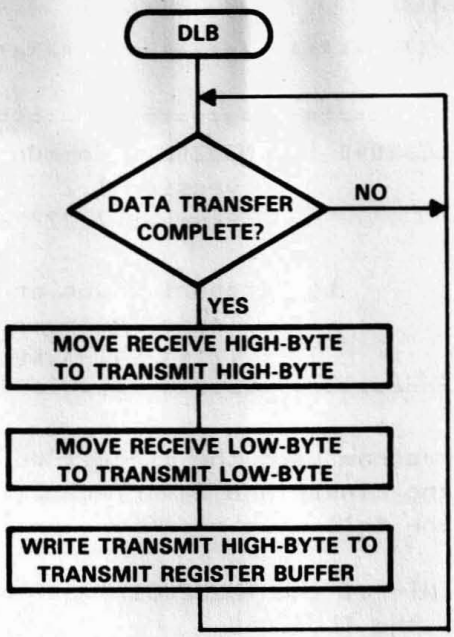
f. PRIMARY-SECONDARY COMMUNICATION 2



g. PRIMARY-SECONDARY COMMUNICATION 3



h. PRIMARY-SECONDARY COMMUNICATION 4



i. DIGITAL LOOPBACK

C.2 Communication Program List

```
0001            ****************************************************************
0002            *                                                              *
0003            *  ========================================================    *
0004            *      TLC32040 to TMS320C17 Communication Program             *
0005            *                    version 1.2                               *
0006            *                    revised 7/22/88                           *
0007            *                                                              *
0008            *               by Hironori Okubo and Woody Rowand             *
0009            *                    Texas Instruments                         *
0010            *                    (214) 997-3460                            *
0011            *  ========================================================    *
0012            *                                                              *
0013            *  This program uses the circuit published in the Volume       *
0014            *  3 of the Linear and Interface Circuit Applications book     *
0015            *  with the following modification:                            *
0016            *                                                              *
0017            *    1. INT- of the TMS320C17 must be connected to EODX-       *
0018            *       of the TLC32040.                                       *
0019            *                                                              *
0020            *                                                              *
0021            *  In this configuration, the program will allow the           *
0022            *  TLC32040 to communicate with the TLC320C17                  *
0023            *  with the restriction that all interrupts except INT-        *
0024            *  are prohibited and only synchronous communication           *
0025            *  can occur. The program allows the user two levels of        *
0026            *  nesting in the main program; the remaining two levels       *
0027            *  are reserved for the interrupt vector and subroutines.      *
0028            *                                                              *
0029            *  If desired, this program may be used with the               *
0030            *  TMS32011 Digital Signal Processor with the following        *
0031            *  change. Since the TMS32011 has only sixteen words of        *
0032            *  data RAM on data page 1, all of the registers used by       *
0033            *  this program should be moved to data page 0, except         *
0034            *  for SSTSTK (the temporary storage location for the          *
0035            *  status register) which must remain on page 1 (since         *
0036            *  the SST instruction always addresses page 1).               *
0037            *                                                              *
0038            ****************************************************************
0039    0000    SSTSTK EQU   >00        stack for status (SST) register.
0040    0001    ACHSTK EQU   >01        stack for accumulator high (ACCH).
0041    0002    ACLSTK EQU   >02        stack for accumulator low (ACCL).
0042    0003    RXEFLG EQU   >03        xmit/receive in progress.
0043    0004    DRCV1  EQU   >04        storage for high byte receive data.
0044    0005    DRCV2  EQU   >05        storage for low byte receive data.
0045    0006    DXMT1  EQU   >06        storage for high byte xmit data.
0046    0007    DXMT2  EQU   >07        storage for low byte xmit data.
0047    0008    DXMT3  EQU   >08        storage for high byte secndry data.
0048    0009    DXMT4  EQU   >09        storage for low byte secndry data.
0049    000A    VECT   EQU   >0A        storage for interrupt vector addr.
0050    000B    ANINT1 EQU   >0B        storage for normal xmit/rcv vect 1.
0051    000C    ANINT2 EQU   >0C        storage for normal xmit/rcv vect 2.
0052    000D    ASINT1 EQU   >0D        storage for secndry xmit/rcv vect 1.
0053    000E    ASINT2 EQU   >0E        storage for secndry xmit/rcv vect 2.
0054    000F    ASINT3 EQU   >0F        storage for secndry xmit/rcv vect 3.
```

```
0055 0000
0056       0010  ASINT4 EQU   >10         storage for secndry xmit/rcv vect 4.
0057       0011  CNTREG EQU   >11         storage for control register.
0058       0012  MXINT  EQU   >12         storage for xmit interrupt mask.
0059       0013  CLRX   EQU   >13         storage for xmit interrupt clear.
0060       0014  CLRX1  EQU   >14         storage for xmit intrpt clear/mask.
0061       0015  TEMP   EQU   >15         temporary register.
0062       00FF  FLAG   EQU   >FF         flag set.
0063             *   ====================================
0064             *      Branch to initialization routine.
0065             *   ====================================
0066 0000                    AORG  >0000
0067 0000 F900               B     INIT       branch to initialization routine.
     0001 0013
0068 0002
0069             ****************************************************************
0070             *  ================================                            *
0071             *      Interrupt service routine.                              *
0072             *  ================================                            *
0073             *                                                              *
0074             *  To initiate secondary communication, change the             *
0075             *  contents of VECT to the address of the secondary            *
0076             *  communication subroutine and store the information          *
0077             *  in DXMT3 and DXMT4.                                         *
0078             *                                                              *
0079             *  e.g.                                                        *
0080             *      LAC   ASINT1     modify VECT.                           *
0081             *      SACL  VECT                                              *
0082             *         |                                                    *
0083             *      LAC   H1         store high-byte of secondary           *
0084             *      SACL  DXMT3      information in DXMT3.                  *
0085             *      LAC   H2         store low-byte in DXMT4.               *
0086             *      SACL  DXMT4                                             *
0087             *                                                              *
0088             ****************************************************************
0089 0002                    AORG  >02
0090 0002 6E01  INTSVC LDPK  1
0091 0003 7C00               SST   SSTSTK     push status register.
0092 0004 5801               SACH  ACHSTK     push accumulator high.
0093 0005 5002               SACL  ACLSTK     push accumulator low.
0094 0006 4813               OUT   CLRX,PA0   make sure FSX-flag is clear.
0095 0007 4011  WAIT1  IN    CNTREG,PA0 read control register.
0096 0008 2011               LAC   CNTREG,0   load accumulator with control reg.
0097 0009 7912               AND   MXINT      mask-off xmit interrupt flag.
0098 000A FF00               BZ    WAIT1      loop until xmit interrupt flag is
     000B 0007
0099 000C
0100             *                             recognized.
0101 000C 200A               LAC   VECT       load acc with interrupt vector.
0102 000D 7F8C               CALA             call appropriate xmit/rcv routines.
0103 000E 6501               ZALH  ACHSTK     pop accumulator high.
0104 000F 7A02               OR    ACLSTK     pop accumulator low.
0105 0010 7B00               LST   SSTSTK     pop status register.
0106 0011 7F82               EINT             enable interrupts.
0107 0012 7F8D               RET              return to main program.
```

```
0013
                ***************************************************************
                *  ===================================                        *
                *      Initialization after reset.                            *
                *  ===================================                        *
                *                                                             *
                *  Data RAM locations >80 through >92 are reserved by         *
                *  this program. The user must set the status register        *
                *  at the end of this program with the SST command or        *
                *  a combination of SOVM, LDPK etc.                           *
                *                                                             *
                ***************************************************************
0013 7F81       INIT   DINT                 disable interrupts.
0014 6E01              LDPK  1              set Data page pointer one.
0015 7F89              ZAC                  clear registers.
0016 6880              LARP  0
0017 7083              LARK  0,RXEFLG+>80
0018 50A8              SACL  *+
0019 50A8              SACL  *+
001A 50A8              SACL  *+
001B 50A8              SACL  *+
001C 50A8              SACL  *+
001D 50A8              SACL  *+
001E 50A8              SACL  *+
001F 5088              SACL  *
0020 4906              OUT   DXMT1,PA1      clear transmit registers.
0021 4906              OUT   DXMT1,PA1
0022 7E04              LACK  ?00000100
0023 5012              SACL  MXINT          initialize xmit-int mask.
0024 7E01              LACK  1              prepare for serial port initial-
0025 5015              SACL  TEMP           ization and initialization of regis-
0026 6A15              LT    TEMP           ters containing 16-bit constants.
0027 80A1              MPYK  CLX1           initialize interrupt flag clear.
0028 7F8E              PAC
0029 6713              TBLR  CLRX
002A 80A2              MPYK  CLX2           initialize interrupt flag clear
002B 7F8E              PAC                  with interrupts disabled.
002C 6714              TBLR  CLRX1
002D 809D              MPYK  IGN
002E 7F8E              PAC
002F 500A              SACL  VECT           initialize interrupt vector.
0030 8077              MPYK  NINT1          save normal communication address
0031 7F8E              PAC                  to its storage.
0032 500B              SACL  ANINT1
0033 807D              MPYK  NINT2          save normal communication address 2
0034 7F8E              PAC                  to its storage.
0035 500C              SACL  ANINT2
0036 8084              MPYK  SINT1          save secondary communication
0037 7F8E              PAC                  address 1 to its storage.
0038 500D              SACL  ASINT1
0039 808A              MPYK  SINT2          save secondary communication
003A 7F8E              PAC                  address 2 to its storage.
003B 500E              SACL  ASINT2
003C 8090              MPYK  SINT3          save secondary communication
003D 7F8E              PAC                  address 3 to its storage.
```

```
0163 003E 600F          SACL  ASINT3
0164 003F A095          MPYK  SINT4       save secondary communication
0165 0040 CE14          PAC               address 4 to its storage.
0166 0041 6010          SACL  ASINT4
0167 0042
0168              ****************************************************************
0169              *  ========================================                    *
0170              *      Synchronize high/low byte transmission.                 *
0171              *  ========================================                    *
0172              *                                                              *
0173              *    The time between FSX- interrupts is approximately         *
0174              *    ten microseconds (50 cycles). Wait for first              *
0175              *    FSX-, if this is the first interrupt, delay 60            *
0176              *    cycles (past the second interrupt). If it is the          *
0177              *    second interrupt, no harm done.                           *
0178              *                                                              *
0179              ****************************************************************
0180 0042 E014          OUT   CLRX1,PA0   clear interrupt flags, disable int.
0181 0043 8011  IGNOR   IN    CNTREG,PA0  read control register.
0182 0044 2011          LAC   CNTREG      wait
0183 0045 4E12          AND   MXINT             for
0184 0046 F680          BZ    IGNOR                 FSX- flag.
     0047 0043
0185 0048
0186 0048 C014          LARK  0,20        wait 60 cycles (20 X 3 cycles) in
0187 0049 5500  IGNOR1  NOP               case FSX- int. is first of the pair.
0188 004A FB90          BANZ  IGNOR1      if FSX- int was the second, delay
     004B 0049
0189 004C
0190 004C E013          OUT   CLRX,PA0    anyway.
0191 004D
0192 004D CE00          EINT              enable interrupt.
0193              ****************************************************************
0194              *  ================================                            *
0195              *      Main program (user area)                                *
0196              *  ================================                            *
0197              *                                                              *
0198              *  This program allows the user two levels of nesting,         *
0199              *  since one level is used as stack for the interrupt and      *
0200              *  the interrupt service routine makes one subroutine call.    *
0201              *  User routines such as digital filtering, FFTs, and          *
0202              *  secondary communication judgement may be placed here.       *
0203              *  The number of instruction cycles between interrupts         *
0204              *  varies with the sampling rate.  In the power-up             *
0205              *  condition this is approximately 500 cycles.                 *
0206              *                                                              *
0207              *  In the example below, the first two transmissions send      *
0208              *  secondary information to the AIC. The first configures      *
0209              *  the TB and RB registers. The second configures the          *
0210              *  control register.                                           *
0211              *                                                              *
0212              ****************************************************************
0213 004E CA00  MAIN    ZAC               prepare first control word.
0214 004F 6006          SACL  DXMT1
0215 0050 CA03          LACK  >03
```

```
0216 0051 5007          SACL  DXMT2       should be xxxx xx11.
0217 0052 7E24          LACK  >24
0218 0053 5008          SACL  DXMT3
0219 0054 7E92          LACK  >92
0220 0055 5009          SACL  DXMT4
0221 0056 200D          LAC   ASINT1      set VECT for secondary
0222 0057
0223 0057 500A          SACL  VECT        communications.
0224 0058 4906          OUT   DXMT1,PA1   store first transmit byte in
0225                    *                 transmit buffer.
0226 0059 7F89          ZAC
0227 005A 5003          SACL  RXEFLG      clear xmit/rcv end flag.
0228 005B 2003  MAIN1   LAC   RXEFLG
0229 005C FF00          BZ    MAIN1       wait for data transfer to complete.
     005D 005B
0230 005E
0231 005E 7F89          ZAC               prepare second control word.
0232 005F 5006          SACL  DXMT1
0233 0060 7E03          LACK  >03
0234 0061 5007          SACL  DXMT2
0235 0062 7E00          LACK  >00
0236 0063 5008          SACL  DXMT3
0237 0064 7E67          LACK  >67
0238 0065 5009          SACL  DXMT4
0239 0066 200D          LAC   ASINT1
0240 0067 500A          SACL  VECT
0241 0068 4906          OUT   DXMT1,PA1
0242 0069 7F89          ZAC
0243 006A 5003          SACL  RXEFLG      clear xmit/rcv end flag.
0244                    ****************************************************
0245                    *  ================================               *
0246                    *       Digital loop-back program                 *
0247                    *  ================================               *
0248                    *                                                 *
0249                    *  This program serves as an example of what can be done  *
0250                    *  in the user area.                              *
0251                    *                                                 *
0252                    ****************************************************
0253 006B 2003  DLB     LAC   RXEFLG      wait for data transfer to complete.
0254 006C FF00          BZ    DLB
     006D 006B
0255 006E
0256 006E 2004          LAC   DRCV1       move receive data to transit
0257 006F 5006          SACL  DXMT1       registers.
0258 0070 2005          LAC   DRCV2
0259 0071 5007          SACL  DXMT2
0260 0072 4906          OUT   DXMT1,PA1   write first transmit byte to
0261                    *                 transmit buffer.
0262 0073 7F89          ZAC
0263 0074 5003          SACL  RXEFLG      clear rcv/xmit-end flag.
0264 0075 F900          B     DLB
     0076 006B
0265 0077
```

```
                 ***************************************************************
                 *  ==================================                         *
                 *      Normal interrupt routines.                             *
                 *  ==================================                         *
                 *                                                             *
                 *  These routines destroy the contents of the accumulator     *
                 *  and the data page pointer, making it necessary to save     *
                 *  these before the routines begin.                           *
                 *                                                             *
                 *  Write the contents of DXMT2 to the transmit buffer and     *
                 *  read the receive buffer into DRCV1.                        *
                 *                                                             *
                 ***************************************************************
0077
0077 4907  NINT1  OUT   DXMT2,PA1  write xmit-low to xmit register.
0078 4104         IN    DRCV1,PA1  read rcv-data-high from rcv reg.
0079 200C         LAC   ANINT2     prepare next interrupt vector.
007A 500A         SACL  VECT
007B 4813         OUT   CLRX,PA0   clear xmit interrupt flag.
007C 7F8D         RET
007D 4105  NINT2  IN    DRCV2,PA1  read receive-data-low from rcv reg.
007E 200B         LAC   ANINT1     prepare next interrupt vector.
007F 500A         SACL  VECT
0080 4813         OUT   CLRX,PA0   clear xmit interrupt flag.
0081 7EFF         LACK  FLAG
0082 5003         SACL  RXEFLG     set xmit/rcv end flag.
0083 7F8D         RET
                 ***************************************************************
                 *  ========================================                   *
                 *      Secondary interrupt routines                           *
                 *  ========================================                   *
                 *  These routines destroy the contents of the accumulator     *
                 *  and the data page pointer.                                 *
                 *                                                             *
                 *  The following routines write the low byte of the primary*
                 *  data word and the high and low byte of the secondary       *
                 *  data word. They also read the A/D information from         *
                 *  the receive registers.                                     *
                 ***************************************************************
0084 4907  SINT1  OUT   DXMT2,PA1  write xmit-data-low to xmit reg.
0085 4104         IN    DRCV1,PA1  read receive-data-high from rcv reg.
0086 200E         LAC   ASINT2     prepare next interrupt vector.
0087 500A         SACL  VECT
0088 4813         OUT   CLRX,PA0   clear xmit interrupt flag.
0089 7F8D         RET
008A 4908  SINT2  OUT   DXMT3,PA1  write secondary-data-high to xmit.
008B 4105         IN    DRCV2,PA1  read receive-data-low from rcv.
008C 200F         LAC   ASINT3     prepare next interrupt vector.
008D 500A         SACL  VECT
008E 4813         OUT   CLRX,PA0   clear xmit interrupt flag.
008F 7F8D         RET
0090 4909  SINT3  OUT   DXMT4,PA1  write secondary-data-low to xmit.
0091 2010         LAC   ASINT4     prepare next interrupt vector.
0092 500A         SACL  VECT
0093 4813         OUT   CLRX,PA0   clear xmit interrupt flag.
```

```
0321 0094 7F8D          RET
0322 0095 200B  SINT4   LAC   ANINT1      prepare next interrupt vector.
0323 0096 500A          SACL  VECT
0324 0097 4813          OUT   CLRX,PA0    clear xmit interrupt flag.
0325 0098 7F89          ZAC
0326 0099 5007          SACL  DXMT2       clear DXMT2 immediately to eliminate
0327 009A 7EFF          LACK  FLAG        unnexpected secondary communications
0328 009B 5003          SACL  RXEFLG      set xmit/rcv end flag.
0329 009C 7F8D          RET
0330             ****************************************************************
0331             *  ===========================                                 *
0332             *  Ignore first interrupt.                                      *
0333             *  ===========================                                 *
0334             *     This routine is used to ignore the first data trans-      *
0335             *  mission and also to synchronize the AIC with the            *
0336             *  processor.                                                   *
0337             ****************************************************************
0338 009D 200B  IGN     LAC   ANINT1
0339 009E 500A          SACL  VECT
0340 009F 4813          OUT   CLRX,0
0341 00A0 7F8D          RET
0342             ****************************************************************
0343             *                                                              *
0344             *    CONTROL REGISTER INFORMATION                              *
0345             *                                                              *
0346             *      SERIAL-PORT CONFIG.     INT. MASK   INT. FLAG           *
0347             *    | 1  0  0 0  1  1  1  0| 0  0  0  1| 0  1  0  0|          *
0348             *     15 14 13 12 11 10  9  8  7  6  5 4  3  2  1  0           *
0349             *                       |                  |  |  |  |_INT     *
0350             *                       |_XF status        |  |  |____FSR     *
0351             *                                          |  |_______FSX     *
0352             *                                          |__________FR      *
0353             *                                                              *
0354             *                                    (write 1's to clear)      *
0355             ****************************************************************
0356 00A1 8E1F  CLX1    DATA  >8E1F
0357 00A2 8E0F  CLX2    DATA  >8E0F
0358                    END
NO ERRORS, NO WARNINGS
```

```
0317 009D 200B  IGN    LAC   ANINT1
0318 009E 500A         SACL  VECT
0319 009F 4813         OUT   CLRX,0
0320 00A0 7F8D         RET
0321            ****************************************************************
0322            *                                                              *
0323            *    CONTROL REGISTER INFORMATION                              *
0324            *                                                              *
0325            *      SERIAL-PORT CONFIG.     INT. MASK   INT. FLAG           *
0326            *    | 1  0  0 0  1  1  1  0| 0  0  0  1| 0  1  0  0|          *
0327            *     15 14 13 12 11 10  9  8  7  6  5 4  3  2  1  0          *
0328            *                       |                    |  |  |  |_INT    *
0329            *                       |_XF status          |  |  |____FSR    *
0330            *                                            |  |_______FSX    *
0331            *                                            |__________FR     *
0332            *                                                              *
0333            *                                    (write 1's to clear)      *
0334            ****************************************************************
0335 00A1 8E1F  CLX1   DATA  >8E1F
0336 00A2 8E0F  CLX2   DATA  >8E0F
0337                   END
NO ERRORS, NO WARNINGS
```

Implementation of a 1280 × 1024 × 8 Display Using the TLC34075 Video Interface Palette

By
Robert Milhaupt, Jeffrey Nye, and John Yin

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1 INTRODUCTION

The TLC34075 Video Interface Palette (VIP) achieves a new level of video system integration by incorporating in a single device logic typically implemented with 20 to 30 integrated circuits. The TLC34075 contains programmable video shift registers, VGA pass-through logic, VRAM control circuitry, video sync and blank control, a voltage reference, dot clock multiplexers, monitor detection circuitry, a true color pipeline with overlay, a 256-entry 24-bit-wide palette RAM, a VGA-compatible register set, and frame buffer test circuitry. The feature set of the TLC34075 is designed to provide maximum flexibility to the designer so that the resulting system can support an extremely broad applications base. The high level of integration enables very low chip count designs and makes large amounts of board space available for product differentiation.

This application report details a graphics design capable of resolutions up to 1280 by 1024 by 8. The design utilizes a 110-MHz TLC34075 and a 40-MHz TMS34020A. The discussion herein includes the local-bus interface and back-end implementation. Since this design is independent of the host bus, the host interface is left as an exercise to the reader. The hardware described in this application report has been built and tested in a laboratory environment.

2 FEATURE SET DESCRIPTION

This section briefly outlines the features found in the TLC34075 and those found in the design implementation.

2.1 TLC34075 Feature Set

- RS-343A-Compatible Outputs (RGB)
- Programmable Sync Pedestal
- Sync on Green
- Separate TTL-Compatible Sync With Polarity Control
- Programmable Pixel Depth:
  1, 2, 4, 8, or 24+8 bits per pixel
- Programmable Pixel Bus Width:
  4, 8, 16, or 32 bits wide
- VGA Compatible Register Set
- VGA Pass-Through Port
- On-Chip Voltage Reference
- 4/5 Input Dot Clock Multiplexer
- Split Shift Register Transfer SCLK Pulse Generation
- Monitor Detection
- Palette Paging Register

2.2 Design Features

- Supports several programmable resolutions and pixel depths including:
  - 1280 by 1024 (1, 2, 4, or 8 bits per pixel) noninterlaced (discussed)
  - 1024 by 768 (1, 2, 4, or 8 bits per pixel) noninterlaced (not discussed)†
  - 640 by 480 (1, 2, 4, or 8 bits per pixel) noninterlaced (discussed)
  - 512 by 512 (1, 2, 4, 8, or 32 bits per pixel) noninterlaced (not discussed)†
- 2M bytes of zero-wait-state VRAM (TMS44C251-10)
- 1M bytes of zero-wait-state DRAM (TMS44C256-10)

† Resolutions not discussed herein will be addressed in future application notes.

3 RELATED DOCUMENTATION

Following is a partial list of literature pertinent to the design described in this article.

- TMS34020 User's Guide (SPVU019)
- TMS34020, TMS34020A Data Sheet (SPUS004B)
- TLC34075 Data Manual (SLAS043)
- MOS Memory Data Book (SMYD091)
- 340 Family Graphics Library User's Guide (SPVU027)
- 340 Family Code Generation Tools User's Guide (SPVU020A)
- TIGA Interface User's Guide, Rev 2.0 (SPVU015B)

4 DESIGN DESCRIPTION

The system block diagram is shown in Figure 1. The LAD bus is a 32-bit multiplexed address and data path used as the local bus in this design. All peripherals accessible to the TMS34020A are linked via this bus. The LAD bus is also used by the decoder logic to enable access to these peripherals.

The RCA bus is the RAM address bus used directly by the VRAM and DRAM banks. This bus, an important feature of the TMS34020A, eliminates the need for external row and column address multiplexers.

The three-state PXD bus is a 64-bit pixel data path multiplexed to 32 bits. It is used to bring pixel data into the TLC34075. Control of the PXD data bus is shared by the TMS34020A, which performs memory-to-shift-register transfer cycles based on VCLK, the TLC34075, which provides the SCLK and the VCLK signals, and the RASDCD (U5) decoder, which performs the three-state multiplexing function by enabling the SOE pin of the proper VRAM bank.

VCLK is the synchronizing clock used by the TMS34020A to determine when to assert video sync and blank signals and when to perform the next memory-to-shift-register transfer cycle for screen refresh. The frequency of VCLK is adjustable via a register in the TLC34075 and is typically a submultiple of the dot clock.

SCLK is the VRAM shift clock used to move the next pixel data to the serial output port of the VRAM; this pixel data is subsequently captured by the input latch of the TLC34075. The frequency of SCLK is adjustable via a register in the TLC34075 and is always related to the number of pixels available at the pixel input to the TLC34075. For example, the combination of a 4-bit pixel and a 32-bit-wide PXD bus requires that the SCLK frequency is one eighth of the dot clock frequency because 8 pixels are obtained with every SCLK pulse.

Two latches and two decoder devices are used to configure the memory map and control access to the peripherals on the local bus.

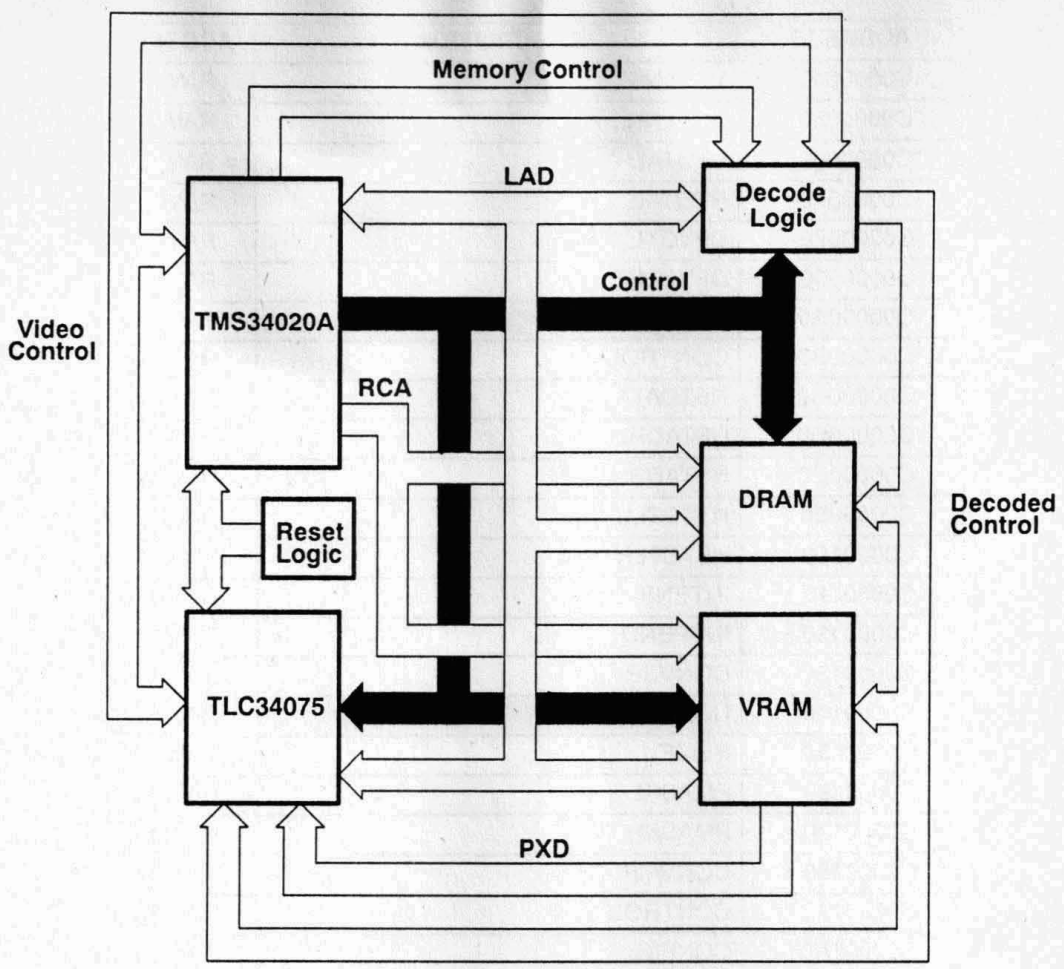

Figure 1. System Block Diagram

The RESET (U38) PAL® provides a controlled reset pulse to the TMS34020A and to the TLC34075 reset generation circuitry.

4.1 Memory Map

The memory map of this design is summarized in the table below.

ADDRESS	DESCRIPTION	ACCESS
00000000	Start of VRAM Bank 0	R/W:32
00800000	Start of VRAM Bank 1	R/W:32
01000000	Start of DRAM Bank 0	R/W:32
017FFFFF	End of DRAM Bank 0	------
---------	TMS34020A I/O Registers	------
C0000000	VESYNC	R/W:16
C0000010	HESYNC	R/W:16
C0000020	VEBLNK	R/W:16
C0000030	HEBLNK	R/W:16

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ADDRESS	DESCRIPTION	ACCESS
C0000040	VSBLNK	R/W:16
C0000050	HSBLNK	R/W:16
C0000060	VTOTAL	R/W:16
C0000070	HTOTAL	R/W:16
C0000080	DPYCTL	R/W:16
C0000090	DPYSTRT	R/W:16
C00000A0	DPYINT	R/W:16
C00000B0	CONTROL	R/W:16
C00000C0	HSTDATA	R/W:16
C00000D0	HSTADRL	R/W:16
C00000E0	HSTADRH	R/W:16
C00000F0	HSTCTLL	R/W:16
C0000100	HSTCTLH	R/W:16
C0000110	INTENB	R/W:16
C0000120	INTPEND	R/W:16
C0000130	CONVSP	R/W:16
C0000140	CONVDP	R/W:16
C0000150	PSIZE	R/W:16
C0000160	PMASKL	R/W:16
C0000170	PMASKH	R/W:16
C0000180	CONVMP	R/W:16
C0000190	CONTROL	R/W:16
C00001A0	CONFIG	R/W:16
C00001B0	DPYTAP	R/W:16
C00001C0	VCOUNT	R/W:16
C00001D0	HCOUNT	R/W:16
C00001E0	DPYADR	R/W:16
C00001F0	REFADR	R/W:16
C0000200	DPYSTL	R/W:16
C0000210	DPYSTH	R/W:16
C0000220	DPYNXL	R/W:16
C0000230	DPYNXH	R/W:16
C0000240	DINCL	R/W:16
C0000250	DINCH	R/W:16
C0000260	Reserved	------
C0000270	HESERR	R/W:16
C0000280	Reserved	------
C0000290	Reserved	------
C00002A0	Reserved	------
C00002B0	Reserved	------
C00002C0	SCOUNT	R/W:16
C00002D0	BSFLTST	R:16
C00002E0	DPYMSK	R/W:16
C00002F0	Reserved	------

ADDRESS	DESCRIPTION	ACCESS
C0000300	SETVCNT	R/W:16
C0000310	SETHCNT	R/W:16
C0000320	BSFLTDL	R:16
C0000330	BSFLTDH	R:16
C0000340	Reserved	-----
C0000350	Reserved	-----
C0000360	Reserved	-----
C0000370	Reserved	-----
C0000380	IHOST1L	R:16
C0000390	IHOST1H	R:16
C00003A0	IHOST2L	R:16
C00003B0	IHOST2H	R:16
C00003C0	IHOST3L	R:16
C00003D0	IHOST3H	R:16
C00003E0	IHOST4L	R:16
C00003F0	IHOST4H	R:16
----------	End of TMS34020A I/O Register Set	-----
----------	Beginning of TLC34075 Register Set	-----
D0000000	Write Mode Address Register	R/W:8
D0000020	Palette Holding Register	R/W:8
D0000040	Read Mask Register	R/W:8
D0000060	Read Mode Address Register	R/W:8
D0000080	Reserved	-----
D00000A0	Reserved	-----
D00000C0	Reserved	-----
D00000E0	Reserved	-----
D0000100	General Control Register	R/W:8
D0000120	Input Clock Register	R/W:8
D0000140	Output Clock Register	R/W:8
D0000160	MUX Control Register	R/W:8
D0000180	Palette Page Register	R/W:8
D00001A0	Reserved	-----
D00001C0	Test Register	R/W:8
D00001E0	Reset State	R/W:8
----------	End of TLC34075 Register Set	------
FF800000	Beginning of shadow of DRAM Bank 0	R/W:32
FFF00000	TMS34020A Interrupt and Trap Vectors	R/W:32
FFFFFFFF	End of Interrupt and Trap Vectors and shadow of DRAM Bank 0	------

4.1.1 Memory Map Decoding

The memory map previously shown is decoded by the RASDCD (U5) PAL. A RAS-banking method is used. The RASDCD (U5) PAL provides bank decoding based on the URAS output from the TMS34020A and the latched address information provided by the SN74AS841 (U3) address latch. The RAS0, RAS1, and RAS2 signals are used to drive the RAS input signals of VRAM bank 0, VRAM bank 1, and the DRAM

bank, respectively. The RAS2 output of the RASDCD (U5) PAL is also decoded to map the DRAM into the address range of the TMS34020A's interrupt and trap vectors. Because the TMS34020A's interrupt and trap vectors are stored at the end of the shadow of DRAM bank 0, program memory space in DRAM must not use upper locations of DRAM. The RASDCD (U5) PAL also provides a chip select signal, PALETEN, which is generated for the TLC34075. Because incomplete address decoding is used, all banks are aliased throughout memory space; the memory map only shows the suggested memory usage and the shadowing of DRAM bank 0.

The video RAM RAS signals are not based solely on address. The TMS34020A provides two special bus cycles during which both banks of video RAM should be activated:

- the load-write-mask cycle: used to write-protect bit planes within the video RAM.
- the load-color-register cycle: copies the color value from the TMS34020A COLOR1 register into the video RAM color register. The color register data is then used during block-write cycles; this is useful for bulk initialization of memory or for fast screen clearing.

During either a load-write-mask cycle or a load-color-register cycle, the TMS34020A zeroes the LAD bus during the address portion of the cycle and zeroes the RCA bus for both the row and column portions of the cycle. If these cycles were not special-cased, only video RAM bank 0 would act on these cycles, as it is mapped to address zero. The RAS2 signal is not asserted during these cycles since the TMS44C256 DRAM does not support these cycles.

4.1.2 Mapping the TLC34075 Into TMS34020A Memory Space

The TLC34075 implements a VGA-compatible register set that uses an 8-bit data bus. Since the TMS34020A's LAD bus is 32 bits wide, it is convenient to map the TLC34075 into the TMS34020A's memory space as a 32-bit-wide device, ignoring the upper 24 bits of data.

The TLC34075 chip-select signal ($\overline{\text{PALETEN}}$) generated by the RASDCD (U5) PAL is used by the LTCHDCD (U4) PAL to generate read and write strobes to the TLC34075. The TLC34075's write signal ($\overline{\text{WR}}$) is driven low when $\overline{\text{PALETEN}}$ is low and $\overline{\text{WE}}$ is low. The TLC34075's $\overline{\text{RD}}$ input is driven low when PALETEN is low, $\overline{\text{WE}}$ is high, and $\overline{\text{TR}}/\overline{\text{QE}}$ is low ($\overline{\text{TR}}/\overline{\text{QE}}$, while not strictly required, provides symmetrical timing for $\overline{\text{RD}}$ and $\overline{\text{WR}}$ assertion). The four register select inputs of the TLC34075 are connected to the four latched address bits: LDAT8, LDAT7, LDAT6, and LDAT5. This imposes several constraints on the software operation of the system. When reading values from the TLC34075's registers, only the lower 8 bits of a 32-bit, long-word-aligned memory access are valid. Similarly, a 32-bit-wide write to a 32-bit word-aligned address of a TLC34075 register only uses the lower 8 bits of data. It is safest to access the TLC34075 with 8-bit reads and writes to long-word-aligned addresses as shown in the memory map.

4.1.3 Address Latching

The address latches, the LTCHDCD (U4) PAL, and the SN74AS841 (U3) latch generate latched address information for the memory decoder PAL and the TLC34075. The memory decoder PAL requires latched address bits 31-28, 24-23, and status bits 3-0, and the TLC34075 uses latched address bits 8-5. The LTCHDCD (U4) PAL uses internal feedback to implement a transparent latch. In addition, it forces latched address bits 8-5 high during reset, as described in Section 4.5.

4.2 Frame Buffer Organization

Frame buffer memory in 1280-by-1024-by-8 systems is typically implemented with either "packed" or "unpacked" scan lines. While the unpacked scan line method is the simpler hardware implementation, it causes poor memory utilization, as memory fragments not used for pixel data appear at the end of each scan line. The packed scan line implementation utilizes frame buffer memory efficiently, as all memory not used

for pixel data appears in a contiguous block at the end of the frame buffer. Prior to availability of the TLC34075, implementing a 1280-by-1024 packed frame buffer for a TMS340-based system has been complex. The architecture of the TLC34075 removes virtually all of that complexity.

The following discussion deals with the tradeoffs associated with unpacked- versus packed-frame buffer memories in TMS340 designs. As background to the discussion, the first section deals with the operation of the TMS34020A memory controller regarding shift register transfer cycles.

4.2.1 TMS34020A Shift Register Transfer Operation

When the graphics system is ready to display valid video data, the screen refresh enable bit of the display control I/O register (SRE [DPYCTL]) is set to one by system software. At this time, the video timing logic of the TMS34020A begins scheduling VRAM shift register transfer cycles (also called serial register transfers, memory-to-register transfers, screen refresh cycles, or SRTs). The TMS34020A supports two types of SRTs: those that occur during the horizontal blanking interval and those that occur during the active display time. SRTs that occur during active display time (midline reload cycles) are not required for this design.

The TMS44C251 video RAM supports two types of shift register transfer: a normal shift register transfer (SRT) that transfers one whole RAM array row into the VRAM's serial shift register and a split shift register transfer (SSRT) that transfers one half of a RAM array row to one half of the VRAM's serial shift register. The TMS34020A supports both types. Unless the SRT bit of the DPYCTL (0xC0000080) register is set to one, the TMS34020A only performs normal SRTs. If the SRT bit is set, the TMS34020A schedules, at the beginning of blanking, an SRT immediately followed by a SSRT. Additional SSRTs may be scheduled by the TMS34020A during the active portion of the scan line if the SCLK input of the TMS34020A is cycling and the TMS34020A determines that the serial shift register is nearly empty. If split shift register transfers are not needed during the active portion of the scan line, the TMS34020A's SCLK input should be tied to ground. Although the application described herein uses split shift register transfers, it does not require SSRTs during the active portion of the scan line but only during blanking. Therefore, in this application, the TMS34020A's SCLK input is tied to ground.

At the onset of the horizontal blanking period for a scan line, the TMS34020A memory controller schedules an SRT cycle to occur during the blanking interval. The SRT cycle instructs the VRAM to copy pixel data from a row of its RAM array into its serial shift register. An example of an SRT cycle is shown in Figure 2.

For applications in which a pixel data scan line wraps from one RAM row to the next row rather than being contained in a single RAM row, a split shift register transfer (SSRT) cycle is used to copy the scan line from the RAM into the serial shift register. As shown in Figure 4, packed scan line implementation results in numerous instances of scan lines wrapping from one RAM row to the next. Hence, SSRTs are used in systems that employ packed scan line frame buffers.

4.2.2 Packed and Unpacked Frame Buffers

The amount of memory required for a 1280-by-1024-by-8 frame buffer depends on whether a packed or unpacked implementation is chosen. In a packed implementation, the scan line pixel data are stored contiguously in the frame buffer (i.e, the last pixel of a scan line is followed immediately by the first pixel of the next scan line; there are no unused bits between scan lines). Therefore, the pitch of the pixel information (the difference in storage addresses for vertically adjacent pixels) equals the amount of memory required to store one pixel data scan line (in this case, 1280 pixels/line times 8 bits/pixel, or 10240 bits). A minimum of 1.25M bytes of memory is required to implement a 1280-by-1024-by-8 packed frame buffer (1280 bytes/line × 1024 lines).

In an unpacked frame buffer implementation, the pitch of the pixel data is typically chosen to be the power of two that is greater than or equal to the amount of memory required to store one pixel data scan line. For

example, a 1280-by-1024-by-8 unpacked frame buffer (one scan line requires 10240 storage bits) would typically employ a pitch of 16384 bits, which is the first power of two greater than the 10240 bits required for one scan line. Therefore, a minimum of 2.1M bytes of memory is required to implement a 1280-by-1024-by-8 unpacked frame buffer (2048 bytes/line × 1024 lines).

Each system has both advantages and disadvantages:

FRAME BUFFER TYPE	ADVANTAGE	DISADVANTAGE
Unpacked	May not require split shift register transfers	Typically fragments unused frame buffer memory
Packed	Does not fragment unused frame buffer memory	Typically requires split shift register transfers

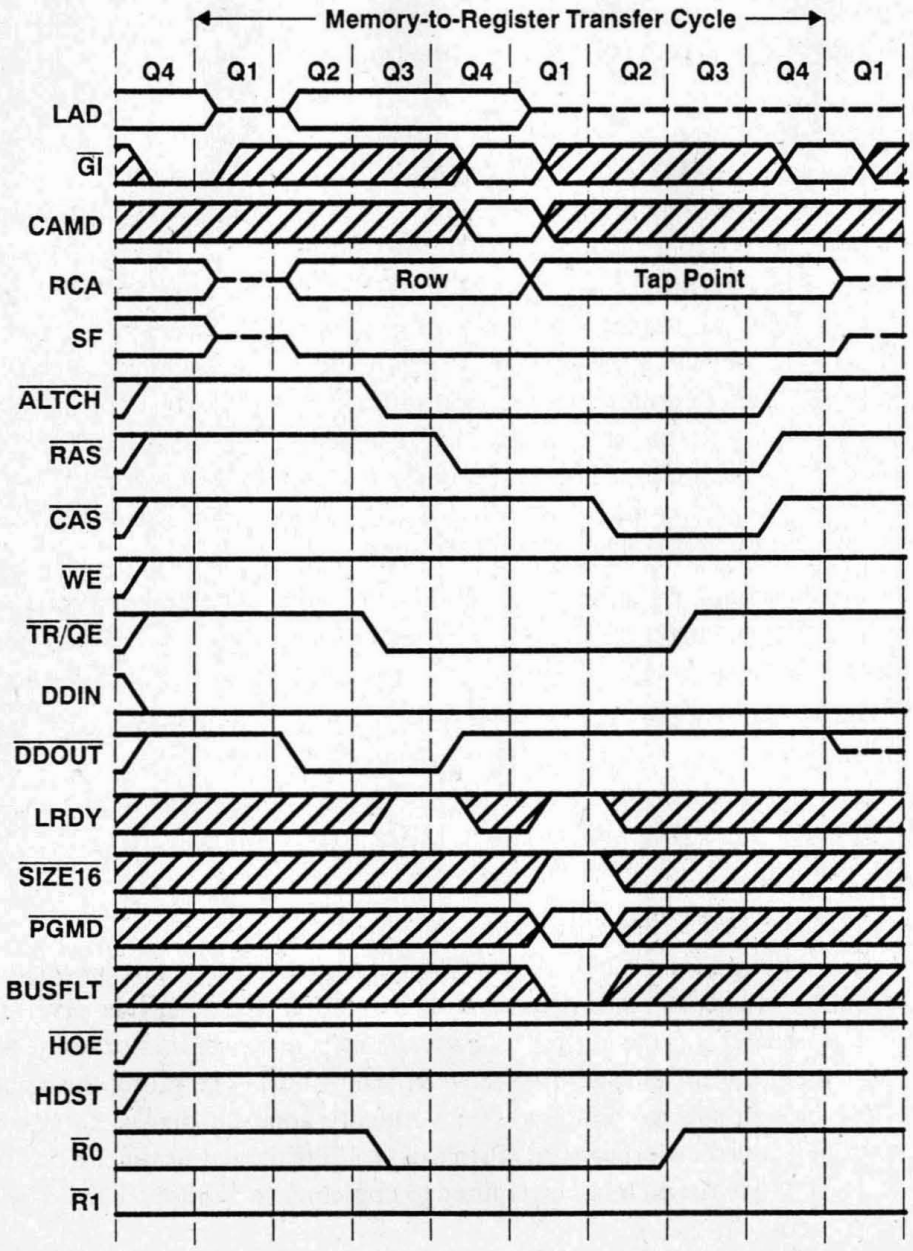

Figure 2. Shift Register Transfer Cycle

Figures 3 and 4 show the memory organization for unpacked and packed frame buffers, respectively, for a 1280-by-1024-by-8 display..

VRAM Bank	RAM Array Row		
0	0	Scan Line 0	Unused
0	1	Scan Line 1	Unused
0	2	Scan Line 2	Unused
0	3	Scan Line 3	Unused
0	4	Scan Line 4	Unused
0	5	Scan Line 5	Unused
⋮	⋮	⋮	
0	509	Scan Line 509	Unused
0	510	Scan Line 510	Unused
0	511	Scan Line 511	Unused
1	0	Scan Line 512	Unused
1	1	Scan Line 513	Unused
1	2	Scan Line 514	Unused
1	3	Scan Line 515	Unused
⋮	⋮	⋮	
1	509	Scan Line 1021	Unused
1	510	Scan Line 1022	Unused
1	511	Scan Line 1023	Unused

Figure 3. Unpacked 1280-by-1024-by-8 Display Memory

In implementing a 1280-by-1024-by-8 unpacked frame buffer, no split shift register transfers are needed, as no scan line crosses a VRAM array row boundary. The packed frame buffer organization does span scan line information across VRAM array row boundaries and, therefore, requires split shift register transfers.

Note that, in both the packed and unpacked systems, the first scan line in the second bank of VRAM is aligned with the beginning of the first row of the bank. This is necessary, as switching between banks of VRAM during the scan line would be extremely difficult to synchronize. Consider the last SRT in the first bank of VRAM for the packed frame buffer. If the last SRT in VRAM bank 0 only gets a portion of the data for the scan line, the SSRT will address the beginning of the second bank of VRAM. Since the SSRT occurs during blanking, there is no way to determine when to change from VRAM bank 0 driving the PXD bus to VRAM bank 1 driving the PXD bus. (There is no method by which data from the RAM array of one bank of VRAM may be transferred into the serial shift register of the other VRAM bank using SRTs or SSRTs.) Since the TMS34020A requires that the display pitch must be constant throughout the display, the packed frame buffer implementation requires that the first scan line in VRAM bank 0 be offset from the beginning of the bank as shown in Figure 4. The starting point chosen in Figure 4 stores the maximum amount of the

frame buffer in VRAM bank 0 while placing the first pixel of a scan line at the beginning of VRAM bank 1. For other resolutions and pixel depths in which the frame buffer spans more than one VRAM bank, and when implementing multiple-page frame buffers, the starting address of the frame buffer must be chosen similarly.

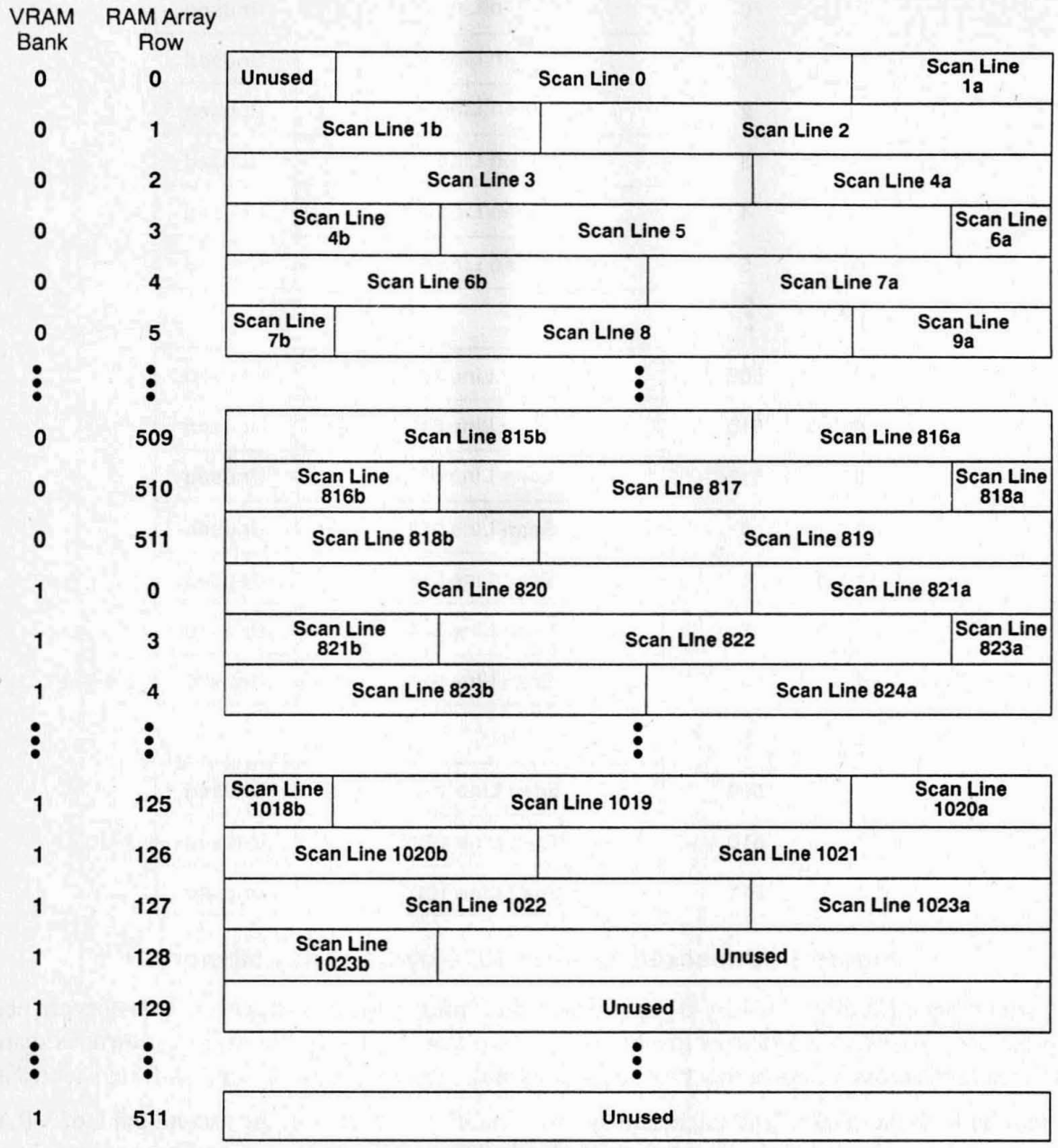

Figure 4. Packed 1280-by-1024-by-8 Display Memory

4.2.3 Split Shift Register Transfers

When using split shift register transfers (for VRAMs that support this feature), the VRAM shift register is split in half. A split shift register transfer cycle specifies which half of the shift register is to be loaded from which RAM array row. The data loaded into the shift register half-row comes from the RAM array row specified at row address time (when RAS is low). The most significant bit of the column address determines which half of the shift register is loaded, and all other column address bits hold the least significant bits of the tap address. If the most significant bit of the column address is a zero, then the lower

(least significant) half of the RAM array row is loaded into the lower half of the shift register; if the most significant bit of the column address is a one, then the upper (most significant) half of the RAM array row is loaded into the upper half of the shift register.

In generating screen refresh cycles, the TMS34020A determines whether split shift register transfers should be used based on the value of the SSV (enable split-serial-register midline reload) bit in its DPYCTL register. If the SSV bit is set to one, the TMS34020A performs an SRT with a row address and tap point followed by an SSRT with a full row address and a half-row address during the column address subcycle. The SSRT replaces one half of the data transferred into the shift register during the SRT. It is important to note that the VRAM's SCLK input must cycle at least once between the SRT and the SSRT in order to transfer the tap point sent during the SRT between the VRAM internal tap point latch and the VRAM internal tap point counter. Since this SCLK loads data into the shift register from the RAM array, it is effectively the first SCLK pulse for the display line, and the pixel data that the VRAMs present at their serial outputs must be displayed before the next SCLK pulse. Figures 5 and 6 show the pertinent signals during horizontal blanking for systems without and with split shift register transfers, respectively. The $\overline{\text{BLANK}}$ signal shown is the TLC34075's internal blanking signal, which is delayed by an amount equal to the internal pixel pipeline delay.

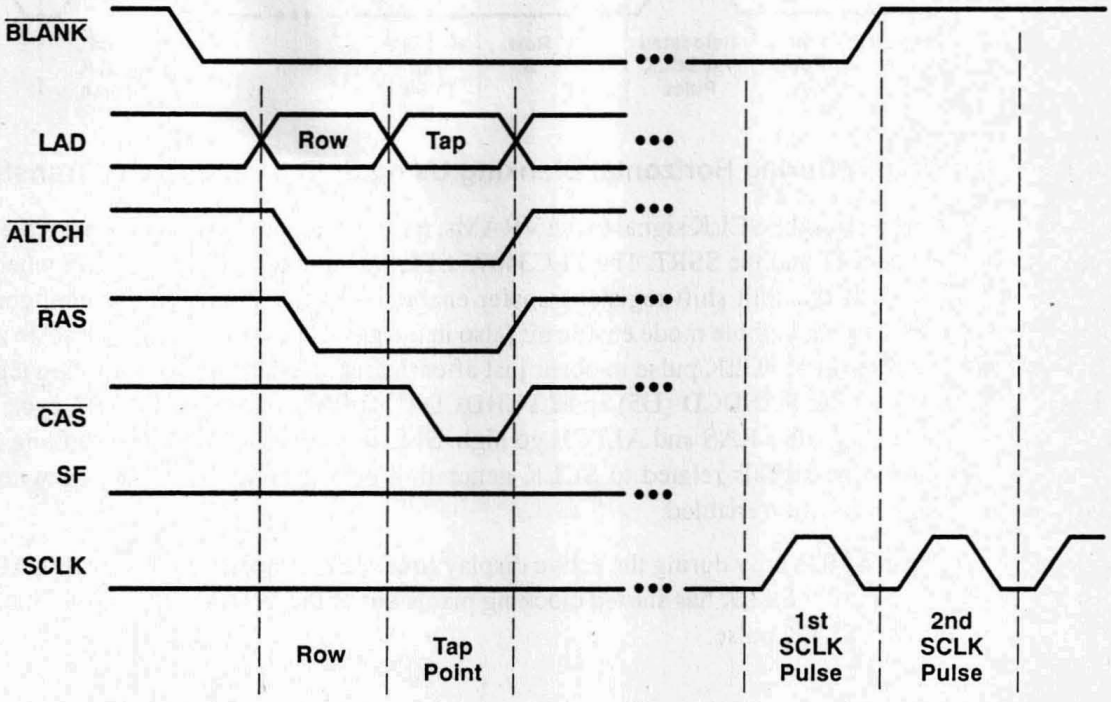

Figure 5. SRT Signals During Horizontal Blanking Without Split Shift Register Transfers

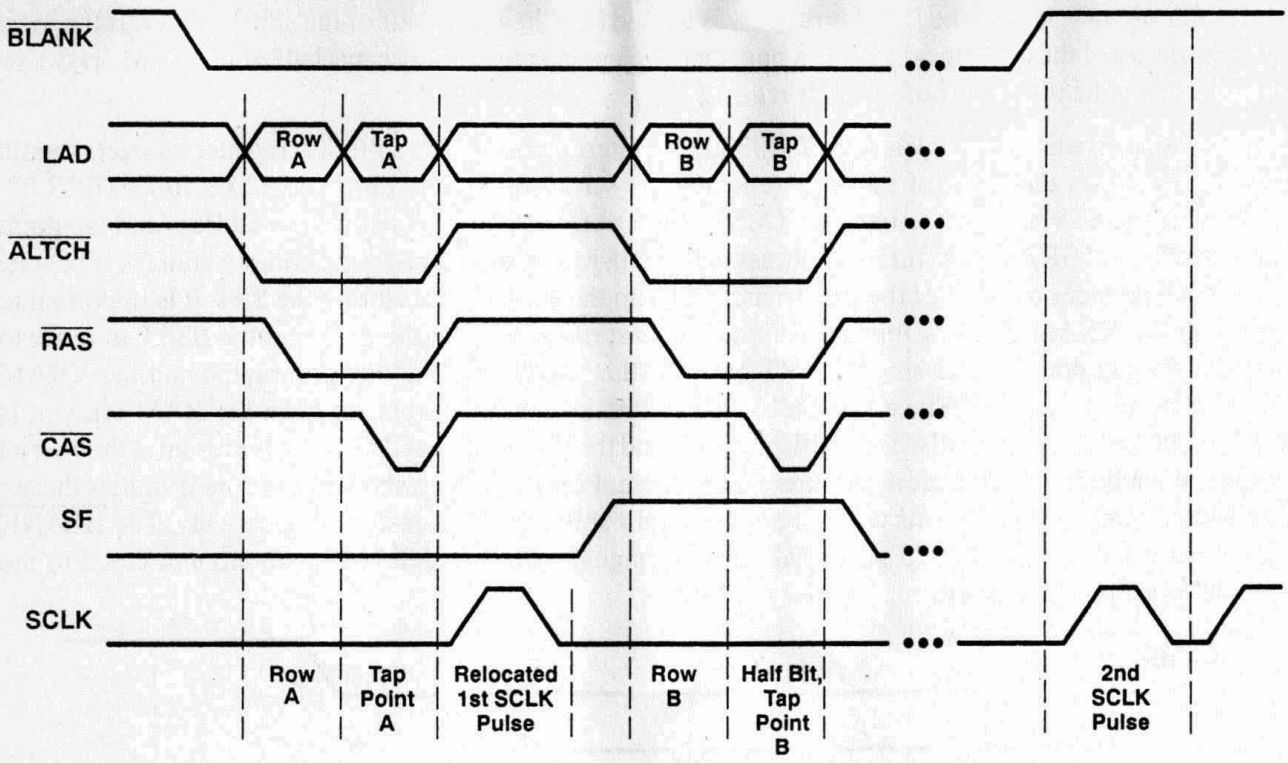

Figure 6. SRT Signals During Horizontal Blanking Using Split Shift Register Transfers

Since the TLC34075 generates the SCLK signal to the VRAMs, it is convenient to allow it to insert the first SCLK pulse between the SRT and the SSRT. The TLC34075 SFLAG input tells the TLC34075 when the first SRT has completed. If the split shift register transfer enable bit in the TLC34075 general control register is set to 1 and the special nibble mode enable bit (also in the general control register) is set to zero, the TLC34075 relocates the first SCLK pulse to occur just after the rising edge of SFLAG following the SRT. External circuitry (in the RASDCD (U5) and LTCHDCD (U4) PALs) decodes the SRT cycle and drives the SFLAG input high after RAS and ALTCH go high. SFLAG is driven low when blanking goes inactive. Figure 7 shows the signals related to SCLK generation during horizontal blanking with the TLC34075 SCLK pulse relocation enabled.

For systems that perform SSRTs only during the active display time, there is no need to assert SFLAG. In this case, the SSRTs occur after SCLK has started clocking pixels out of the VRAM. The tap point of the SRT is latched by the first SCLK pulse.

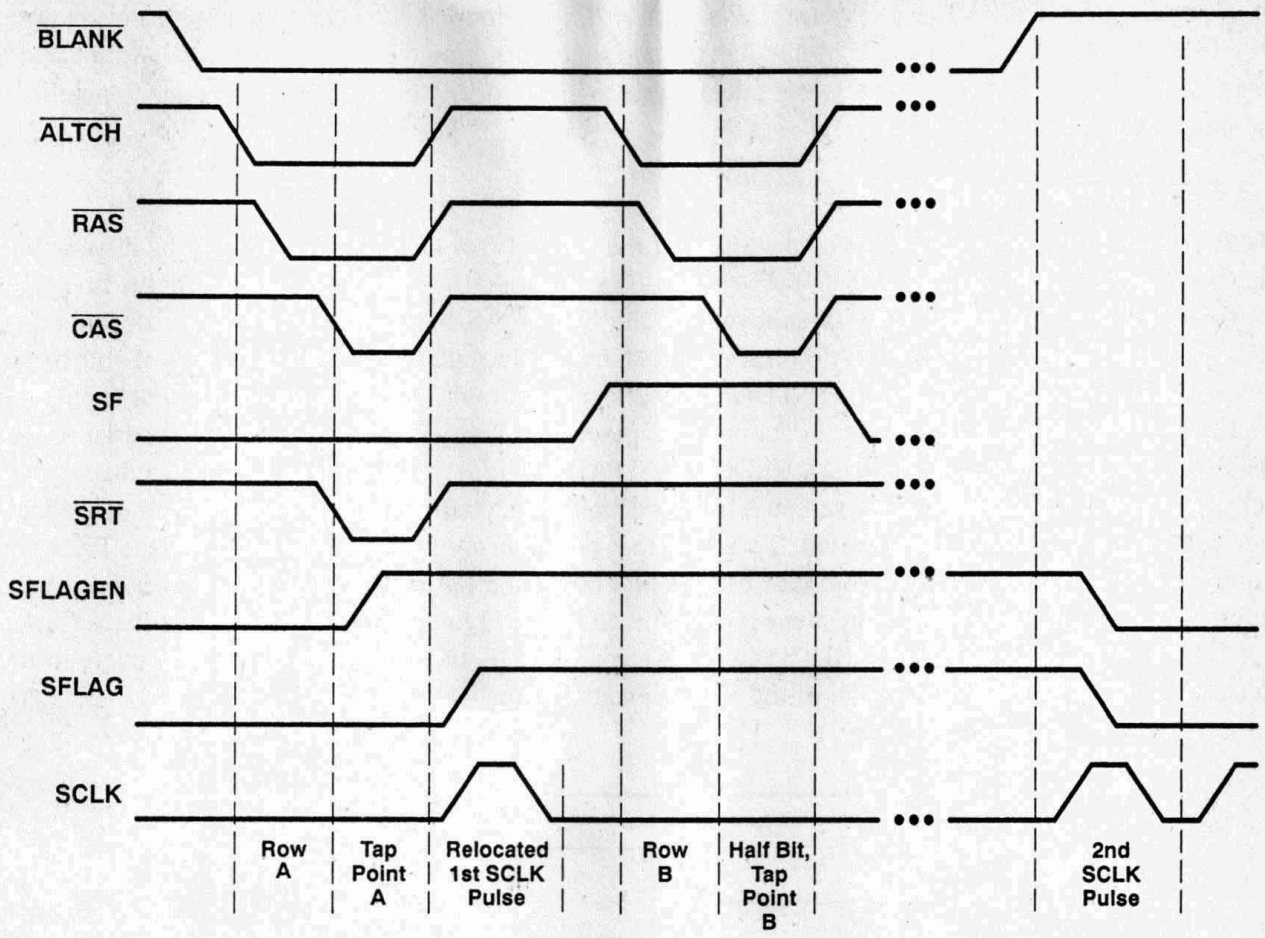

Figure 7. SCLK Pulse Between SRT and SSRT and Related Signals

4.2.4 Packed Displays and TMS34020A Screen Refresh Latency

In certain display configurations, it is not possible to employ screen organizations that require the use of SSRTs. This problem stems from the set time between the start of horizontal blanking and the TMS34020A-generated screen refresh cycles (the scheduling of screen refresh cycles is discussed in the TMS34020 User's Guide) and the amount of pixel pipeline delay. In systems for which the minimum screen refresh latency times two is less than the SCLK period, an SRT may occur while the palette is still pushing pixels through its pipeline. In this situation, SCLK may be high at the time when the relocated SCLK pulse should be inserted. Because the VRAM sees no rising edge on SCLK, it does not accept the tap point presented during the SRT, giving an improper image on the screen. Avoid using packed frame buffers for displays with low pixel sizes (number of bits per pixel) and low dot clock frequencies. At one and two bits per pixel, the noninterlaced 640-by-480 SCLK period is greater than two times the screen refresh latency, suggesting that these configurations should be implemented as unpacked frame buffers. Note that the situation wherein the SCLK period is greater than two times the TMS34020A's minimum screen refresh latency corresponds to a display that requires a relatively small frame buffer; this typically eliminates the need for packed frame buffer implementation.

There may be occasions when, even if two times the minimum screen refresh latency time is less than the SCLK period, it is necessary to implement a packed display organization. In systems with a set screen refresh latency, it may be possible to delay the SRT. In TMS34020A-based systems, the SRT can be wait-stated until SCLK falls. As an example, in a TMS34020A-based system, the SRT cycle could be wait-stated until SCLK falls using the LRDY signal of the TMS34020A.

In systems with a user-defined screen refresh latency, this latency should be set to be greater than the worst-case pixel pipeline delay but shorter than the horizontal blanking width. Consider all possible factors when determining the latency setting (e.g., delays due to high-priority bus cycles, delays due to pipelined memory accesses, etc.).

4.2.5 Multiplexing the PXD Bus

During an SRT, the RCA bus carries the address of the VRAM row and the tap point for the display line data but does not distinguish between VRAM banks. Since the LAD bus carries the address of the first pixel of a display line during the address subcycle of the SRT, RAS banking is in effect as described in Section 4.1.1. Only one bank of VRAM receives a RAS cycle. Because the serial data outputs of both banks of VRAM are tied to the 32-bit-wide PXD bus, the serial data outputs must be three-stated so that only the appropriate VRAM bank drives pixel data onto the pixel bus. The VRAMs each provide a serial output enable pin (SOE) for this purpose. The RASDCD (U5) PAL provides two outputs to drive these enable pins: SOE0 and SOE1. The address of the screen refresh is decoded and, during the tap point subcycle of the SRT, the appropriate SOE output is asserted. To assure that both banks of VRAM do not drive the PXD bus simultaneously when switching from one bank to the other, the RASDCD (U5) PAL forces both SOE outputs inactive during the row address subcycle of the SRT (see Figures 8 and 9). Internal feedback is used to latch the SOE outputs. The RASDCD (U5) PAL also signals the beginning of an SRT cycle to the LTCHDCD (U4) PAL for generation of the SFLAG signal to the TLC34075.

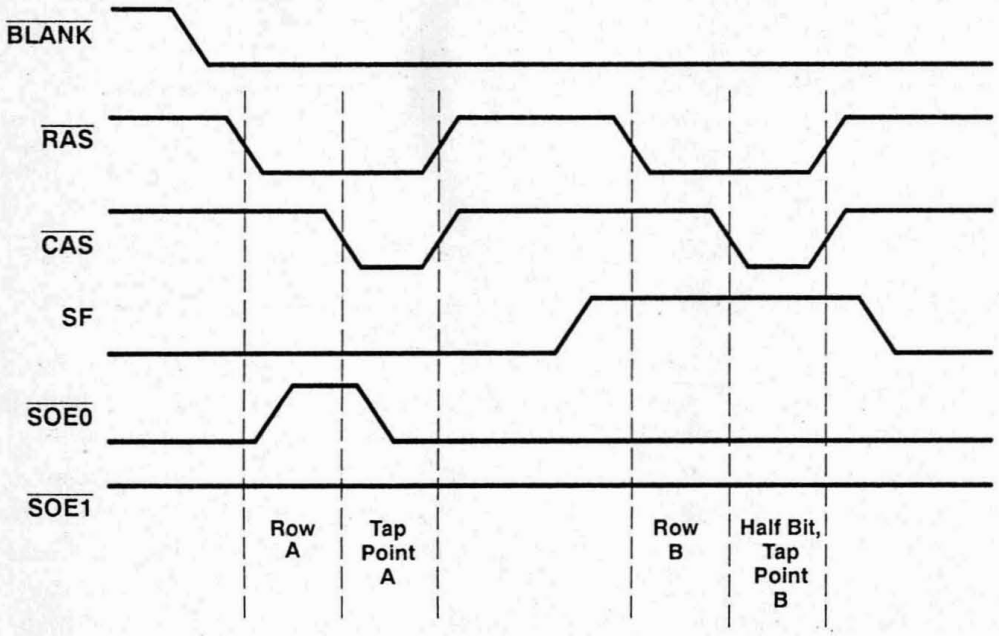

Figure 8. Generation of SOE0 and SOE1 (Both Previous and Current Display Line in VRAM Bank 0)

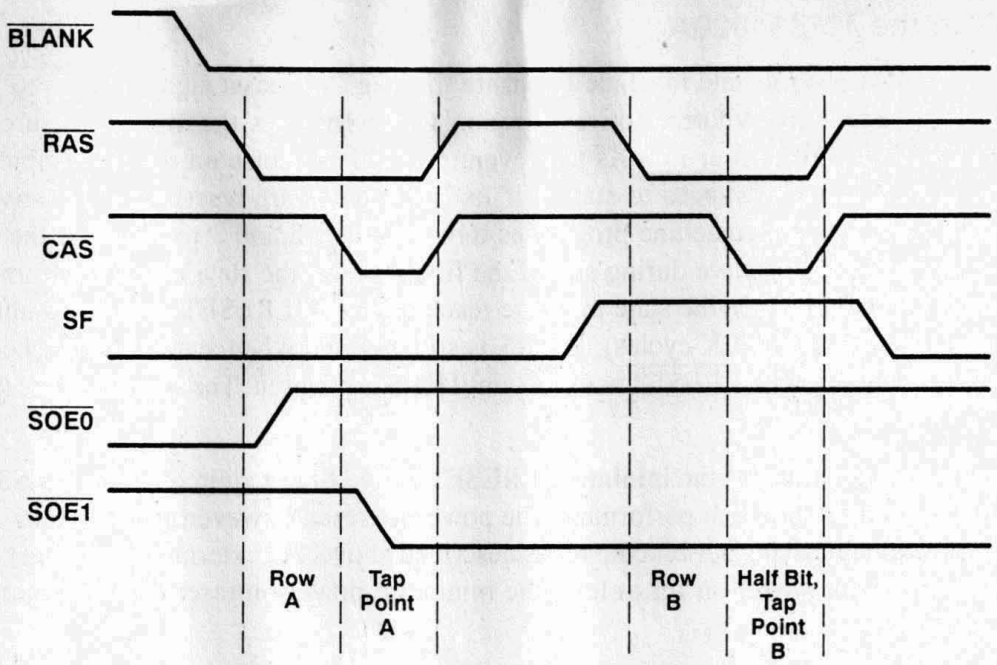

Figure 9. Generation of SOE0 and SOE1 (Previous Display Line in VRAM Bank 0, Current Line in VRAM Bank 1)

4.3 Video Interface Palette Control

The TLC34075's video output generation is based on sync and blanking signals from the TMS34020A, dot clock inputs, and TLC34075 control register values. In turn, the TLC34075 provides to the TMS34020A VCLK and SCLK signals that are used to generate video sync and blank signals (HSYNC, VSYNC, HBLNK, and VBLNK).

4.3.1 V ideo Interface Palette Control Registers

The TLC34075 implements ten control registers. Four of these registers are used to program the palette look-up table. The remaining six registers control the pixel data multiplexer, input clock select, VCLK and SCLK divide ratios, SCLK relocation for SSRTs, and several other aspects of palette operation. These registers are more thoroughly described in Section 5.

4.3.2 Accessing the Video Interface Control Registers

The RASDCD (U5) PAL maps the TLC34075's control registers into the TMS34020A's local memory space starting at address D0000000h. Each register is mapped into 32 bits of the memory space. However, since the TLC34075 has an 8-bit data bus, only the lower 8 bits of each long-word-aligned group of 32 bits may be read or written to. Memory accesses with the most significant nibble equal to Dh enable the palette, and latched address bits 8 through 5 are tied to the TLC34075's register select pins RS3 thru RS0, respectively. Note that this addressing scheme aliases the palette's registers throughout the range D0000200h through DFFFFFFFh.

4.3.3 TLC34075 Dot Clock Inputs

The TLC34075 has five possible dot clock inputs. Two of the five may be combined as a single complementary, ECL-compatible clock input or used as two separate TTL-compatible clock inputs. For a noninterlaced resolution of 1280 by 1024, a dot clock input of about 108 MHz is required. This design uses a 110-MHz ECL oscillator with complementary outputs running at a 5-V supply voltage for 1280-by-1024 displays. A 25-MHz TTL oscillator is used for 640-x-480 displays.

4.4 Resetting the TMS34020A

The RESET (U38) PAL uses a state machine to ensure that the local reset signal ($\overline{\text{LRESET}}$) meets the TMS34020A's reset requirements during active operation. Of the 16 states, the first four ensure that a reset pulse has a minimum length of four LCLKs to prevent reset due to noise on the HRS input. The state machine starts at state 0 and advances to state 1 if its HRS (hardware reset) input is active when its LCLK<1> input falls. The state machine progresses through states 2 and 3 to state 4 if the HRS input remains active (if HRS goes inactive during any of the first 4 states, the state machine returns to state 0 without asserting LRESET). Once the state machine reaches state 4, LRESET is asserted until the state machine reaches state 15 (12 LCLK cycles). If HRS is still asserted when state 15 is reached, the state machine remains in state 15, with $\overline{\text{LRESET}}$ asserted, until HRS is released. The state machine then returns to state 0.

This state machine timing exceeds the minimum LRESET active time required by the TMS34020A for reset after a power-on reset has been performed. The power-on reset, however, must be over 3 times the reset pulse length attainable using a 4-bit counter as described above. An external circuit must ensure that HRS is asserted cleanly at power-on for at least the minimum power-on reset time as described in the TMS34020A data sheet.

4.5 Resetting the TLC34075

Power-on reset of the TLC34075 is accomplished automatically by internal circuitry. An operating reset of the TLC34075 is effected by writing all ones to the TLC34075 register select (RS<3:0>) lines and then causing a low-to-high transition on the $\overline{\text{WR}}$ input. In this design, these actions occur as follows: when the RESET (U38) PAL asserts the LRESET signal, the LTCHDCD (U4) PAL drives LDAT<8:5> high and pulses its PALETWR output low while LCLK1 is high. No circuitry is needed to special-case the data inputs during the hardware reset, as the TLC34075 ignores its data bus when RS<3:0> are all high.

5 PROGRAMMING THE TLC34075 REGISTERS

This section describes several of the TLC34075's control registers. Included are the general control register, the input clock selection register, the output clock selection register, the multiplexer control register, and the palette programming registers. See the TLC34075 data sheet for details on the registers not described herein.

5.1 General Control Register

The general control register allows selection of several attributes of the outputs to the monitor as well as the special nibble mode (used in systems with distributed 16-bit-wide pixel buses) and SCLK pulse relocation. The polarities of the horizontal and vertical sync outputs are programmable; a 7.5-IRE pedestal and "sync on green" are also selectable. Table 1 describes the bit fields of the general control register. The general control register appears in the memory map at D0000100h.

Table 1. TLC34075 General Control Register

GENERAL CONTROL REGISTER BIT								FUNCTION
7	6	5	4	3	2	1	0	
X	X	X	X	X	X	X	0	HSYNCOUT active low
X	X	X	X	X	X	X	1	HSYNCOUT active high
X	X	X	X	X	X	0	X	VSYNCOUT acrtive low
X	X	X	X	X	X	1	X	VSYNCOUT active high
X	X	X	X	X	0	X	X	Split shift register transfer disable
X	X	X	X	0	1	X	X	Split shift register transfer enable
X	X	X	X	0	X	X	X	Special nibble mode disable
X	X	X	X	1	0	X	X	Special nibble mode enable
X	X	X	0	X	X	X	X	0-IRE pedestal
X	X	X	1	X	X	X	X	7.5-IRE pedestal
X	X	0	X	X	X	X	X	Sync disable
X	X	1	X	X	X	X	X	Sync enable
X	0	X	X	X	X	X	X	Reserved
X	1	X	X	X	X	X	X	Reserved
0	X	X	X	X	X	X	X	MUXOUT low (default)
1	X	X	X	X	X	X	X	MUXOUT high

5.2 Input Clock (Dot Clock) Selection

Input clock selection is based on the required display resolution and the frequencies of the available oscillators. The 110-MHz oscillator on the complementary inputs of the TLC34075 is selected by writing 8h to the input clock selection register (at memory location D0000120h). Note that the TLC34075 does not require an active clock to access the control registers.

5.3 SCLK and VCLK Divide Ratio Selection

SCLK and VCLK divide ratios are selected via the output clock selection register. The SCLK divide ratio determines how many pixels are available on the TLC34075's pixel inputs for each SCLK pulse. The SCLK divide ratio depends on the number of input bits used on the pixel bus (this application uses all 32 bits) and the number of bits per pixel. For a pixel size of 8 bits and a 32-bit-wide pixel bus, the SCLK divide ratio must be 4. Similarly, for a pixel size of 2 bits and a 32-bit-wide pixel bus, the SCLK divide ratio must be 16. The TLC34075 provides power-of-two SCLK divide ratios between 1 and 32, inclusive. An additional option holds the TLC34075 SCLK output in the low state regardless of the sync, blank, and clock inputs.

The VCLK divide ratio is used to determine the frequency of the signal that the TMS34020A uses to generate sync and blank signals. To reduce the RF noise generated by the board, the VCLK divide ratio is generally chosen to give the lowest possible frequency at which it is possible for the TMS34020A to produce proper sync and blank timings. The TLC34075 provides power-of-two VCLK divide ratios between 1 and 32, inclusive. An additional option holds the TLC34075 VCLK output in the high state regardless of the sync, blank, and clock inputs.

The SCLK and VCLK divide ratio selections are programmed as a six-bit value in the output clock selection register, which is mapped to memory location D0000140h in this application. The output clock selection register programming values are listed in Table 2.

Table 2. TLC34075 Output Clock Selection Register Programming Values

VCLK DIVIDE RATIO	SCLK DIVIDE RATIO					
	1	2	4	8	16	32
1	00h	01h	02h	03h	04h	05h
2	08h	09h	0Ah	0Bh	0Ch	0Dh
4	10h	11h	12h	13h	14h	15h
8	18h	19h	1Ah	1Bh	1Ch	1Dh
16	20h	21h	22h	23h	24h	25h
32	28h	29h	2Ah	2Bh	2Ch	2Dh

5.4 Multiplexer Control Programming

The multiplexer control register determines how the TLC34075 uses the input data. The number of bits per pixel and the number of bits physically connected to the pixel inputs of the TLC34075 are specified by this register. Each valid multiplexer control register value implies an SCLK divide ratio. The valid multiplexer control register values for this implementation are listed in Table 3. The multiplexer control register appears in the memory map at D0000160h.

Table 3. Suggested Multiplexer Control Register Values for This Implementation

NUMBER OF BITS PER PIXEL	MULTIPLEXER CONTROL REGISTER VALUE
1	13h
2	17h
4	18h
8	1Eh

5.5 Accessing the Palette Color Look-Up Tables

The TLC34075's palette look-up tables are accessed by writing the address of the look-up table entry to a palette read address register or palette write address register (D0000060h and D0000000h, respectively), then reading or writing the palette data register (D0000020h) three times (once each for red, green, and blue). After the three reads or writes, the palette read address register or palette write address register is autoincremented. The TLC34075 also has a pixel mask register (D0000040h) that allows incoming pixel values to be masked.

5.6 Suggested Values for TMS34020A and TLC34075 Registers

Table 4 shows the suggested TMS34020A and TLC34075 register values to use with a Mitsubishi Diamond Scan monitor and the hardware described. Video timing registers (addresses C0000000h to C0000070h) may need to be recalculated for other monitors. Note that the DPYCTL values for a 640-by-480 display at one or two bits per pixel do not use SSRTs. They implement nonpacked frame buffers; the remainder implement packed frame buffers and use SSRTs.

Table 4. Suggested TMS34020A and TLC34075 Register Values for Use With a Mitsubishi Diamond Scan Monitor

REGISTER	ADDRESS	1280 × 1024 × 8	1280 × 1024 × 4	1280 × 1024 × 2	1280 × 1024 × 1
VESYNC	C0000000h	0002h	0002h	0002h	0002h
HESYNC	C0000010h	0010h	0010h	0010h	0010h
VEBLNK	C0000020h	0022h	0022h	0022h	0022h
HEBLNK	C0000030h	0033h	0033h	0033h	0033h
VSBLNK	C0000040h	0422h	0422h	0422h	0422h
HSBLNK	C0000050h	00D3h	00D3h	00D3h	00D3h
VTOTAL	C0000060h	0426h	0426h	0426h	0426h
HTOTAL	C0000070h	00D7h	00D7h	00D7h	00D7h
DPYCTL	C0000080h	F047h	F047h	F047h	F047h
CONFIG	C00001A0h	0D0Ah	0D0Ah	0D0Ah	0D0Ah
PSIZE	C0000150h	0008h	0004h	0002h	0001h
DPYSTL	C0000200h	0800h	0000h	0000h	0000h
DPYSTH	C0000210h	0000h	0000h	0000h	0000h
DINCLO	C0000240h	2800h	1400h	0A00h	0500h
DINCHI	C0000250h	0000h	0000h	0000h	0000h
DPYMSK	C00002E0h	00FFh	00FFh	00FFh	00FFh
GENCTL	D0000100h	87h	87h	87h	87h
INCLK	D0000120h	08h	08h	08h	08h
OUTCLK	D0000140h	1Ah	1Bh	1Ch	1Dh
MUXCTL	D0000160h	1Eh	1Bh	17h	13h

REGISTER	ADDRESS	640 × 480 × 8	640 × 480 × 4	640 × 480 × 2	640 × 480 × 1
VESYNC	C0000000h	0002h	0002h	0002h	0002h
HESYNC	C0000010h	0006h	0006h	0006h	0006h
VEBLNK	C0000020h	0018h	0018h	0018h	0018h
HEBLNK	C0000030h	001Ah	001Ah	001Ah	001Ah
VSBLNK	C0000040h	01F8h	01F8h	01F8h	01F8h
HSBLNK	C0000050h	00BAh	00BAh	00BAh	00BAh
VTOTAL	C0000060h	01F9h	01F9h	01F9h	01F9h
HTOTAL	C0000070h	00C0h	00C1h	00BFh	00C1h
DPYCTL	C0000080h	F047h	F047h	F007h	F007h
CONFIG	C00001A0h	0D0Ah	0D0Ah	0D0Ah	0D0Ah
PSIZE	C0000150h	0008h	0004h	0002h	0001h
DPYSTL	C0000200h	0000h	0000h	0000h	0000h
DPYSTH	C0000210h	0000h	0000h	0000h	0000h
DINCLO	C0000240h	1400h	0A00h	0800h	0400h
DINCHI	C0000250h	0000h	0000h	0000h	0000h
DPYMSK	C00002E0h	00FFh	00FFh	00FFh	00FFh
GENCTL	D0000100h	87h	87h	83h	83h
INCLK	D0000120h	01h	01h	01h	01h
OUTCLK	D0000140h	12h	13h	14h	15h
MUXCTL	D0000160h	1Eh	1Bh	17h	13h

PART	REFERENCE	QUANTITY
10-μF tantalum capacitor	C1, C2, C3, C4	4
0.1-μF capacitor	C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C53, C54, C55, C56, C57, C58	46
0.22-μF capacitor	C45, C46, C47, C48, C49, C50, C51	7
0.33-μF tantalum capacitor	C52	1
0.1-μF capacitor	C59, C60, C61, C62	4
Ferrite bead Fair Rite Products 3274301112	L1, L2, L3, L4, L5, L6	6
DB9 connector	P1	1
DB15 connector	P2	1
4.7-kΩ resistor	R1	1
75-Ω 1% resistor	R2, R3, R4	3
523-Ω 1% resistor	R5	1
220-Ω resistor	R6, R9	2
330-Ω resistor	R7, R8	2
33-Ω resistor	R10, R11	2
100-Ω resistor	R12	1
33-Ω × 5 Isolated Resistor Network	RSIP1, RSIP2, RSIP3, RSIP4	4
TMS34020AGBL-40	U1	1
40-MHz TTL oscillator	U2	1
74AS841	U3	1
TIBPAL20L8-7	U4, U5	2
TMS44C256-10SD	U6, U7, U8, U9, U10, U11, U12, U13	8
TMS44C251-10SD	U14, U15, U16, U17, U18, U19, U20, U21, U22, U23, U24, U25, U26, U27, U28, U29	16
TLC34075-110	U30	1
25-MHz TTL oscillator	U32	1
110-MHz ECL oscillator GED LM1400E50 series or CTI K1149BA series	U36	1
64-MHz TTL oscillator	U37	1
TIBPAL16R4-25	U38	1

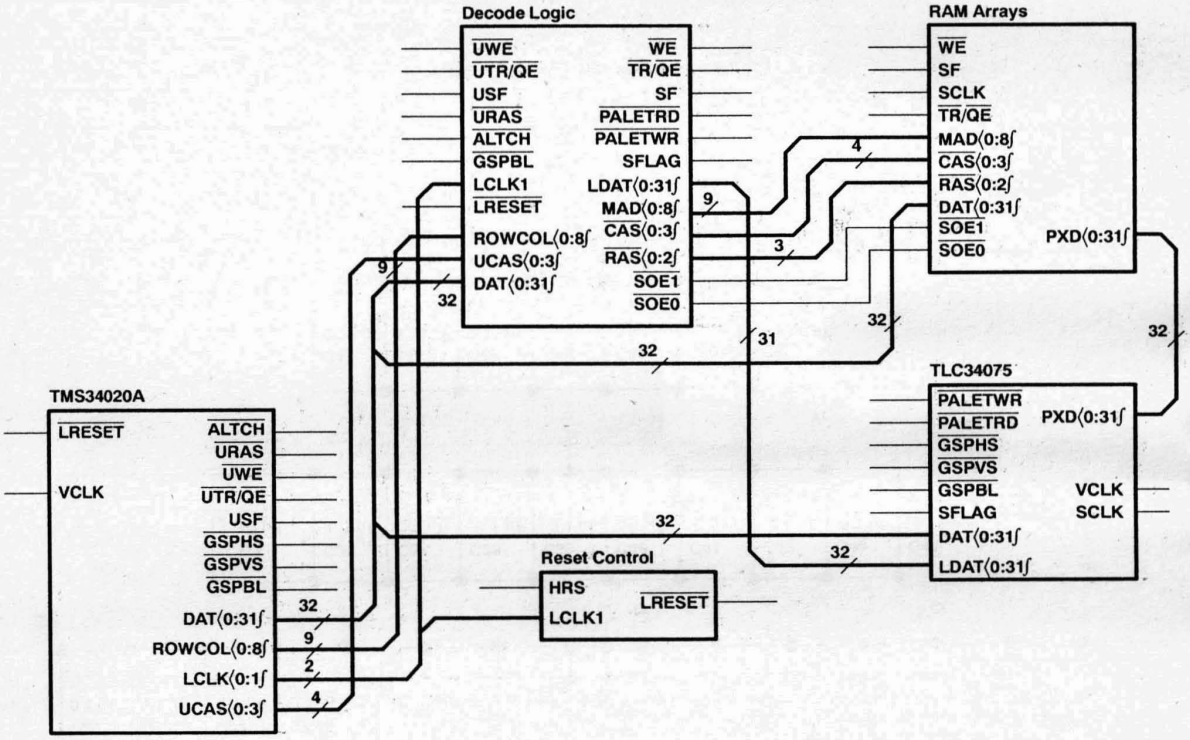

Figure A-1. System Block Diagram

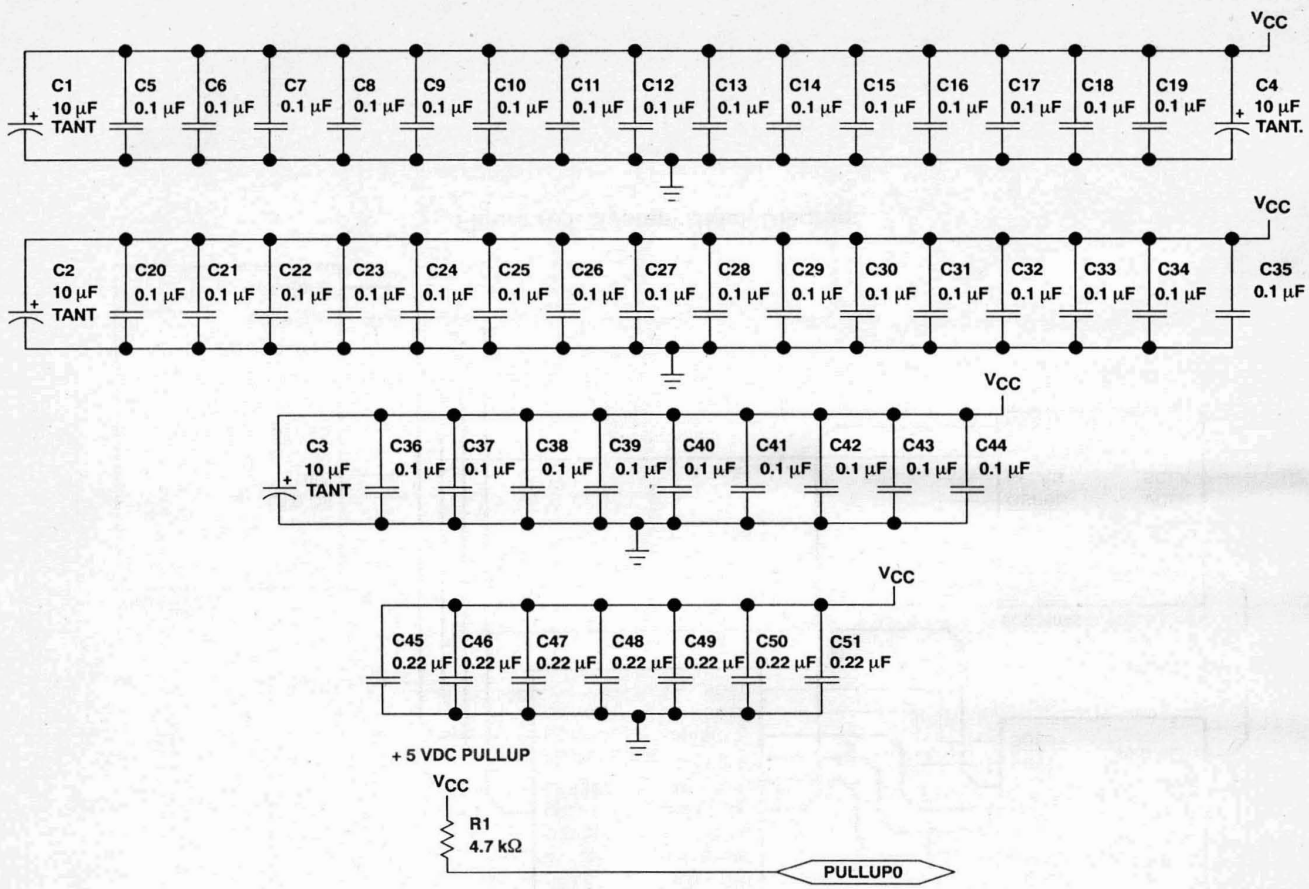

Figure A-2. Power Conditioning

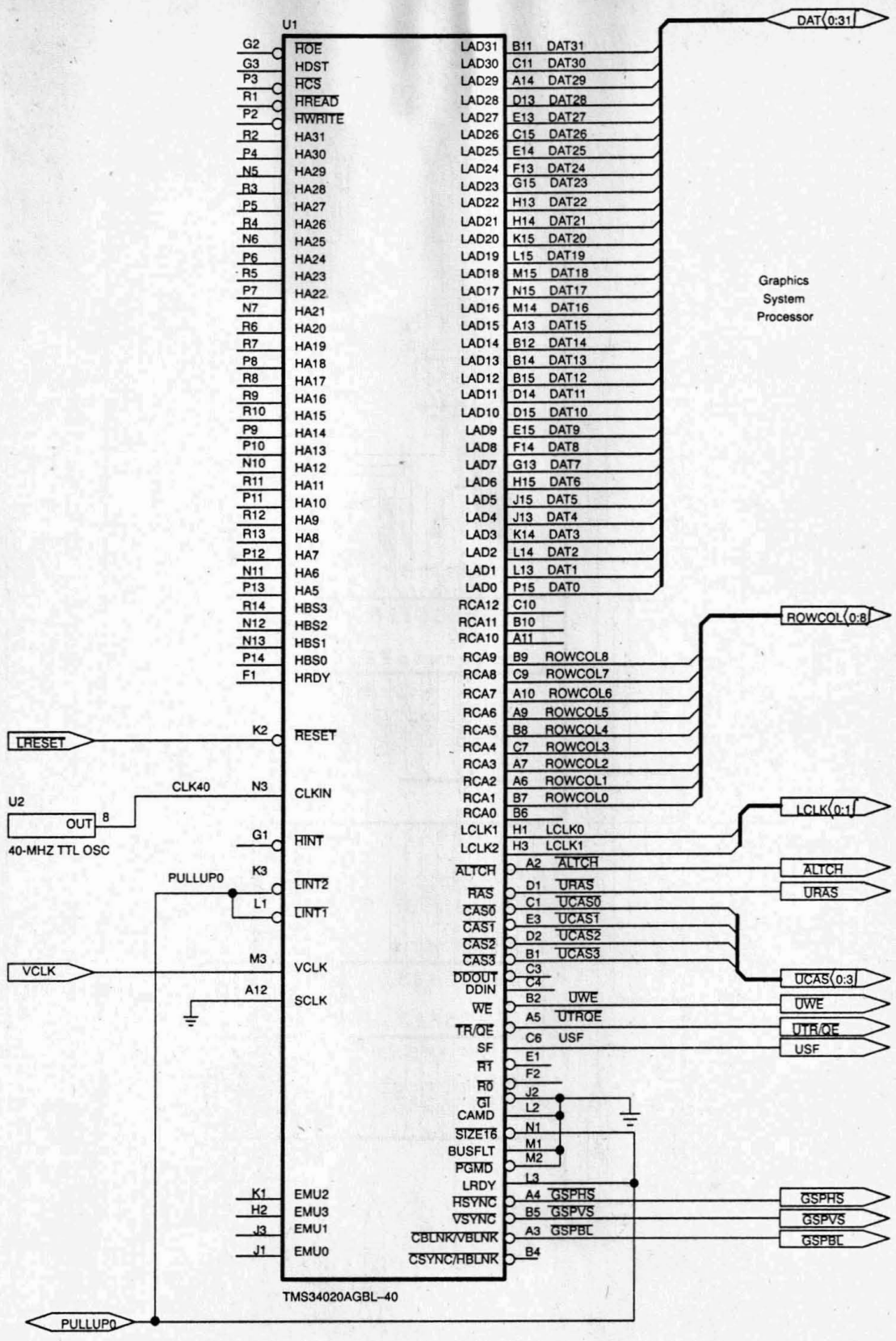

Figure A-3. Graphics System Processor Connection

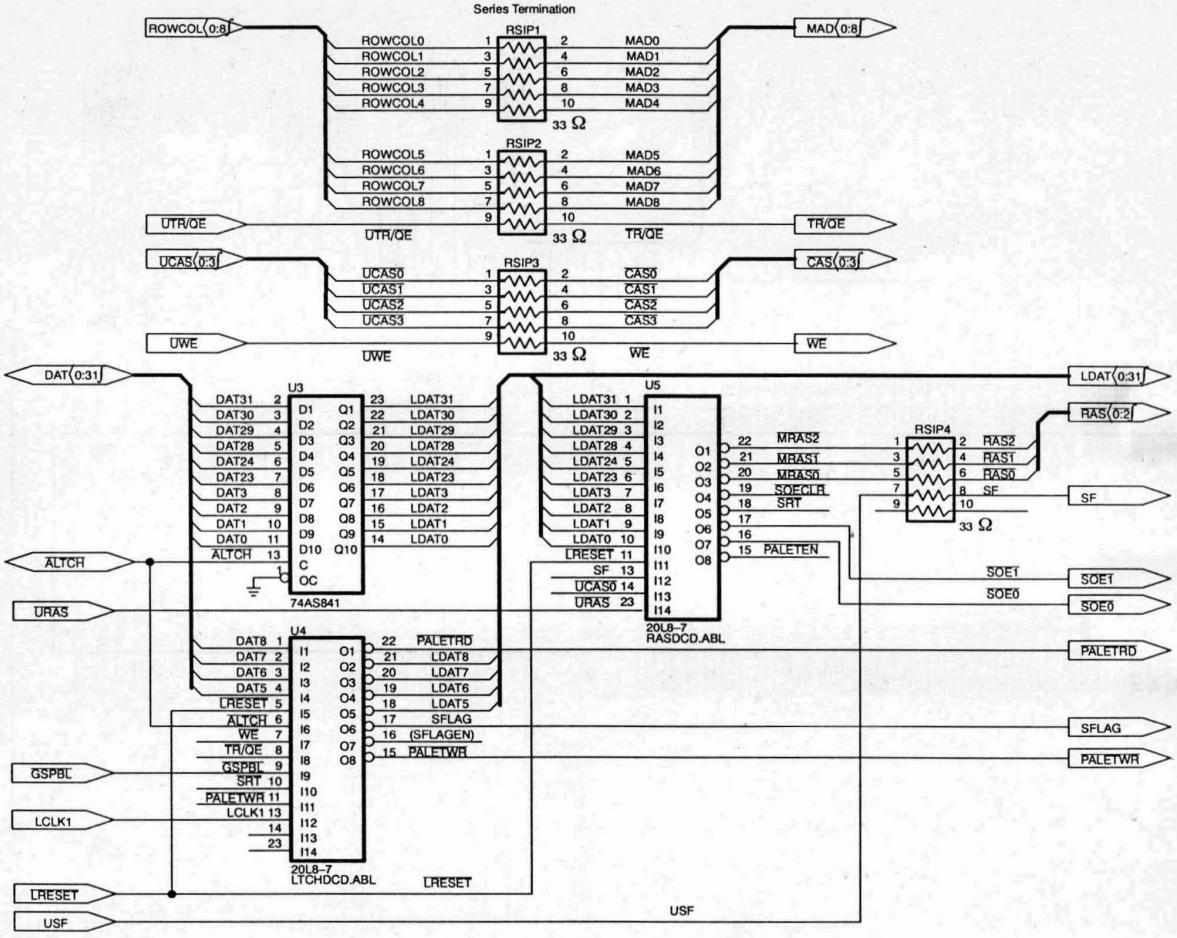

Figure A-4. Address Decoding, VRAM Control, and Series Terminations

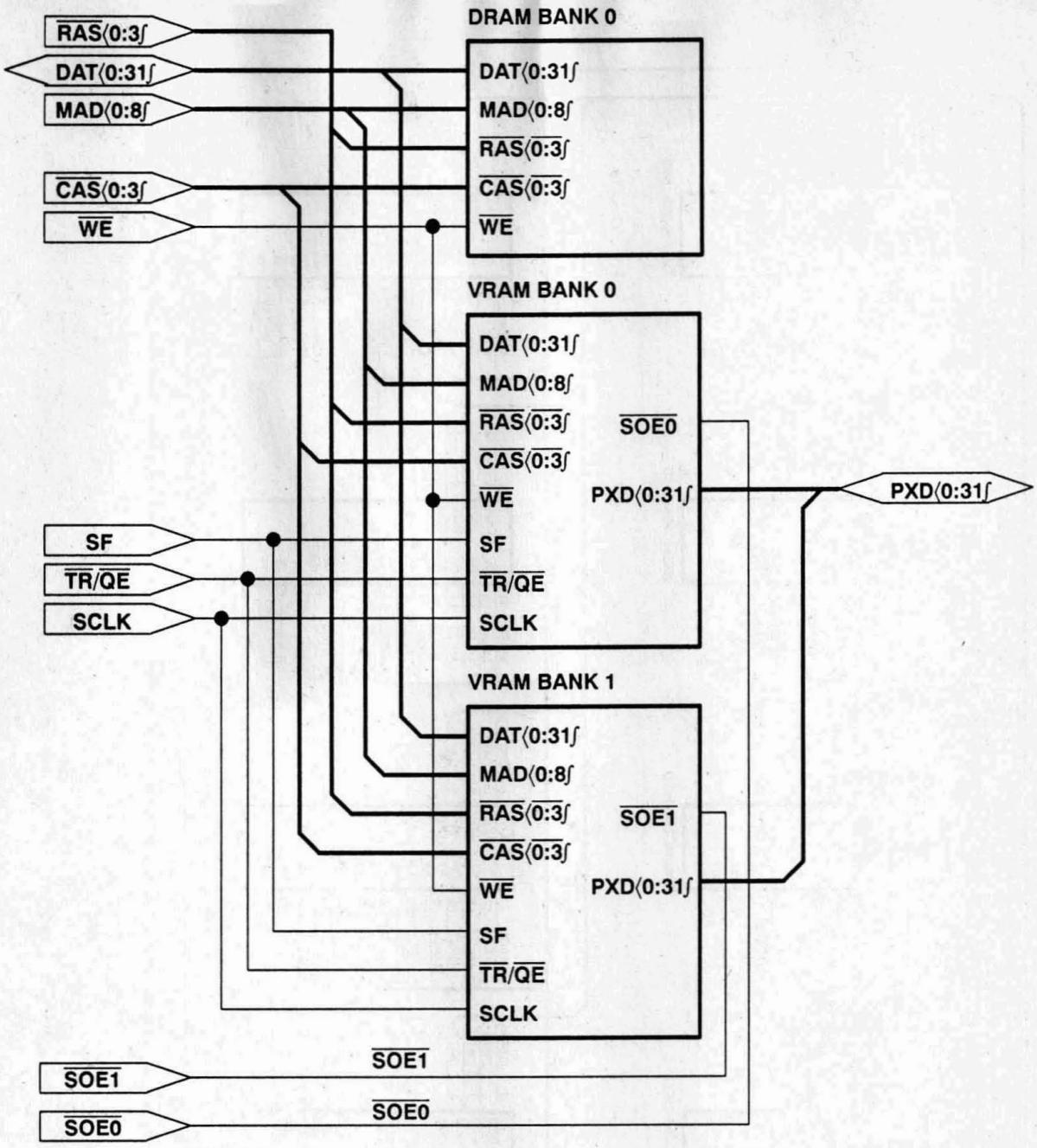

Figure A–5. RAM Array Block Diagram

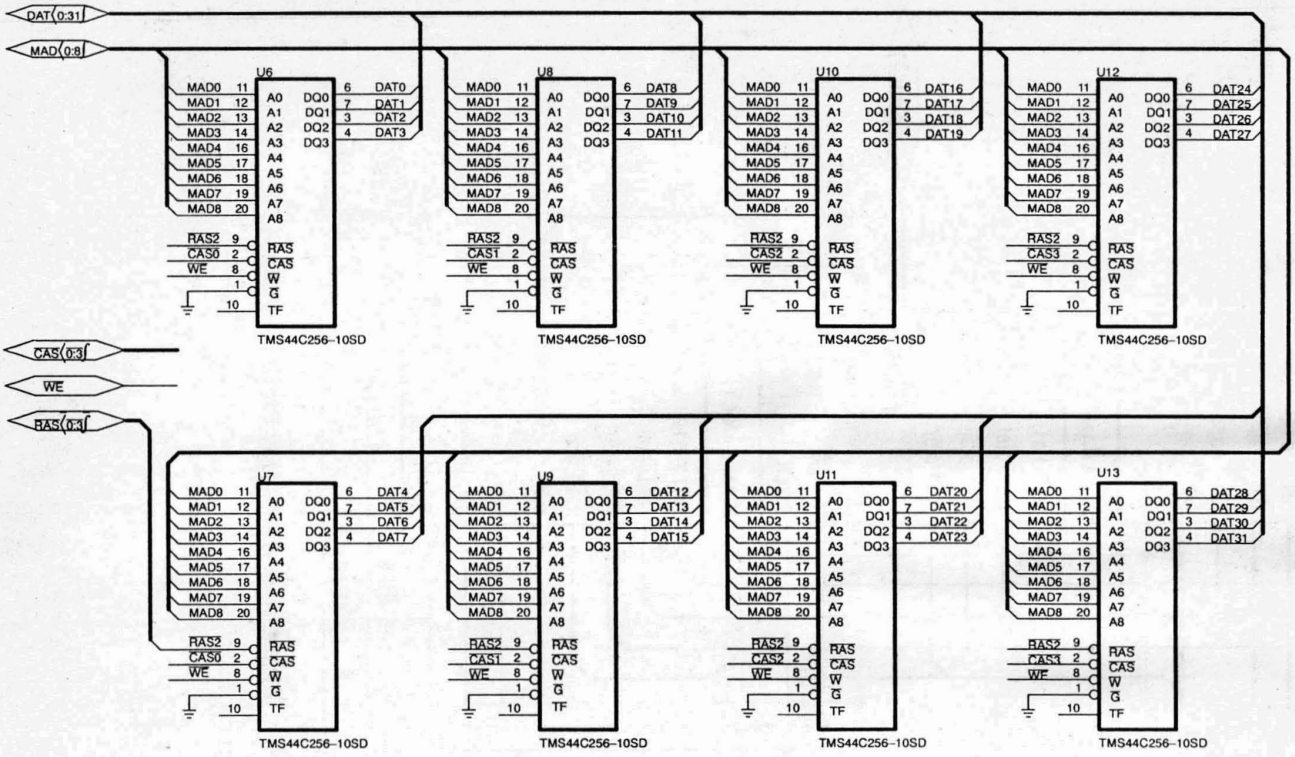

Figure A-6. Program Memory

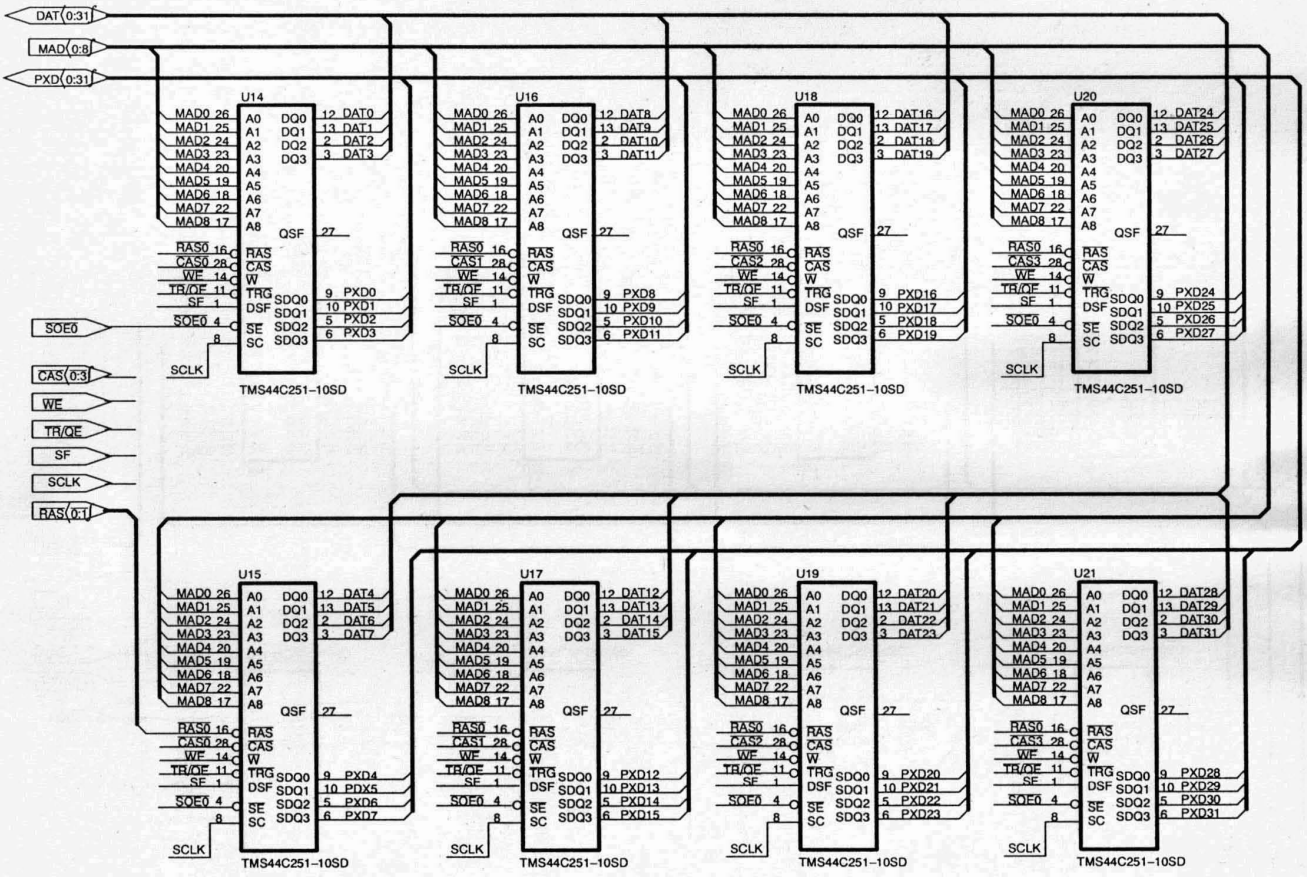

Figure A-7. Frame Memory Bank 0

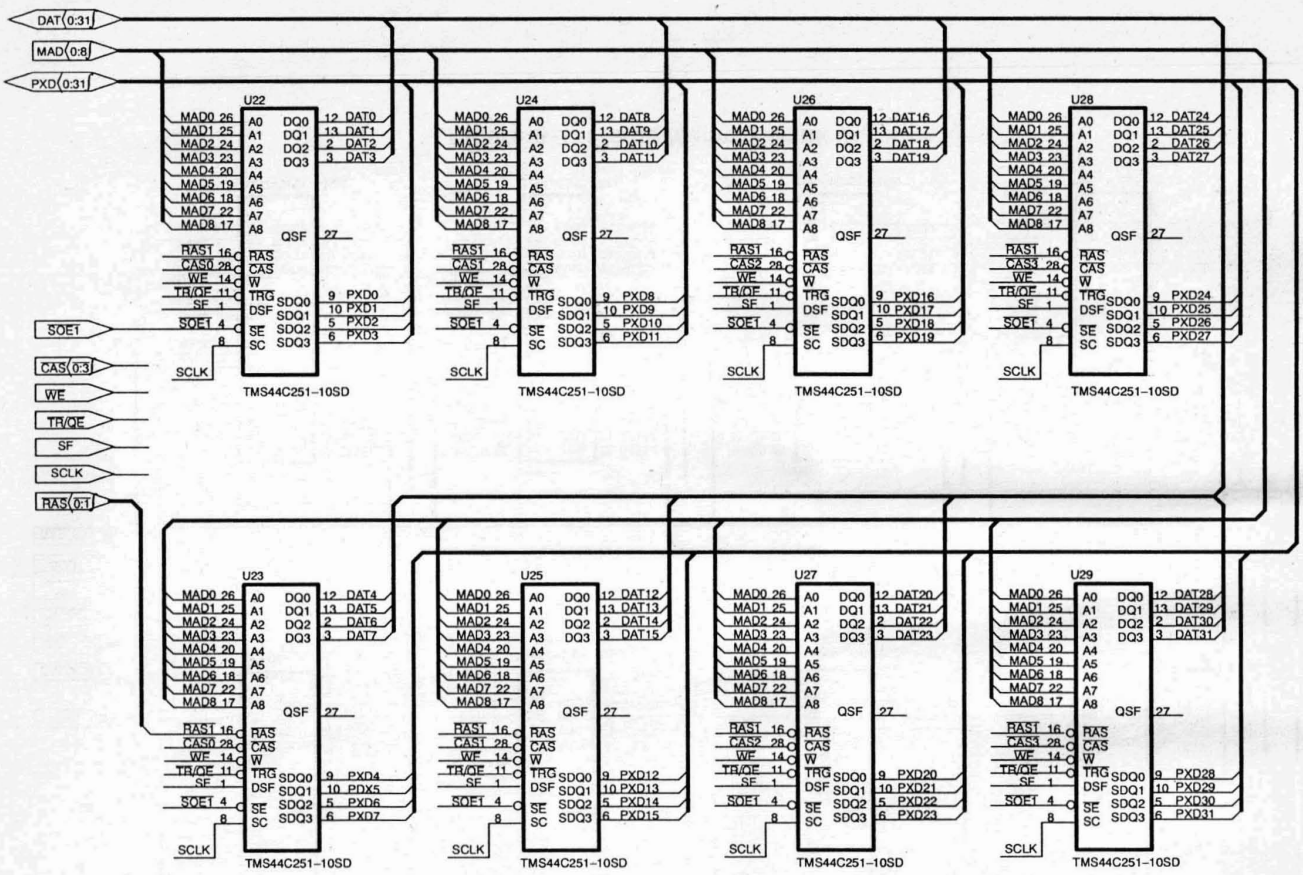

Figure A-8. Frame Memory Bank 1

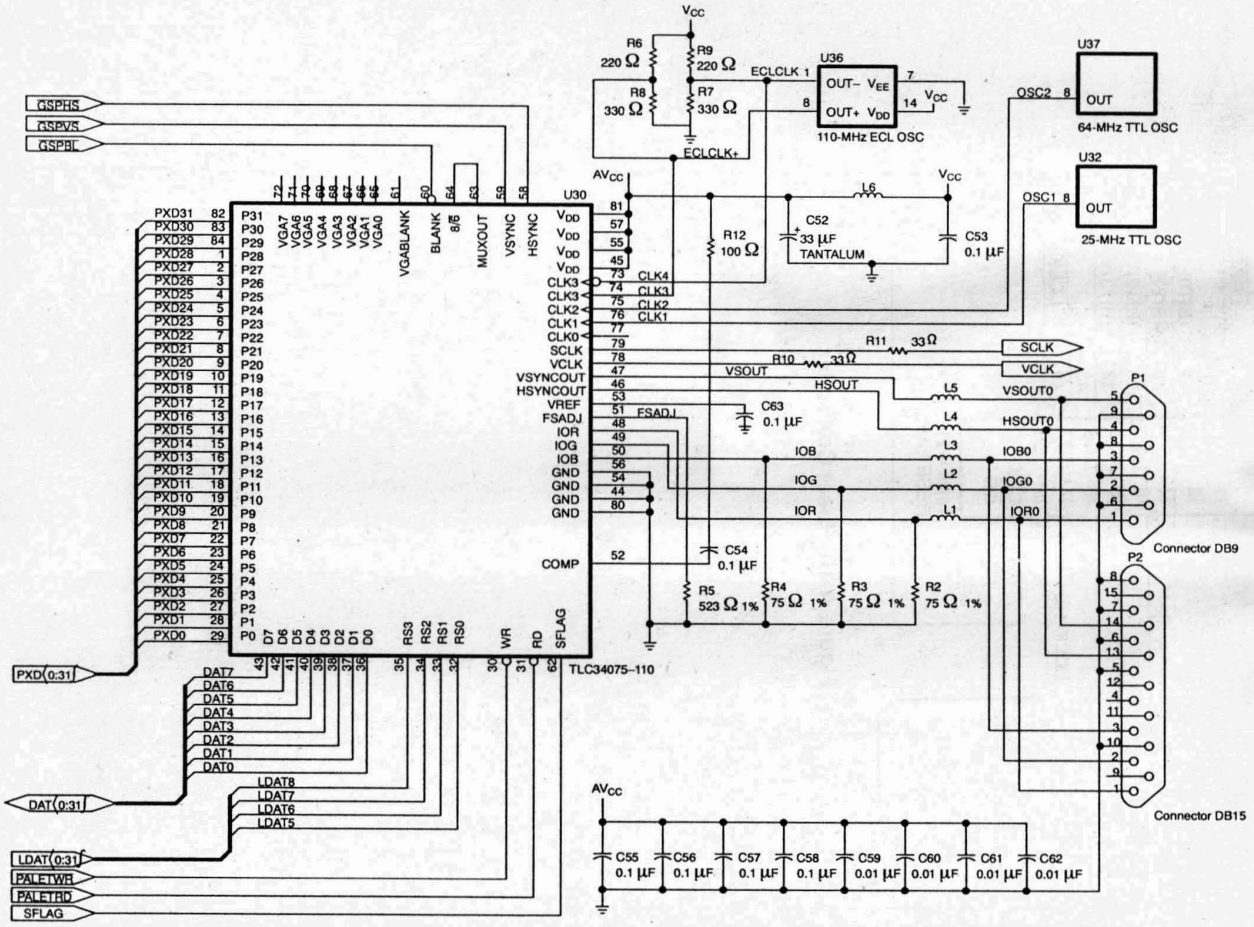

Figure A-9. Video Interface Palette

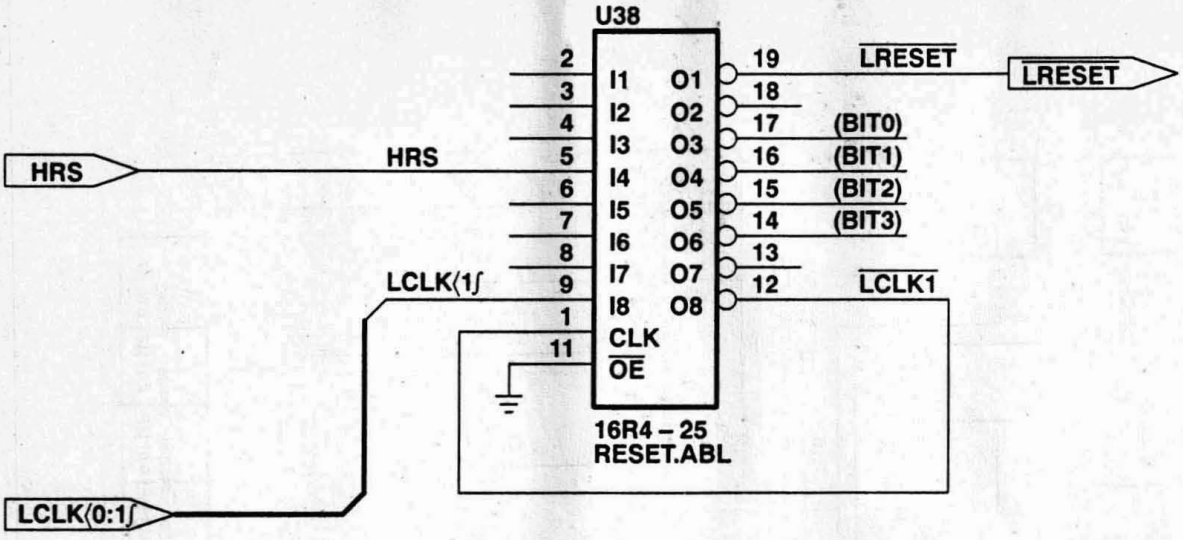

Figure A-10. Reset Controller

```
module  _LTCHDCD
"               Part        TIBPAL20L8-7
"               Reference   U4
"               Revision    *
"               Date        1/8/91
"               By          Bob Milhaupt
"               Company     Texas Instruments, Inc.

title   'Auxillary Decode and Address Latch'

" AUXILLARY DECODE AND ADDRESS LATCHING PAL®(LTCHDCD)
"
" Decodes several signals and latches address data for the 34075 VIP:
" Decodes palette writes and reads and asserts SFLAG after an SRT during
" blanking.  Latches incomming DAT8..5 as LDAT8..5 on the falling edge of
" ALTCH by using internal feedback paths of the PAL.  PALETRD and PALETWR
" are also generated.  During reset, PALETWR is pulsed and LDAT8..5 are
" forced high to send a hardware reset signal to the 34075.

LTCHDCD device 'P20L8';

"Inputs

DAT8            pin 1;
DAT7            pin 2;
DAT6            pin 3;
DAT5            pin 4;
!LRESET         pin 5;
ALTCH           pin 6;
!WE             pin 7;
!TRQE           pin 8;
!GSPBLNK        pin 9;
!SRT            pin 10;
!PALETEN        pin 11;
LCLK1           pin 13;
SFLAGEN         pin 16;

"Outputs

LDAT8           pin 21;
LDAT7           pin 20;
LDAT6           pin 19;
LDAT5           pin 18;
SFLAG           pin 17;
!PALETRD        pin 22;
!PALETWR        pin 15;


EQUATIONS

" LRESET is used in the LDAT8 - 5 equations to ensure that they are
" forced hi during reset.  This is required to send the hardware reset
" to the 34075

LDAT8   =  DAT8  &  ALTCH
        #  LDAT8 & !ALTCH
        #  LRESET;

LDAT7   =  DAT7  &  ALTCH
        #  LDAT7 & !ALTCH
        #  LRESET;

LDAT6   =  DAT6  &  ALTCH
        #  LDAT6 & !ALTCH
```

PAL is a registered trademark of Advanced Micro Devices.

```
        #  LRESET;

LDAT5   =  DAT5  &  ALTCH
        #  LDAT5 & !ALTCH
        #  LRESET;

" LCLK1 and LRESET are used in the PALETWR equation so that the PALETWR pin
" goes active with LCLK1 during reset.  This, coupled with forcing LDAT8..5
" high during reset, sends the hardware reset signal to the 34075.

PALETWR =  PALETEN &  WE
        #  LRESET  &  LCLK1;

PALETRD =  PALETEN & !WE      &  TRQE;

" SFLAGEN decodes the falling edge of ALTCH of an SRT cycle during blanking.
" SFLAG is asserted on the rising edge of ALTCH at the end of the SRT cycle.
" Both SFLAGEN and SFLAG stay active until the end of blanking to ensure
" that SFLAG only goes high once during blanking.

SFLAGEN =  SRT     &  GSPBLNK & !ALTCH
        #  SFLAGEN &  GSPBLNK & !(SRT & !ALTCH) ;

SFLAG   =  SFLAGEN &  GSPBLNK &  ALTCH
        #  SFLAG   &  GSPBLNK;


TEST_VECTORS
"test action of PALETWR pin during reset
([ PALETEN, WE, LCLK1, TRQE, !LRESET] ->
    [ PALETWR, PALETRD])
[ 0 , 0 , 0 , 0 , 0 ] -> [ 0 , 0 ];
[ 0 , 0 , 1 , 0 , 0 ] -> [ 1 , 0 ];
[ 0 , 0 , 0 , 0 , 0 ] -> [ 0 , 0 ];
[ 0 , 0 , 1 , 0 , 0 ] -> [ 1 , 0 ];
[ 0 , 0 , 0 , 0 , 0 ] -> [ 0 , 0 ];
[ 0 , 0 , 1 , 0 , 0 ] -> [ 1 , 0 ];

TEST_VECTORS
"test action of LDAT8..5 during reset
([ DAT8, DAT7, DAT6, DAT5, ALTCH, !LRESET] ->
    [ LDAT8, LDAT7, LDAT6, LDAT5])
[ 0 , 0 , 0 , 0 , 1 , 0 ] -> [ 1 , 1 , 1 , 1 ];
[ 0 , 0 , 0 , 1 , 1 , 0 ] -> [ 1 , 1 , 1 , 1 ];
[ 0 , 0 , 1 , 0 , 1 , 0 ] -> [ 1 , 1 , 1 , 1 ];
[ 0 , 1 , 0 , 0 , 1 , 0 ] -> [ 1 , 1 , 1 , 1 ];
[ 1 , 0 , 0 , 0 , 1 , 0 ] -> [ 1 , 1 , 1 , 1 ];
[ 0 , 0 , 0 , 0 , 1 , 1 ] -> [ 0 , 0 , 0 , 0 ];

TEST_VECTORS
"test action of SFLAG, SFLAGEN

([ SRT, ALTCH, GSPBLNK] -> [ SFLAGEN, SFLAG])
[.X.,.X., 0 ] -> [ 0 , 0 ];
[ 0 , 1 , 1 ] -> [ 0 , 0 ];     " Non-SRT cycle, blank active
[ 0 , 0 , 1 ] -> [ 0 , 0 ];
[ 0 , 1 , 1 ] -> [ 0 , 0 ];     " SRT cycle, blank active
[ 1 , 1 , 1 ] -> [ 0 , 0 ];
[ 1 , 0 , 1 ] -> [ 1 , 0 ];     " SRT cycle, altch low
[ 1 , 1 , 1 ] -> [ 1 , 1 ];     " Altch high at end of SRT
[ 0 , 1 , 1 ] -> [ 1 , 1 ];     " Beginning of next cycle
[ 0 , 0 , 1 ] -> [ 1 , 1 ];     " Altch falls on next cycle
[ 0 , 0 , 0 ] -> [ 0 , 0 ];     " End of blanking
```

```
TEST_VECTORS
"check LDAT8..5 when not resetting
([ DAT8, DAT7, DAT6, DAT5, ALTCH, !LRESET] ->
    [ LDAT8, LDAT7, LDAT6, LDAT5])

[ 0 , 0 , 0 , 0 ,  1 , 1 ] -> [0,0,0,0];
[ 0 , 0 , 0 , 0 ,  0 , 1 ] -> [0,0,0,0];
[.X.,.X.,.X.,.X.,  0 , 1 ] -> [0,0,0,0];

[ 0 , 0 , 0 , 1 ,  1 , 1 ] -> [0,0,0,1];
[ 0 , 0 , 0 , 1 ,  0 , 1 ] -> [0,0,0,1];
[.X.,.X.,.X.,.X.,  0 , 1 ] -> [0,0,0,1];

[ 0 , 0 , 1 , 0 ,  1 , 1 ] -> [0,0,1,0];
[ 0 , 0 , 1 , 0 ,  0 , 1 ] -> [0,0,1,0];
[.X.,.X.,.X.,.X.,  0 , 1 ] -> [0,0,1,0];

[ 0 , 1 , 0 , 0 ,  1 , 1 ] -> [0,1,0,0];
[ 0 , 1 , 0 , 0 ,  0 , 1 ] -> [0,1,0,0];
[.X.,.X.,.X.,.X.,  0 , 1 ] -> [0,1,0,0];

[ 1 , 0 , 0 , 0 ,  1 , 1 ] -> [1,0,0,0];
[ 1 , 0 , 0 , 0 ,  0 , 1 ] -> [1,0,0,0];
[.X.,.X.,.X.,.X.,  0 , 1 ] -> [1,0,0,0];


END _LTCHDCD
```

```
module  _RESET;
"               Part        TIBPAL16R4-25
"               Reference   U38
"               Revision    *
"               Date        1/8/91
"               By          Bob Milhaupt
"               Company     Texas Instruments, Inc.

title   'RESET'

" RESET CONTROL PAL®(RESET)
"
" The primary function of RESET is to filter spurious noise from the
" HRS (Hardware Reset) input and provide a local reset signal (LRESET) which
" meets the TMS34020's reset timing specs.  This reset mechanism is
" implemented using a state machine.  It requires that HRS remain active for
" four successive LCLK1 edges.  Following this condition the state machine
" then goes into a closed 11 state loop.  The last state waits for HRS to be
" removed before returning to state 0.  LRESET is held inactive in states 0
" through 3, and active during states 4 through 15.  The HRS input must be
" held active at power-up long enough to satisfy the TMS34020A power-up reset
" timing requirements.

RESET device 'P16R4';

"Inputs

CLK             pin  1  ;
HRS             pin  5  ;       "Hardware Reset
LCLK1           pin  9  ;

"Outputs

!LRESET         pin  19 ;       "Local Reset signal to 34020, logic
OCLK1           pin  12 ;       "Delayed LCLK1
BIT0            pin  17 ;       "State Machine LSB
BIT1            pin  16 ;
BIT2            pin  15 ;
BIT3            pin  14 ;       "State Machine MSB

"Declarations and Intermediate Variable Definitions

S       =  [BIT3,BIT2,BIT1,BIT0];
S0      =  ^b0000;
S1      =  ^b0001;
S2      =  ^b0010;
S3      =  ^b0011;
S4      =  ^b0100;
S5      =  ^b0101;
S6      =  ^b0110;
S7      =  ^b0111;
S8      =  ^b1000;
S9      =  ^b1001;
S10     =  ^b1010;
S11     =  ^b1011;
S12     =  ^b1100;
S13     =  ^b1101;
S14     =  ^b1110;
S15     =  ^b1111;

EQUATIONS

OCLK1   = !LCLK1;
```

```
LRESET   = (S == S4 ) # (S == S5 ) # (S == S6 ) #
           (S == S7 ) # (S == S8 ) # (S == S9 ) #
           (S == S10) # (S == S11) # (S == S12) #
           (S == S13) # (S == S14) # (S == S15);

STATE_DIAGRAM S
    STATE S0:      IF (  HRS )  THEN S1 ELSE S0;
    STATE S1:      IF (  HRS )  THEN S2 ELSE S0;
    STATE S2:      IF (  HRS )  THEN S3 ELSE S0;
    STATE S3:      IF (  HRS )  THEN S4 ELSE S0;
    STATE S4:        GOTO S5;
    STATE S5:        GOTO S6;
    STATE S6:        GOTO S7;
    STATE S7:        GOTO S8;
    STATE S8:        GOTO S9;
    STATE S9:        GOTO S10;
    STATE S10:       GOTO S11;
    STATE S11:       GOTO S12;
    STATE S12:       GOTO S13;
    STATE S13:       GOTO S14;
    STATE S14:       GOTO S15;
    STATE S15:     IF ( !HRS )  THEN S0 ELSE S12;

END _RESET
```

```
module  _RASDCD;
"               Part        TIBPAL20L8-7
"               Reference   U5
"               Revision    *
"               Date        1/8/91
"               By          Bob Milhaupt
"               Company     Texas Instruments, Inc.

title   'RAS and VRAM Control Decoder'

" RAS DECODE PAL®(RASDCD)
"
" RASDCD performs RAS decoding for memory segmentation.  Note that there is
" a significant degree of aliasing to reduce complexity and chip count of
" the decoder.  LDAT31..28 are used in decoding bank selects for RAM,
" shadow ram, and palette memory mapping.  LDAT24 and LDAT23 (in addition
" to LDAT31..28) are used select between VRAM bank 0, VRAM bank 1, and DRAM
" bank 0 via the RAS0, RAS1, and RAS2 signals, respectively.  One device
" select, PALETEN, is decoded to enable reads and writes of the 34075 Video
" Interface Palette.  Status bits LAD<3:0> determine refresh and VRAM cycles.
" These are also used in decoding the RAS signals.  The SRT output decodes
" Shift Register Transfers.  Other logic uses this signal to determine the
" end of the SRT cycle at which time the SFLAG input of the 34075 Video
" Interface Palette should be asserted.  This relocates the first SCLK pulse
" as necessary when using Split Shift Register Transfers.

RASDCD device 'P20L8';

"Inputs

LDAT31          pin  1;
LDAT30          pin  2;
LDAT29          pin  3;
LDAT28          pin  4;
LDAT24          pin  5;
LDAT23          pin  6;
LDAT3           pin  7;
LDAT2           pin  8;
LDAT1           pin  9;
LDAT0           pin  10;
!LRESET         pin  11;
SF              pin  13;
!CAS0           pin  14;
!URAS           pin  23;

"Outputs

!PALETEN        pin  15;    " Palette select
!RAS2           pin  22;    " DRAM RAS
!RAS1           pin  21;    " VRAM Bank 1 RAS
!RAS0           pin  20;    " VRAM Bank 0 RAS
!SOECLR         pin  19;    " Internal feedback term
!SRT            pin  18;
!SOE1           pin  17;    " Serial Output Enable, Bank 1
!SOE0           pin  16;    " Serial Output Enable, Bank 0

"Declarations and Intermediate Variable Definitions

REFRESH =    !LDAT3  & !LDAT2  &  LDAT1  &  LDAT0 ;

VTRANS  =    !LDAT3  &  LDAT2  & !LDAT1  & !LDAT0 ;

CTRANS  =    !LDAT3  &  LDAT2  & !LDAT1  &  LDAT0 ;
```

```
" OTHVTM decodes some other VRAM cycles where both VRAM banks must have
" active RAS signal: Write-Mask Load and Color-Register Load

OTHVRM  =    !LDAT3  &  LDAT2  &  LDAT1;

INTAREA =     LDAT3  & !LDAT2  &  LDAT1  &  LDAT0 ;

PALET   =     LDAT31 &  LDAT30 & !LDAT29 &  LDAT28;

VBNK0   =    !LDAT31 & !LDAT30 & !LDAT24 & !LDAT23;

VBNK1   =    !LDAT31 & !LDAT30 & !LDAT24 &  LDAT23;

" DBANK aliases DRAM into high memory so the interrupt and trap vectors
" may be written.

DBANK   =  ( !LDAT31 & !LDAT30 & !LDAT29 & !LDAT28 &  LDAT24) #
           (  LDAT31 &  LDAT30 &  LDAT29 &  LDAT28 );

X       =  .X.;

EQUATIONS

SOECLR  =     VTRANS &  URAS   & !CAS0   & !SF;

RAS2    =  (  DBANK  #  REFRESH #  INTAREA) &  URAS;

RAS0    =  (  VBNK0  #  REFRESH #  OTHVRM ) &  URAS & !INTAREA;

RAS1    =  (  VBNK1  #  REFRESH #  OTHVRM ) &  URAS & !INTAREA;

PALETEN =     PALET  & !REFRESH &  URAS;

SOE0    =  (( SOE0   & !SOECLR) # ( VTRANS  &  CAS0 &  RAS0));

SOE1    =  (( SOE1   & !SOECLR) # ( VTRANS  &  CAS0 &  RAS1));

SRT     =  (  VTRANS &  URAS    &  CAS0     & !SF   & (SOE0 # SOE1) )
           # (SRT    & !URAS);

TEST_VECTORS
        ([LDAT31,LDAT30,LDAT29,LDAT28,LDAT24,LDAT23,
          LDAT3,LDAT2,LDAT1,LDAT0,URAS,LRESET,CAS0,SF] ->
         [PALETEN,RAS2,RAS1,RAS0,SOE0,SOE1,SOECLR,SRT])

" check RAS decoding
    [0,0,0,0,0,0,0,0,0,0,0,0,0,0] -> [0,0,0,0,X,X,X,X];
    [1,1,0,1,0,0,0,0,0,0,1,0,0,0] -> [1,0,0,0,X,X,X,X];
    [0,0,0,0,1,0,0,0,0,0,0,1,0,0] -> [0,1,0,0,X,X,X,X];
    [0,0,0,0,1,1,0,0,0,0,0,1,0,0] -> [0,1,0,0,X,X,X,X];
    [0,0,0,0,0,0,0,0,0,0,0,1,0,0] -> [0,0,0,1,X,X,X,X];

" check assertion of RAS0
    [0,0,0,0,0,0,0,0,1,0,0,1,0,0] -> [0,0,0,1,X,X,X,X];
    [0,0,0,0,0,0,0,0,1,0,1,1,0,0] -> [0,0,0,1,X,X,X,X];
    [0,0,0,0,0,0,0,0,1,1,0,1,0,0] -> [0,0,1,1,X,X,X,X];
    [0,0,0,0,0,0,0,0,1,1,1,1,0,0] -> [0,0,1,1,X,X,X,X];
    [0,0,0,0,0,0,0,1,0,0,0,1,0,0] -> [0,0,0,1,X,X,X,X];
    [0,0,0,0,0,0,0,1,0,0,1,1,0,0] -> [0,0,0,1,X,X,X,X];
    [0,0,0,0,0,0,0,1,0,1,0,1,0,0] -> [0,0,0,1,X,X,X,X];

" check assertion of RAS2 when address is 0 and interrupt fetch is given
    [0,0,0,0,0,0,1,0,1,1,1,0,0,0] -> [0,1,0,0,X,X,X,X];
```

```
" check assertion of RAS1
    [0,0,0,0,0,1,0,1,0,0,1,0,0,0] -> [0,0,1,0,X,X,X,X];
    [0,0,0,0,0,1,0,1,0,1,1,0,0,0] -> [0,0,1,0,X,X,X,X];
    [0,0,0,0,0,1,0,1,1,0,1,0,0,0] -> [0,0,1,1,X,X,X,X];
    [0,0,0,0,0,1,0,1,1,1,1,0,0,0] -> [0,0,1,1,X,X,X,X];
    [0,0,0,0,0,1,1,0,0,0,1,0,0,0] -> [0,0,1,0,X,X,X,X];
    [0,0,0,0,0,1,1,0,0,1,1,0,0,0] -> [0,0,1,0,X,X,X,X];
    [0,0,0,0,0,1,1,0,1,0,1,0,0,0] -> [0,0,1,0,X,X,X,X];

" check assertion of RAS2 when address is 0 and interrupt fetch is given
    [0,0,0,0,0,1,1,0,1,1,1,0,0,0] -> [0,1,0,0,X,X,X,X];

" check assertion of RAS2
    [0,0,0,0,1,0,0,1,0,0,1,0,0,0] -> [0,1,0,0,X,X,X,X];
    [0,0,0,0,1,0,0,1,0,1,1,0,0,0] -> [0,1,0,0,X,X,X,X];
    [0,0,0,0,1,0,0,1,1,0,1,0,0,0] -> [0,1,X,X,X,X,X,X];
    [0,0,0,0,1,0,0,1,1,1,1,0,0,0] -> [0,1,X,X,X,X,X,X];
    [0,0,0,0,1,0,1,0,0,0,1,0,0,0] -> [0,1,0,0,X,X,X,X];
    [0,0,0,0,1,0,1,0,0,1,1,0,0,0] -> [0,1,0,0,X,X,X,X];
    [0,0,0,0,1,0,1,0,1,0,1,0,0,0] -> [0,1,0,0,X,X,X,X];
    [0,0,0,0,1,0,1,0,1,1,1,0,0,0] -> [0,1,0,0,X,X,X,X];

" check assertion of RAS2 for a shadow of dram
    [0,0,0,0,1,1,0,1,0,0,1,0,0,0] -> [0,1,0,0,X,X,X,X];
    [0,0,0,0,1,1,0,1,0,1,1,0,0,0] -> [0,1,0,0,X,X,X,X];
    [0,0,0,0,1,1,0,1,1,0,1,0,0,0] -> [0,1,X,X,X,X,X,X];
    [0,0,0,0,1,1,0,1,1,1,1,0,0,0] -> [0,1,X,X,X,X,X,X];
    [0,0,0,0,1,1,1,0,0,0,1,0,0,0] -> [0,1,0,0,X,X,X,X];
    [0,0,0,0,1,1,1,0,0,1,1,0,0,0] -> [0,1,0,0,X,X,X,X];
    [0,0,0,0,1,1,1,0,1,0,1,0,0,0] -> [0,1,0,0,X,X,X,X];
    [0,0,0,0,1,1,1,0,1,1,1,0,0,0] -> [0,1,0,0,X,X,X,X];

" check assertion of RAS2 for another shadow of dram
    [1,1,1,1,1,1,0,1,0,0,1,0,0,0] -> [0,1,0,0,X,X,X,X];
    [1,1,1,1,1,1,0,1,0,1,1,0,0,0] -> [0,1,0,0,X,X,X,X];
    [1,1,1,1,1,1,0,1,1,0,1,0,0,0] -> [0,1,X,X,X,X,X,X];
    [1,1,1,1,1,1,0,1,1,1,1,0,0,0] -> [0,1,X,X,X,X,X,X];
    [1,1,1,1,1,1,1,0,0,0,1,0,0,0] -> [0,1,0,0,X,X,X,X];
    [1,1,1,1,1,1,1,0,0,1,1,0,0,0] -> [0,1,0,0,X,X,X,X];
    [1,1,1,1,1,1,1,0,1,0,1,0,0,0] -> [0,1,0,0,X,X,X,X];
    [1,1,1,1,1,1,1,0,1,1,1,0,0,0] -> [0,1,0,0,X,X,X,X];

" check assertion of RAS2 for another shadow of dram
    [1,1,1,1,1,0,0,1,0,0,1,0,0,0] -> [0,1,0,0,X,X,X,X];
    [1,1,1,1,1,0,0,1,0,1,1,0,0,0] -> [0,1,0,0,X,X,X,X];
    [1,1,1,1,1,0,0,1,1,0,1,0,0,0] -> [0,1,X,X,X,X,X,X];
    [1,1,1,1,1,0,0,1,1,1,1,0,0,0] -> [0,1,X,X,X,X,X,X];
    [1,1,1,1,1,0,1,0,0,0,1,0,0,0] -> [0,1,0,0,X,X,X,X];
    [1,1,1,1,1,0,1,0,0,1,1,0,0,0] -> [0,1,0,0,X,X,X,X];
    [1,1,1,1,1,0,1,0,1,0,1,0,0,0] -> [0,1,0,0,X,X,X,X];
    [1,1,1,1,1,0,1,0,1,1,1,0,0,0] -> [0,1,0,0,X,X,X,X];

" check assertion of SOE0, SOE1 - simulate the sequence of the SRT, SSRT
    [0,0,0,0,0,0,0,1,0,0,0,0,0,0] -> [0,0,0,0,X,X,X,X];     " Begin of SRT
    [0,0,0,0,0,0,0,1,0,0,1,0,0,0] -> [0,0,0,1,0,0,X,X];
    [0,0,0,0,0,0,0,1,0,0,1,0,1,0] -> [0,0,0,1,1,0,X,1];
    [0,0,0,0,0,0,0,1,0,0,0,0,0,0] -> [0,0,0,0,1,0,X,1];
    [0,0,0,0,0,0,0,1,0,0,0,0,0,1] -> [0,0,0,0,1,0,0,1];     " Begin of SSRT
    [0,0,0,0,0,0,0,1,0,0,1,0,0,1] -> [0,0,0,1,1,0,0,0];
    [0,0,0,0,0,0,0,1,0,0,1,0,1,1] -> [0,0,0,1,1,0,0,0];
    [0,0,0,0,0,0,0,1,0,0,0,0,0,1] -> [0,0,0,0,1,0,0,0];
    [0,0,0,0,0,0,1,0,0,0,0,0,0,0] -> [0,0,0,0,1,0,X,0];     " Data cycle
    [0,0,0,0,0,0,1,0,0,0,1,0,0,0] -> [0,0,0,1,1,0,X,0];
    [0,0,0,0,0,0,1,0,0,0,1,0,1,0] -> [0,0,0,1,1,0,X,0];
```

```
    [0,0,0,0,0,0,1,0,0,0,0,0,0,0] -> [0,0,0,0,1,0,X,0];
    [0,0,0,0,0,1,0,1,0,0,0,0,0,0] -> [0,0,0,0,1,0,X,0];      " Begin of SRT
    [0,0,0,0,0,1,0,1,0,0,1,0,0,0] -> [0,0,1,0,0,0,1,0];
    [0,0,0,0,0,1,0,1,0,0,1,0,1,0] -> [0,0,1,0,0,1,X,1];
    [0,0,0,0,0,1,0,1,0,0,0,0,0,0] -> [0,0,0,0,0,1,X,1];
    [0,0,0,0,0,1,0,1,0,0,0,0,0,1] -> [0,0,0,0,0,1,X,1];      " Begin of SSRT
    [0,0,0,0,0,1,0,1,0,0,1,0,0,1] -> [0,0,1,0,0,1,X,0];
    [0,0,0,0,0,1,0,1,0,0,1,0,1,1] -> [0,0,1,0,0,1,X,0];
    [0,0,0,0,0,1,0,1,0,0,0,0,0,1] -> [0,0,0,0,0,1,X,0];
    [0,0,0,0,0,0,0,0,0,0,0,0,0,0] -> [0,0,0,0,0,1,X,0];      " Data cycle
    [0,0,0,0,0,0,0,0,0,0,0,1,0,0] -> [0,0,0,1,0,1,X,0];
    [0,0,0,0,0,0,0,0,0,0,0,1,0,1] -> [0,0,0,1,0,1,X,0];
    [0,0,0,0,0,0,0,0,0,0,0,0,0,0] -> [0,0,0,0,0,1,X,0];

END _RASDCD
```

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ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a four-part type number as shown in the following example.

Example:	**TL**	**598M**	**J**	**/883B**

Prefix

MUST CONTAIN TWO OR THREE LETTERS

SN ..... TI Special Functions or Interface Products
TL, TLE ..... TI Linear Products
TLC ..... TI Linear Silicon-Gate CMOS Products

STANDARD SECOND-SOURCE PREFIXES

AD ..... Analog Devices
ADC, LF, LM, LP, or MP ..... National
LT or LTC ..... Linear Technology
MC ..... Motorola
NE, SA, or SE ..... Signetics
OP ..... PMI
RC, RM, or RV ..... Raytheon
uA ..... Fairchild/National
UC ..... Unitrode

Unique Circuit Description Including Temperature Range

MUST CONTAIN TWO OR MORE CHARACTERS
(From Individual Data Sheets)

Examples:	10	34070
	592	1451AC
	7757	2217-285

Package

MUST CONTAIN ONE OR TWO LETTERS

D, DB, DW, FK, FN, J, JD, JG, KC, KK, KV, LP, N, NS, NT, NW, P, PK, PW, U
(From Pin-Connection Diagrams on Individual Data Sheet)

MIL-STD-883B, Method 5004, Class B

Omit /883B When Not Applicable

ORDERING INSTRUCTIONS

Circuits are shipped in one of the carriers below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped via the most practical carrier.

Dual-In-Line (J, JD, JG, N, NT, NS, NW, P)
– A-Channel Antistatic or Conductive Plastic Tubing

Small Outline (D, DW)
– Tape and Reel
– Antistatic or Conductive Plastic Tubing

Shrink Small Outline (DB)
– Tape and Reel

Thin Shrink Small Outline (PW)
– Tape and Reel

Chip Carriers (FK, FN)
– Antistatic or Conductive Plastic Tubing

Flat (U)
– Milton Ross Carriers

Plug-In (LP)
– Plastic Bag
– Tape and Reel

Power Tab (KC, KK, KV)
– A-Channel Antistatic or Conductive Plastic Tubing

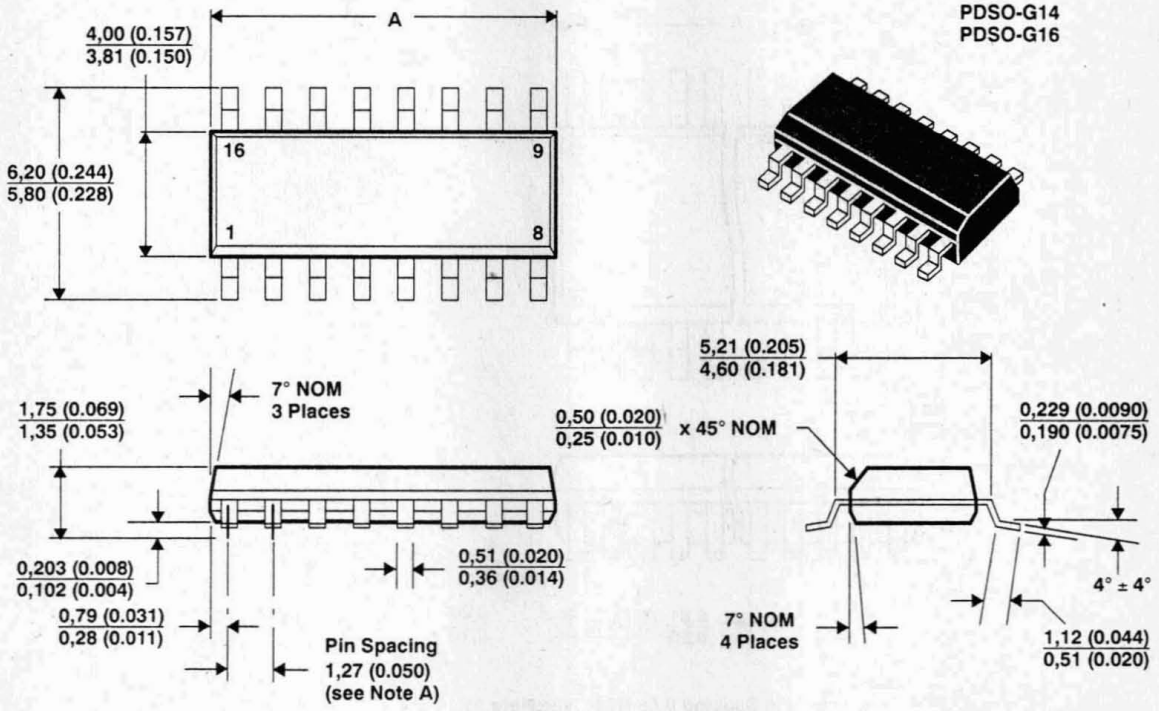
D008, D014, and D016
plastic small-outline packages

Each of these small-outline packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

D008, D014, and D016
(16-pin package used for illustration)

Designation per JEDEC Std 30:

PDSO-G8
PDSO-G14
PDSO-G16



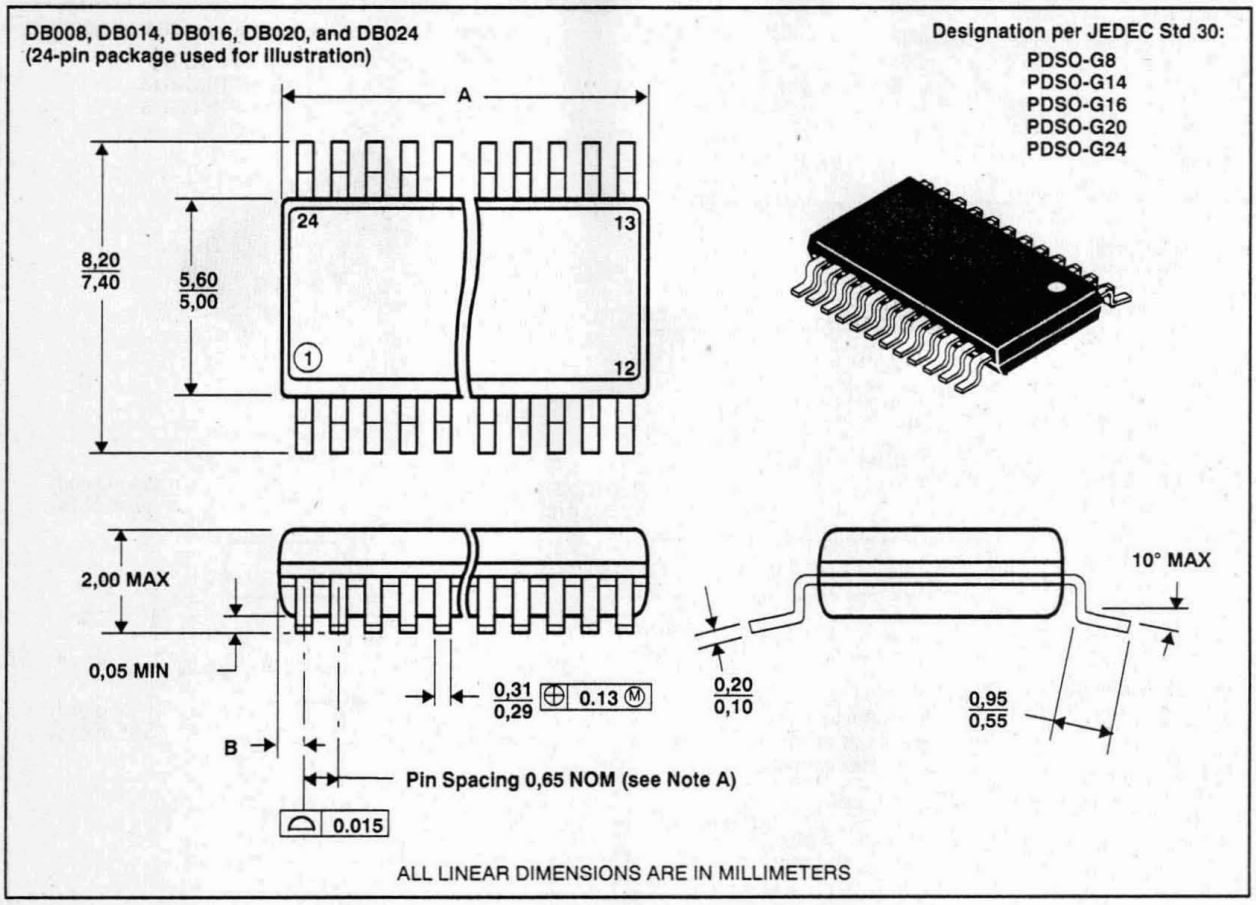
DIM \ PINS	8	14	16
A MIN	4,80 (0.189)	8,55 (0.337)	9,80 (0.386)
A MAX	5,00 (0.197)	8,74 (0.344)	10,00 (0.394)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: C. Leads are within 0,25 (0.010) radius of true position at maximum material condition.
D. Body dimensions do not include mold flash or protrusion.
E. Mold flash or protrusion shall not exceed 0,15 (0.006).
F. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

DB008, DB014, DB016, DB020, and DB024 shrink small-outline packages

These shrink small-outline packages consist of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Leads are within 0,25 mm radius of true position at maximum material condition.
B. Body dimensions do not include mold flash or protrusion.
C. Mold or flash end protrusion shall not exceed 0,15 mm.
D. Interlead flash shall be controlled by TI statistical process control (additional information available through TI field office).
E. Lead tips to be planar within ±0,05 mm exclusive of solder.

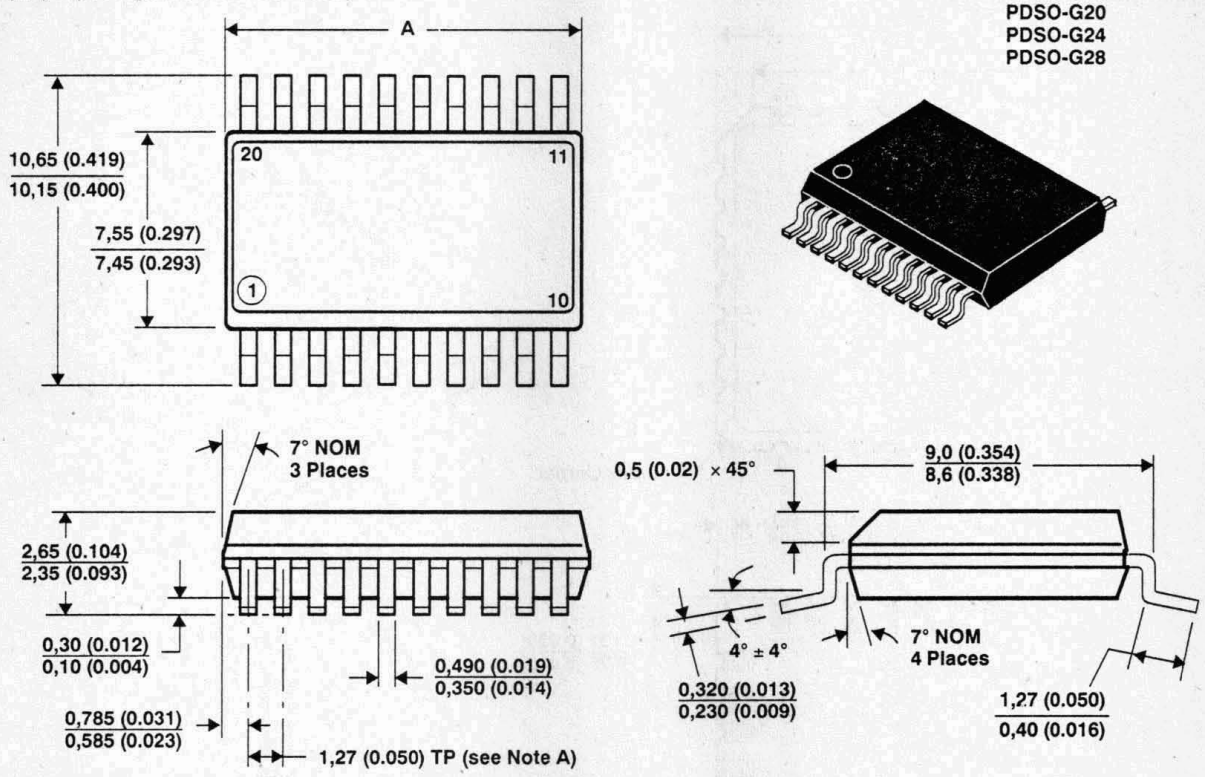
DIM \ PINS	8	14	16	20	24
A MIN	2,70	5,90	5,90	6,90	7,90
A MAX	3,30	6,50	6,50	7,50	8,50
B MAX	0,68	1,30	0,98	0,83	0,68

DW016, DW020, DW024, and DW028
plastic small-outline packages

Each of these small-outline packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

DW016, DW020, DW024, and DW028
(20-pin package used for illustration)

Designation per JEDEC Std 30:
PDSO-G16
PDSO-G20
PDSO-G24
PDSO-G28



DIM \ PINS	16	20	24	28
A MIN	10,16 (0.400)	12,70 (0.500)	15,29 (0.602)	17,68 (0.696)
A MAX	10,36 (0.408)	12,90 (0.508)	15,49 (0.610)	17,88 (0.704)

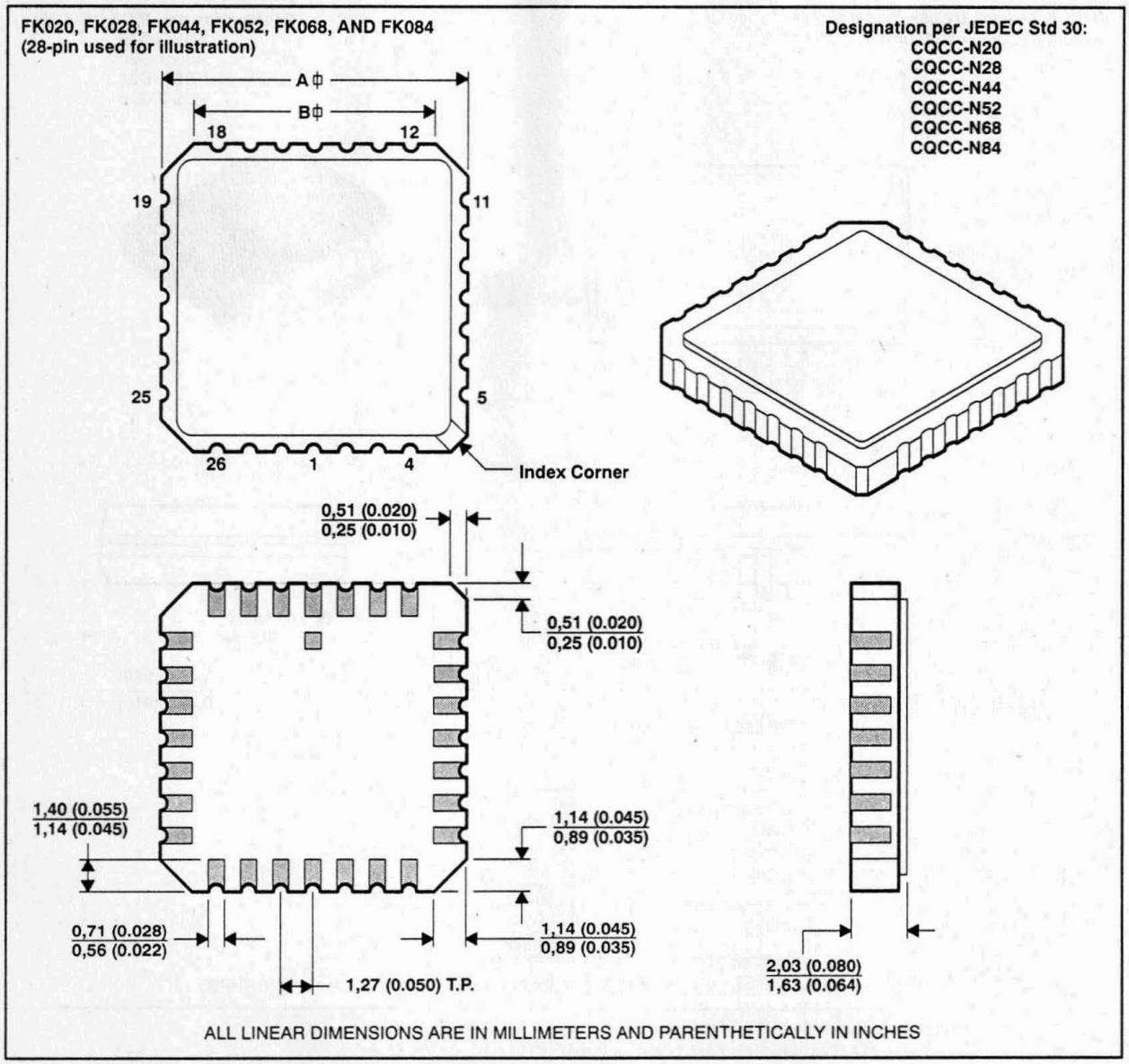
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material condition.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed, 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

FK020, FK028, FK044, FK052, FK068, and FK084 ceramic chip carrier

Each of these hermetically sealed chip carrier packages has a three-layer ceramic base with a metal lid and braze seal. These packages are intended for surface mounting on solder leads on 1,27 (0.050) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

FK package terminal assignments conform to JEDEC Standards 1 and 2.



NOTES: A. See next page for A and B dimensions.

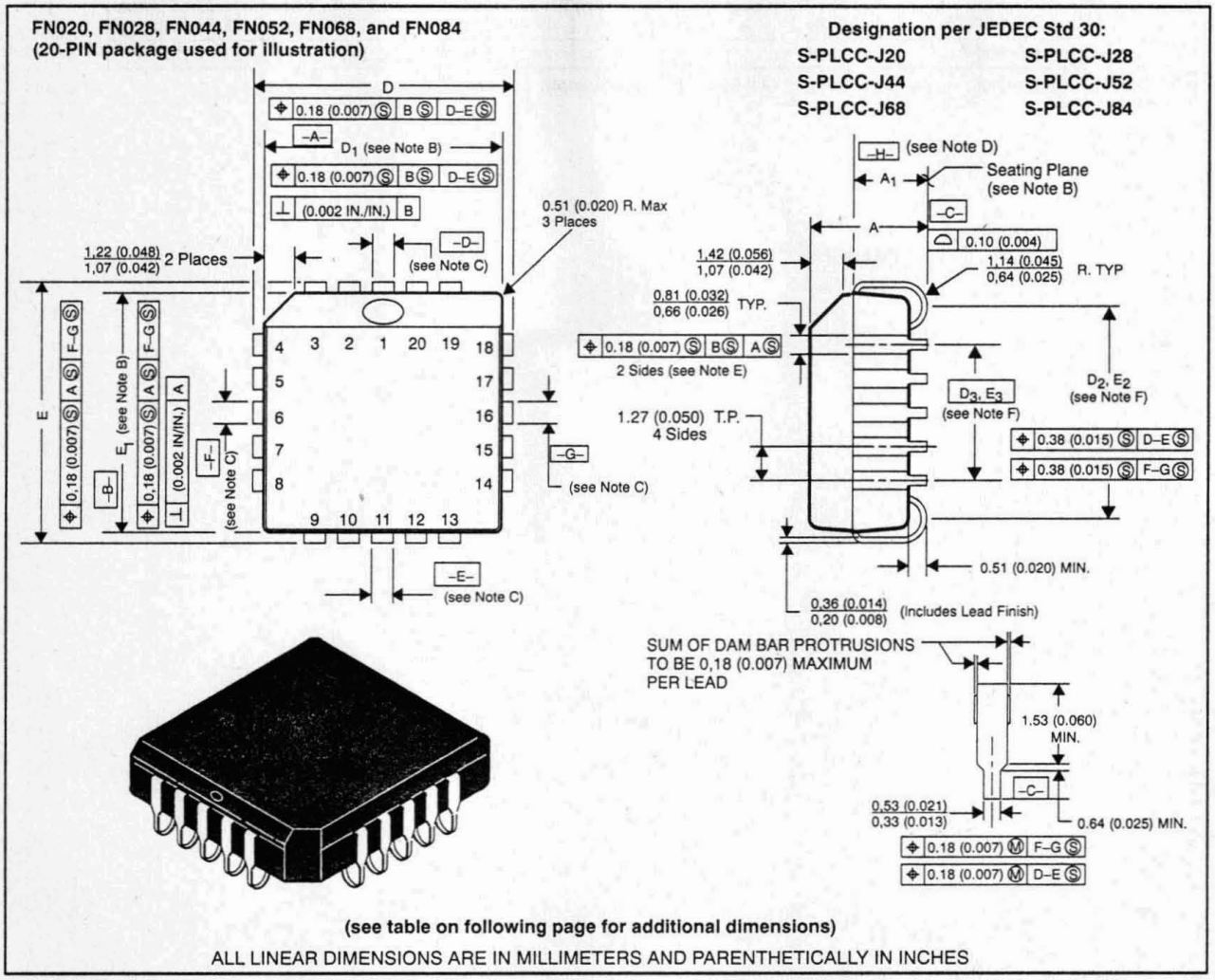
FK020, FK028, FK044, FK052, FK068, and FK084 ceramic chip carrier (continued)

JEDEC OUTLINE DESIGNATION†	NUMBER OF TERMINALS	A		B	
		MIN	MAX	MIN	MAX
MS-004-CB	20	8,69 (0.342)	9,09 (0.358)	7,80 (0.307)	9,09 (0.358)
MS-004-CC	28	11,23 (0.442)	11,63 (0.458)	10,31 (0.406)	11,63 (0.458)
MS-004-CD	44	16,26 (0.640)	16,76 (0.660)	12,58 (0.495)	14,22 (0.560)
MS-004-CE	52	18,78 (0.740)	19,32 (0.760)	12,58 (0.495)	14,22 (0.560)
MS-004-CF	68	23,83 (0.938)	24,43 (0.962)	21,60 (0.850)	21,80 (0.858)
MS-004-CG	84	28,99 (1,141)	29,59 (1.164)	26,60 (1.047)	27,00 (1,063)

† All dimensions and notes for the specified JEDEC outline apply.

FN020, FN028, FN044, FN052, FN068, and FN084
plastic J-leaded chip carrier

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The package is intended for surface mounting on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.



(see table on following page for additional dimensions)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: B. All dimensions conform to JEDEC Specification MO-047AA/AF. Dimensions and tolerancing are per ANSI Y14.5M – 1982.

C. Dimensions D_1 and E_1 do not include mold flash protrusion. Protrusion shall not exceed 0,25 (0.010) on any side. Centerline of center pin each side is within 0,10 (0.004) of package centerline by dimension B. The lead contact points are planar within 0,10 (0.004).

D. Datums [D – E] and [F – G] for center leads are determined at datum [– H –].

E. Datum [– H –] is located at top of leads where they exit plastic body.

F. Location of datums [– A –] and [– B –] to be determined at datum [– H –].

G. Determined at seating plane [– C –].

FN020, FN028, FN044, FN052, FN068, and FN084 plastic J-leaded chip carrier (continued)

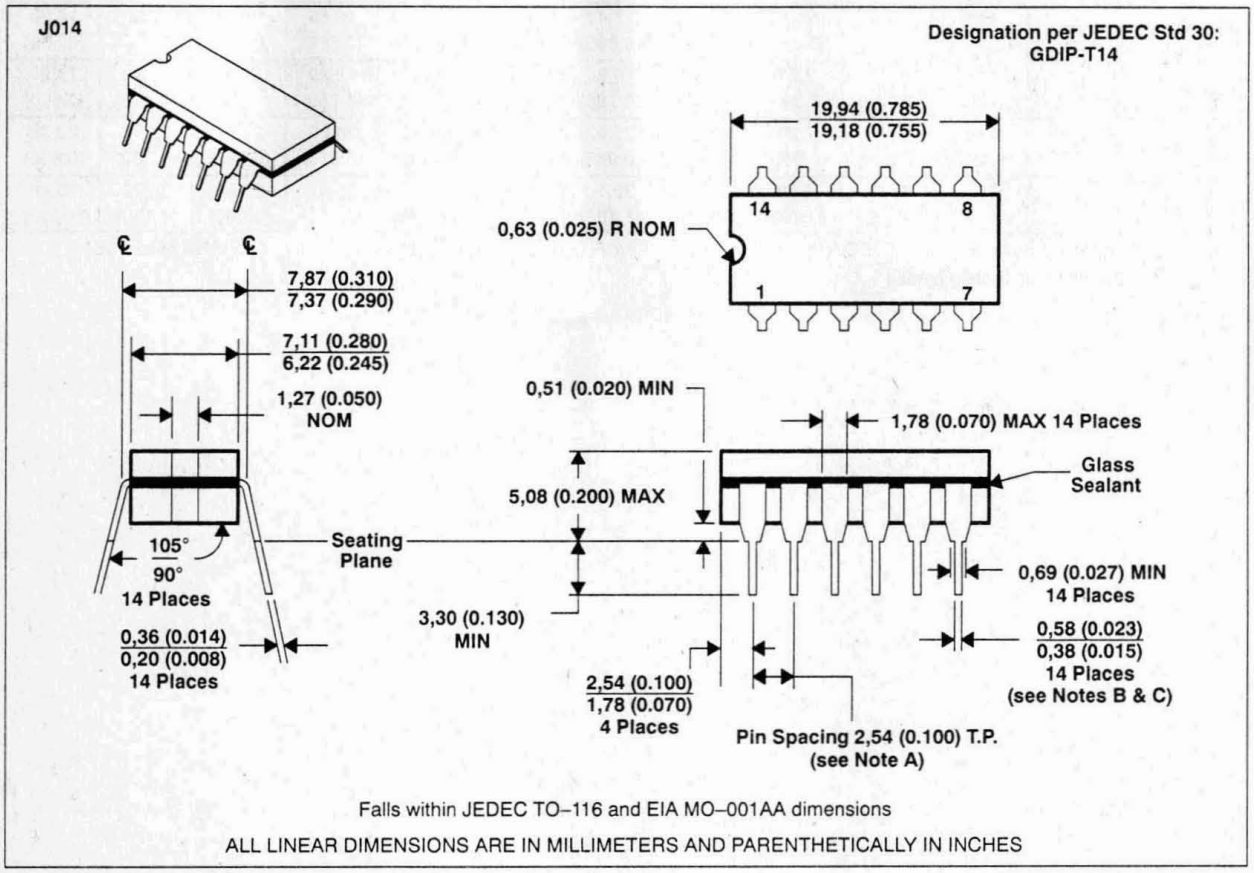
JEDEC OUTLINE	NO.OF PINS	A		A_1		D, E		D_1, E_1		D_2, E_2		D_3, E_3
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	BASIC
MO-047AA	20	4,19 (0.165)	4,57 (0.180)	2,29 (0.090)	3,05 (0.120)	9,78 (0.385)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	7,37 (0.290)	8,38 90.330)	5,08 (0.200)
MO-047AB	28	4,19 (0.165)	4,57 (0.180)	2,29 (0.090)	3,05 (0.120)	12,32 (0.485)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	9,91 (0.390)	10,92 (0.430)	7,62 (0.300)
MO-047AC	44	4,19 (0.165)	4,57 (0.180)	2,29 (0.090)	3,05 (0.120)	17,40 (0.685)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	14,99 (0.590)	16,00 (0.630)	12,70 (0.500)
MO-047AD	52	4,19 (0.165)	5,08 (0.200)	2,29 (0.090)	3,30 (0.130)	19,94 (0.785)	20,19 (0.795)	19,05 (0.750)	19,20 (0.756)	17,53 (0.690)	18,54 (0.730)	15,24 (0.600)
MO-047AE	68	4,19 (0.165)	5,08 (0.200)	2,29 (0.090)	3,30 (0.130)	25,02 (0.985)	25,27 (0.995)	24,13 (0.950)	24,33 (0.958)	22,61 (0.890)	23,62 (0.930)	20,32 (0.800)
MO-047AF	84	4,19 (0.165)	5,08 (0.200)	2,29 (0.090)	3,30 (0.130)	30,10 (1.185)	30,35 (1.195)	29,21 (1.150)	29,41 (1.141)	27,69 (1.090)	28,70 (1.130)	25,40 (1.000)

NOTES A: All dimensions conform to JEDEC Specification MO-047AA/AF. Dimensions and tolerancing are per ANSI Y14.5M – 1982.

F: Determined at seating plane $\boxed{-C-}$.

J014
ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.



Falls within JEDEC TO–116 and EIA MO–001AA dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

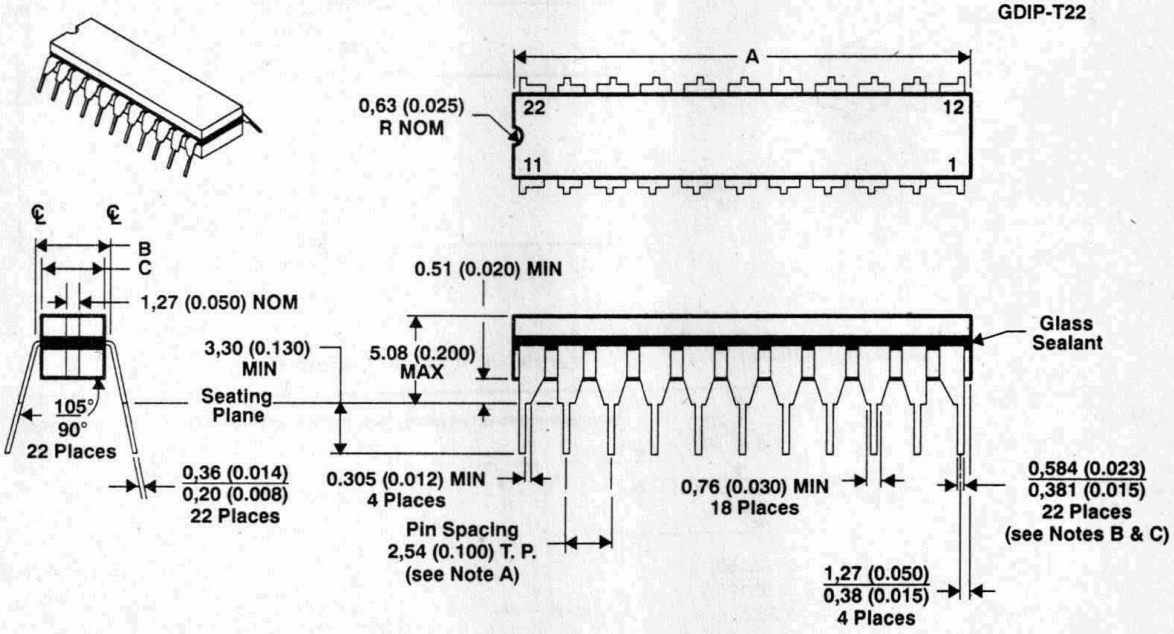
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

J016, J018, J020, and J022 ceramic dual-in-line

These hermetically sealed dual-in-line packages consist of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. These packages are intended for insertion in mounting-hole rows of 7,62 (0.300) centers for the J016, J018, J020, and 10,16 (0.400) centers for the J022, respectively. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (bright-dipped) leads require no additional cleaning or processing when used in solder assembly.

J016, J018, J020, and J022
(22-pin package used for illustration)

Designation per JEDEC Std 30:
GDIP-T16
GDIP-T18
GDIP-T20
GDIP-T22



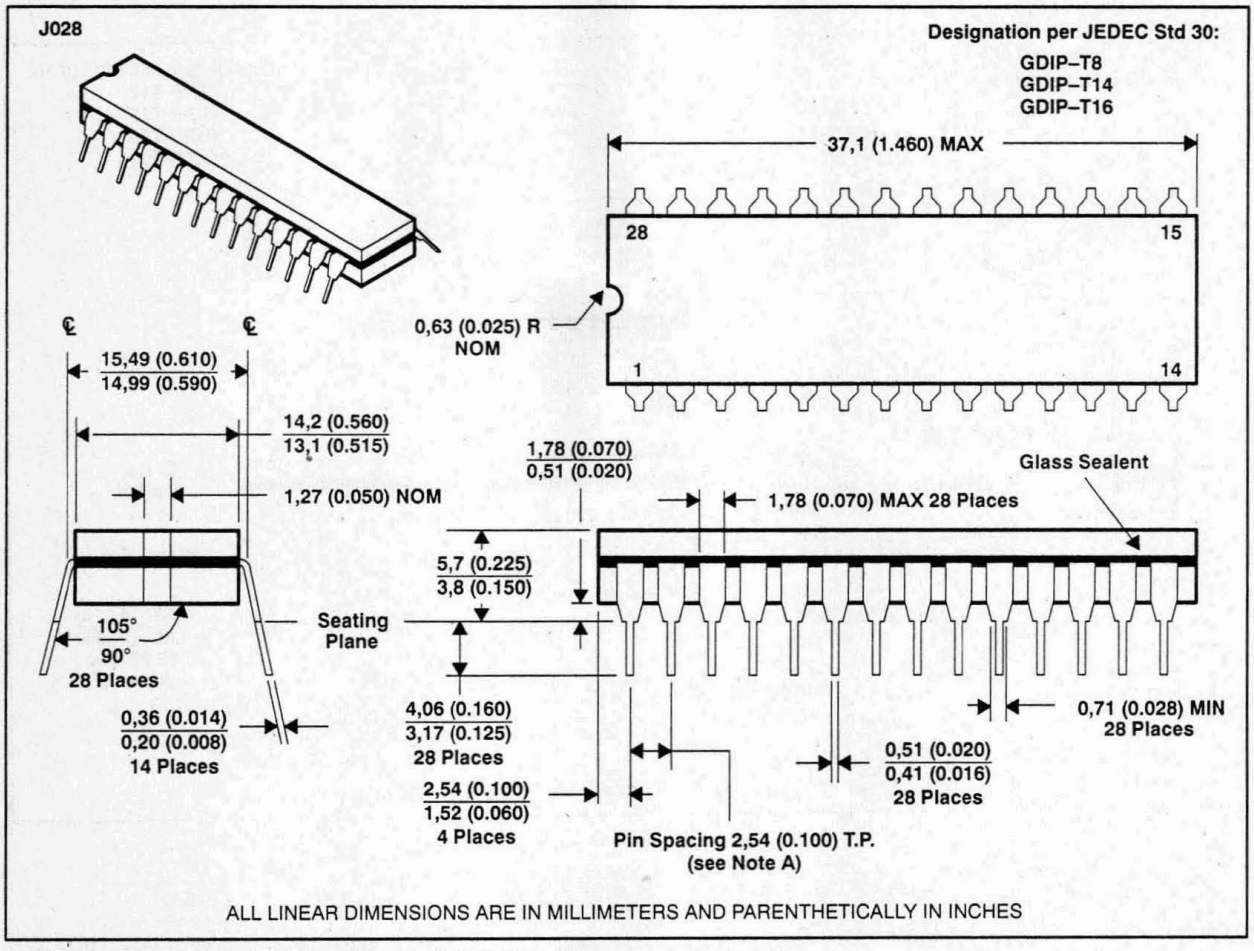
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

DIM / PINS	A		B		C	
	MIN	MAX	MIN	MAX	MIN	MAX
16	19,18 (0.755)	19,94 (0.785)	7,37 (0.290)	7,87 (0.310)	6,22 (0.245)	7,62 (0.300)
18		23,1 (0.910)	7,37 (0.290)	7,87 (0.310)	6,22 (0.245)	7,62 (0.300)
20	23,62 (0.930)	24,76 (0.975)	7,37 (0.290)	7,87 (0.310)	6,22 (0.245)	7,62 (0.300)
22		28,0 (1.100)	9,91 (0.390)	10,41 (0.410)		9,65 (0.388)

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

J028
ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting hole rows on 15,24 (0.600) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.



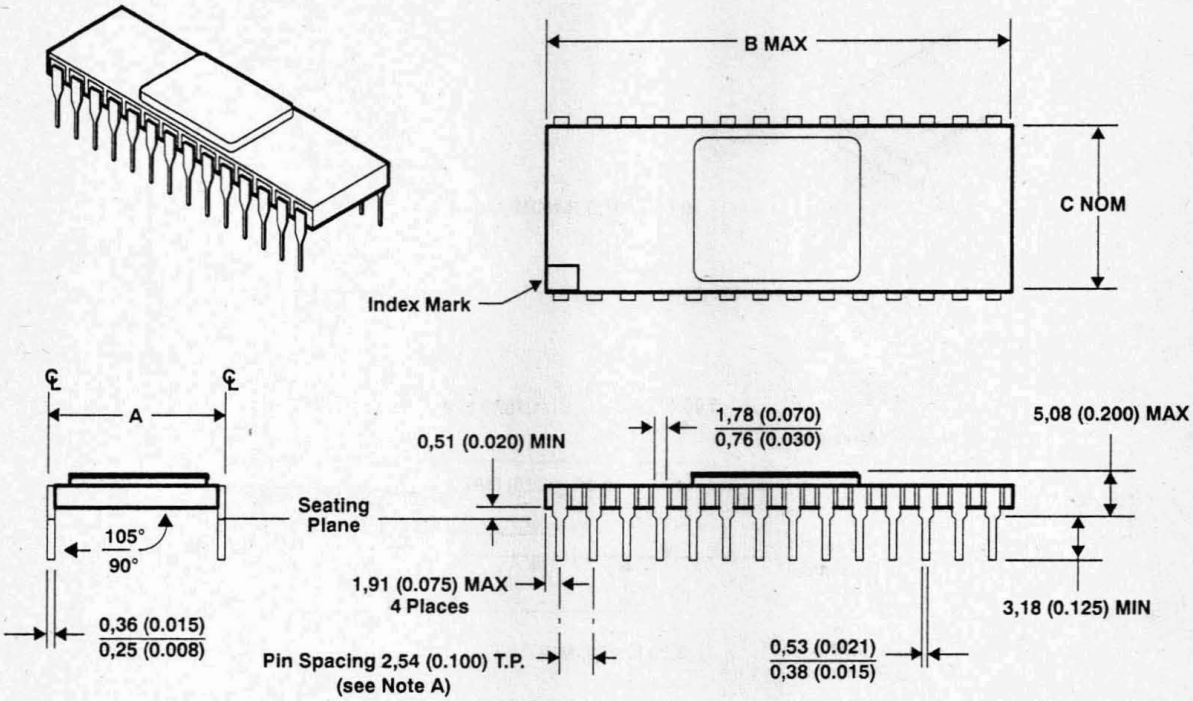
NOTES: D. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
E. This dimension does not apply for solder-dipped leads.
F. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

JD024 and JD028
ceramic side-braze dual-in-line packages

These hermetically sealed dual-in-line packages consist of a ceramic base, metal cap, and side-brazed tin-plated leads. These packages are intended for insertion in mounting-hole rows of 15,24 (0.600) centers. Leads require no additional cleaning or processing when used in solder assembly.

JD024 and JD028
(28-pin package used for illustration)

Designation per JEDEC Std 30:
GDIP–T24
GDIP–T28



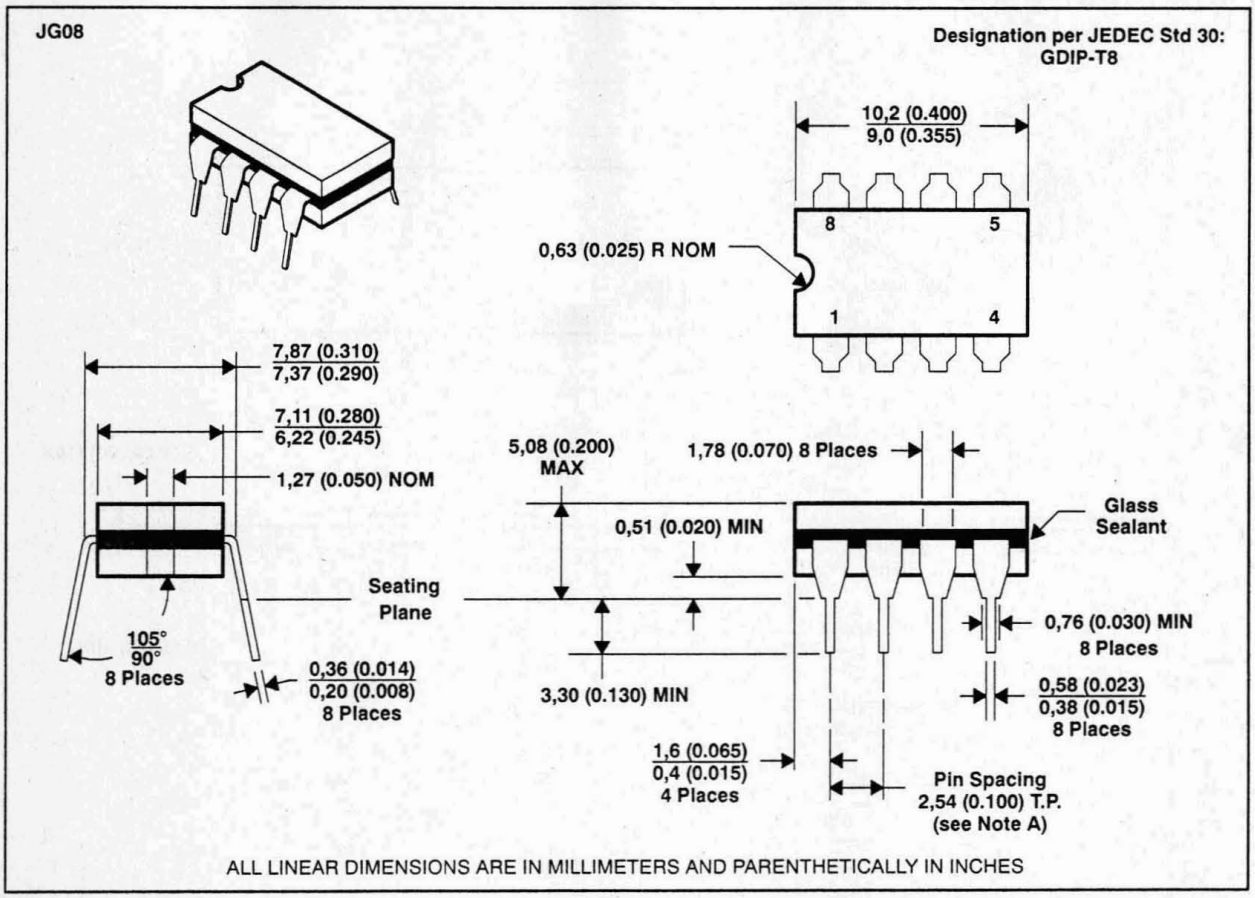
DIM \ PINS	24	28
A +0,51 (+0.020) −0,25 (−0.010)	15,24 (0.600)	15,24 (0.600)
B (MAX)	31,8 (1.250)	36,8 (1.450)
C (NOM)	15,0 (0.590)	15,0 (0.590)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

JG008
ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.



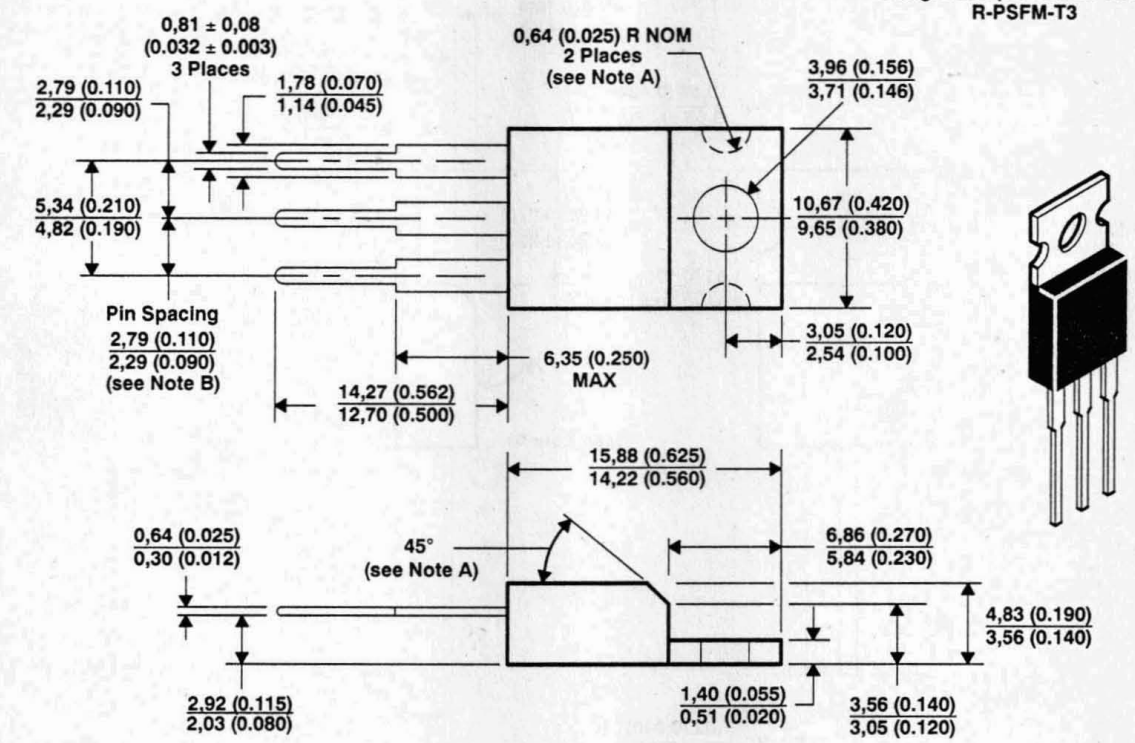
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

KC003
plastic flange-mount package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when the package is operated under high-humidity conditions.

KC003

Designation per JEDEC Std 30:
R-PSFM-T3



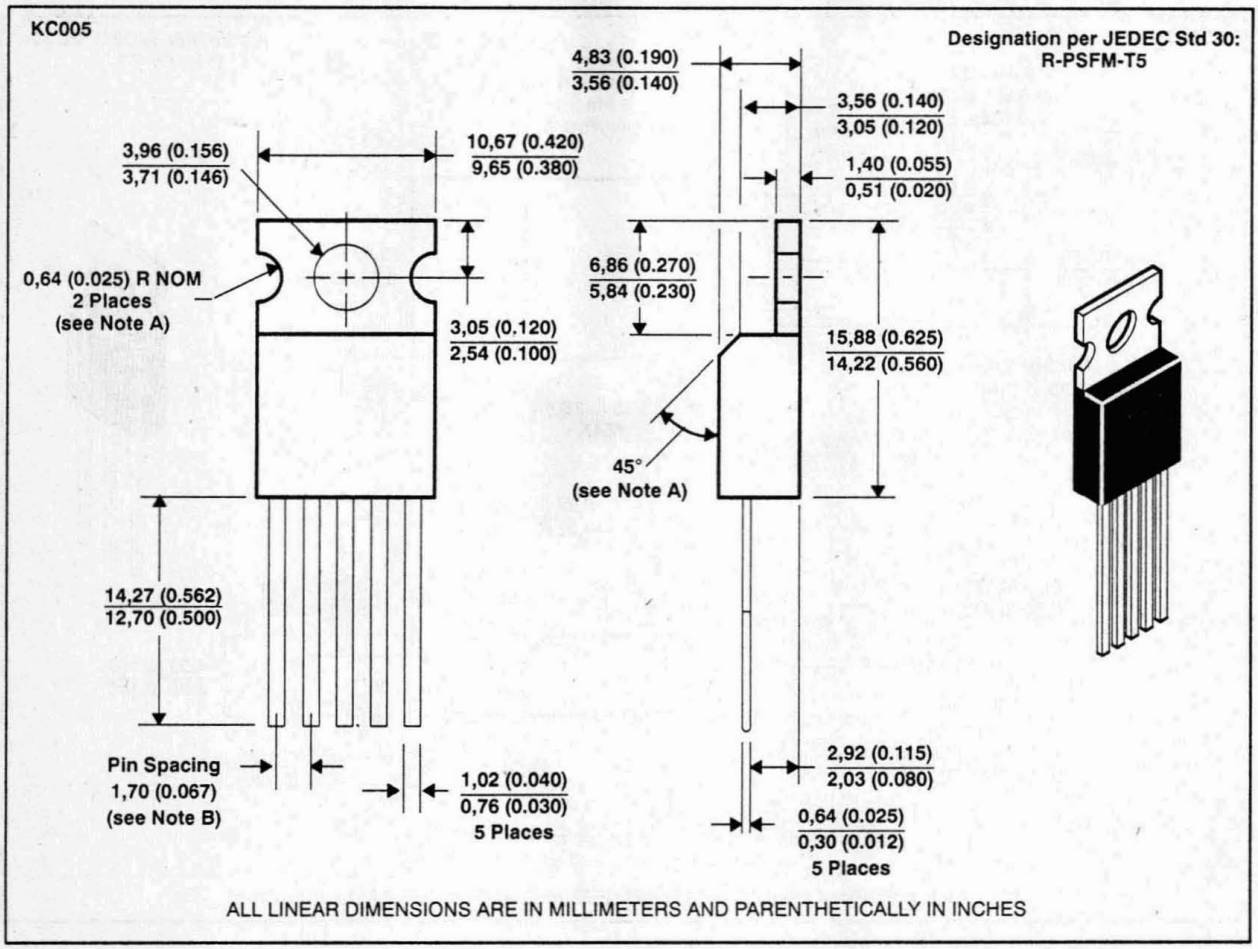
The center terminal is in electrical contact with the mounting tab.
Falls within JEDEC TO-220AB dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Notches and/or mold chamfer may or may not be present.
B. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material conditions.

KC005
plastic flange-mount package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when the package is operated under high-humidity conditions.



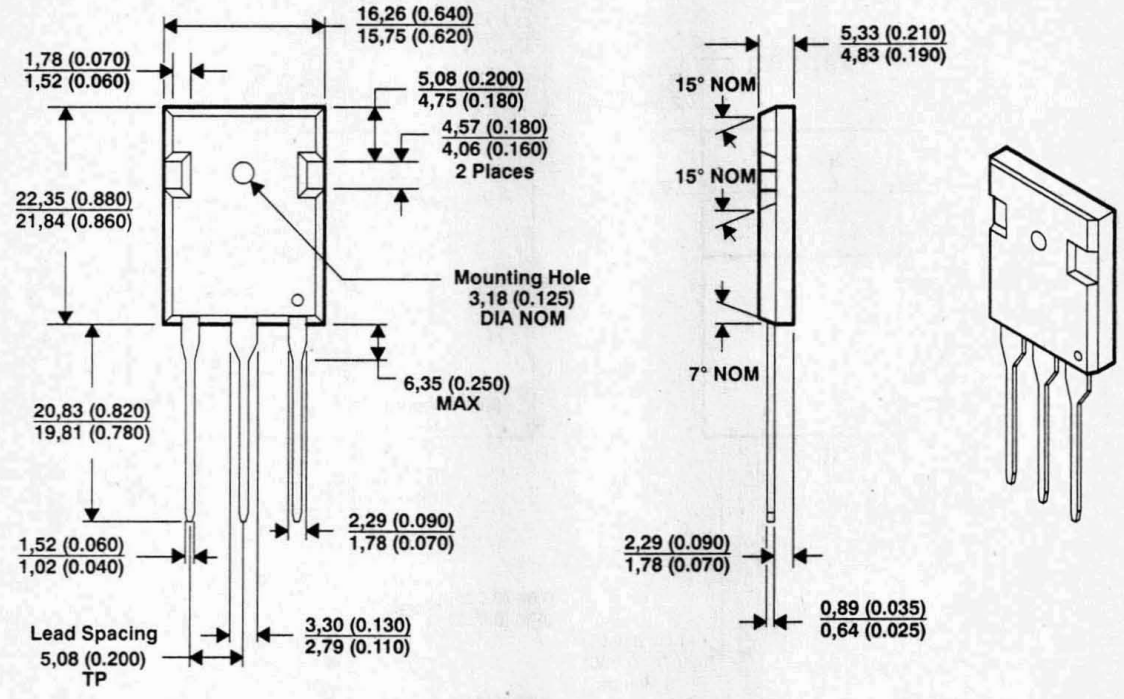
NOTES: A. Notches and chamfer may or may not be present.
B. Leads are with 0,13 (0.005) radius of true position (T.P.) at maximum material conditions.

KK003
plastic flange-mount package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when the package is operated under high-humidity conditions.

KK003

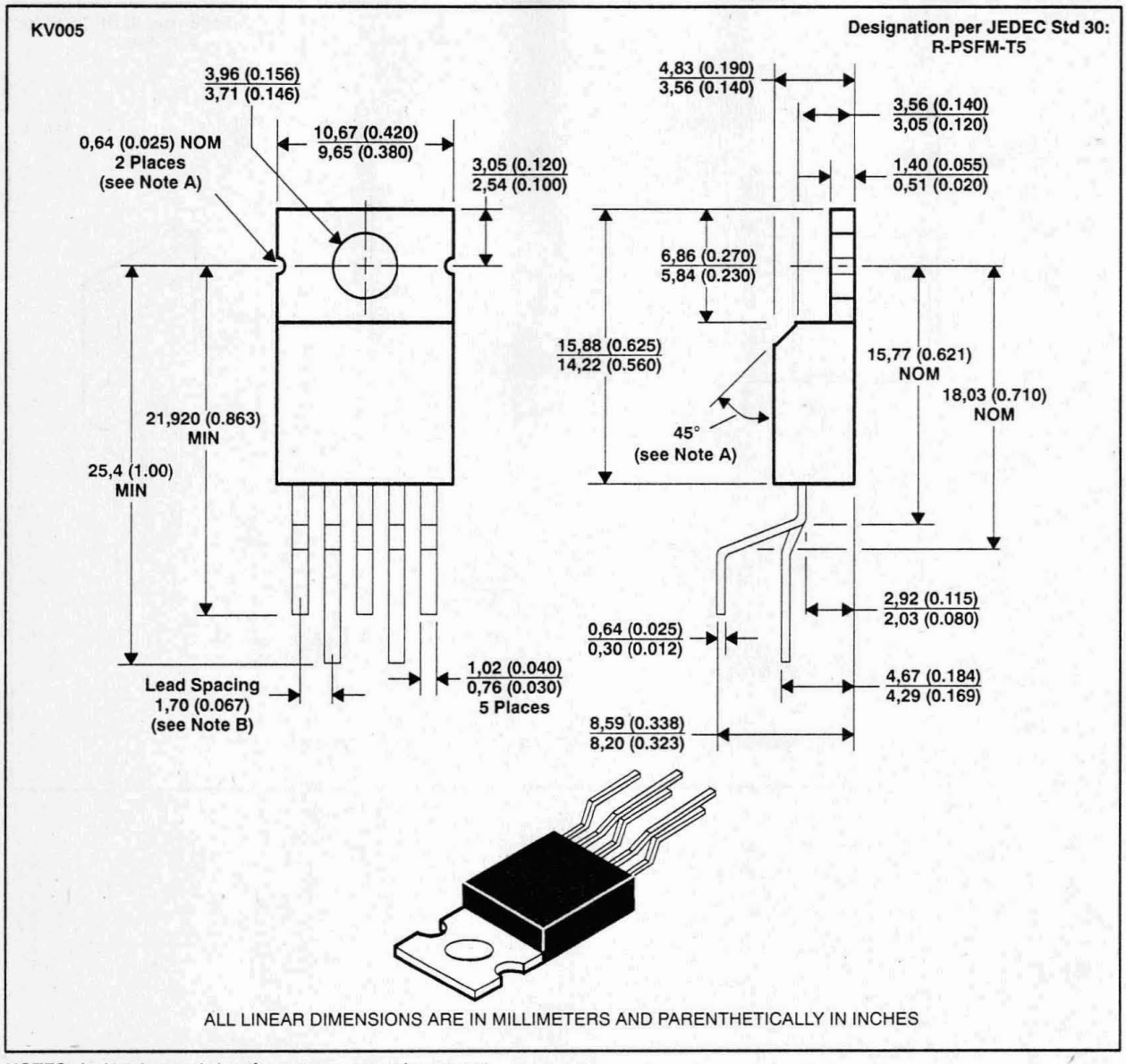
Designation per JEDEC Std 30:
X-PSFM-T3



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

KV005
plastic flange-mount package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when the package is operated under high-humidity conditions.



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

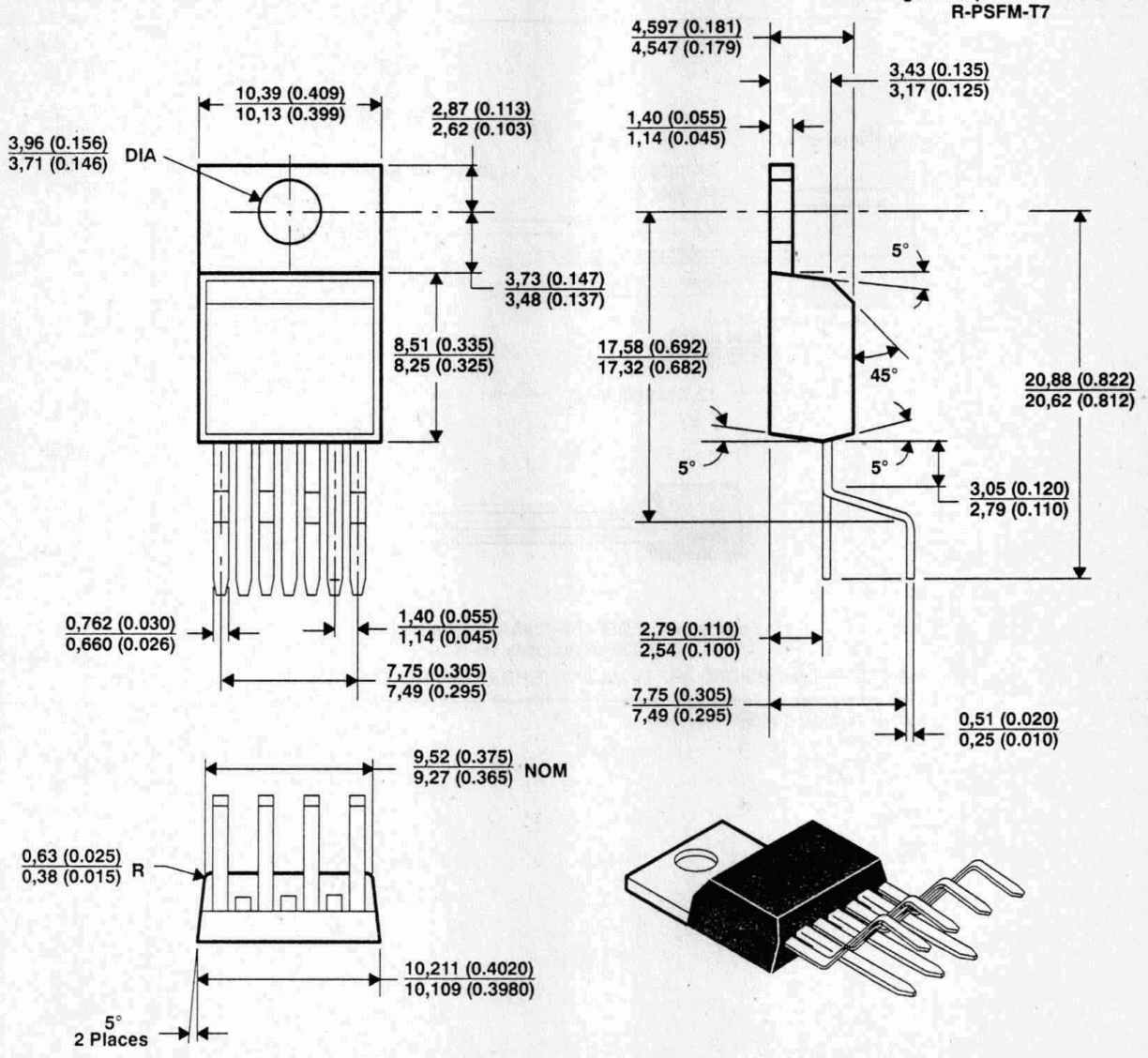
NOTES: A. Notches and chamfer may or may not be present.
B. Leads are with 0,13 (0.005) radius of true position (T.P.) at maximum material conditions.

KV007 plastic flange-mount package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when the package is operated under high-humidity conditions.

KV007

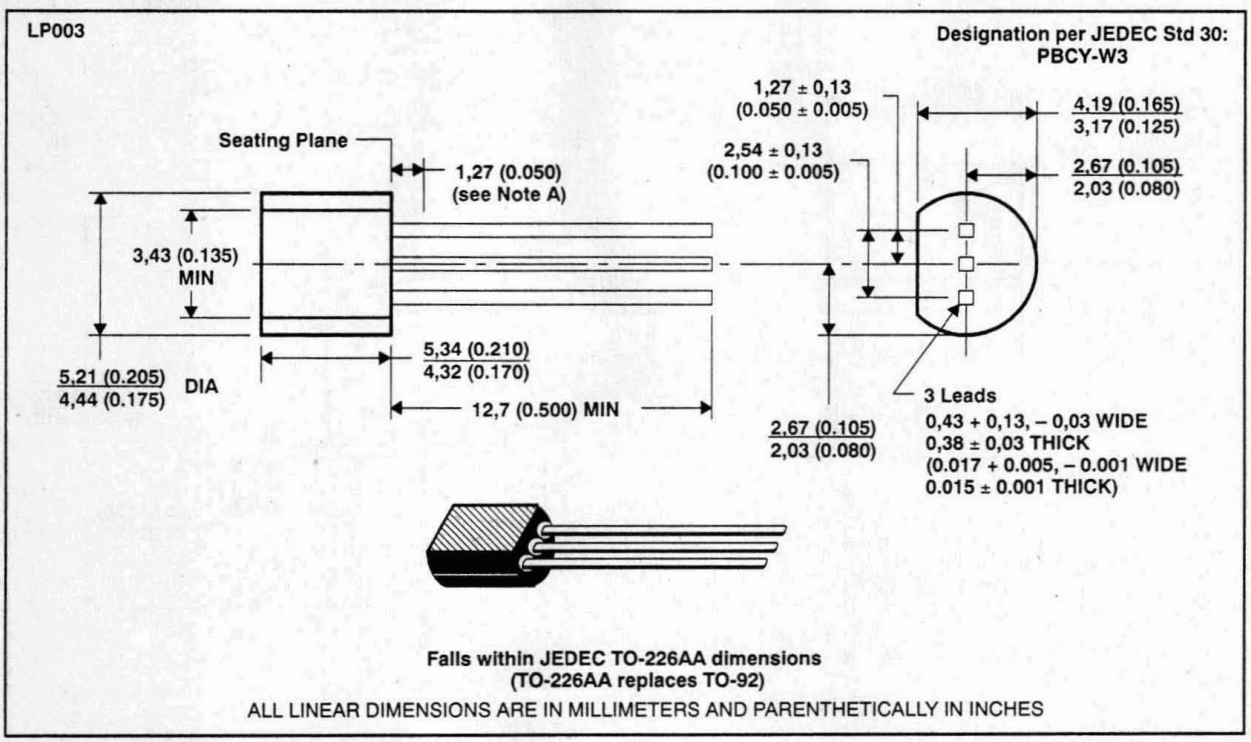
Designation per JEDEC Std 30:
R-PSFM-T7



ALL LINEAR DIMENSIONS ARE IN MILLILMETERS AND PARENTHETICALLY IN INCHES.

LP003
plastic cylindrical package

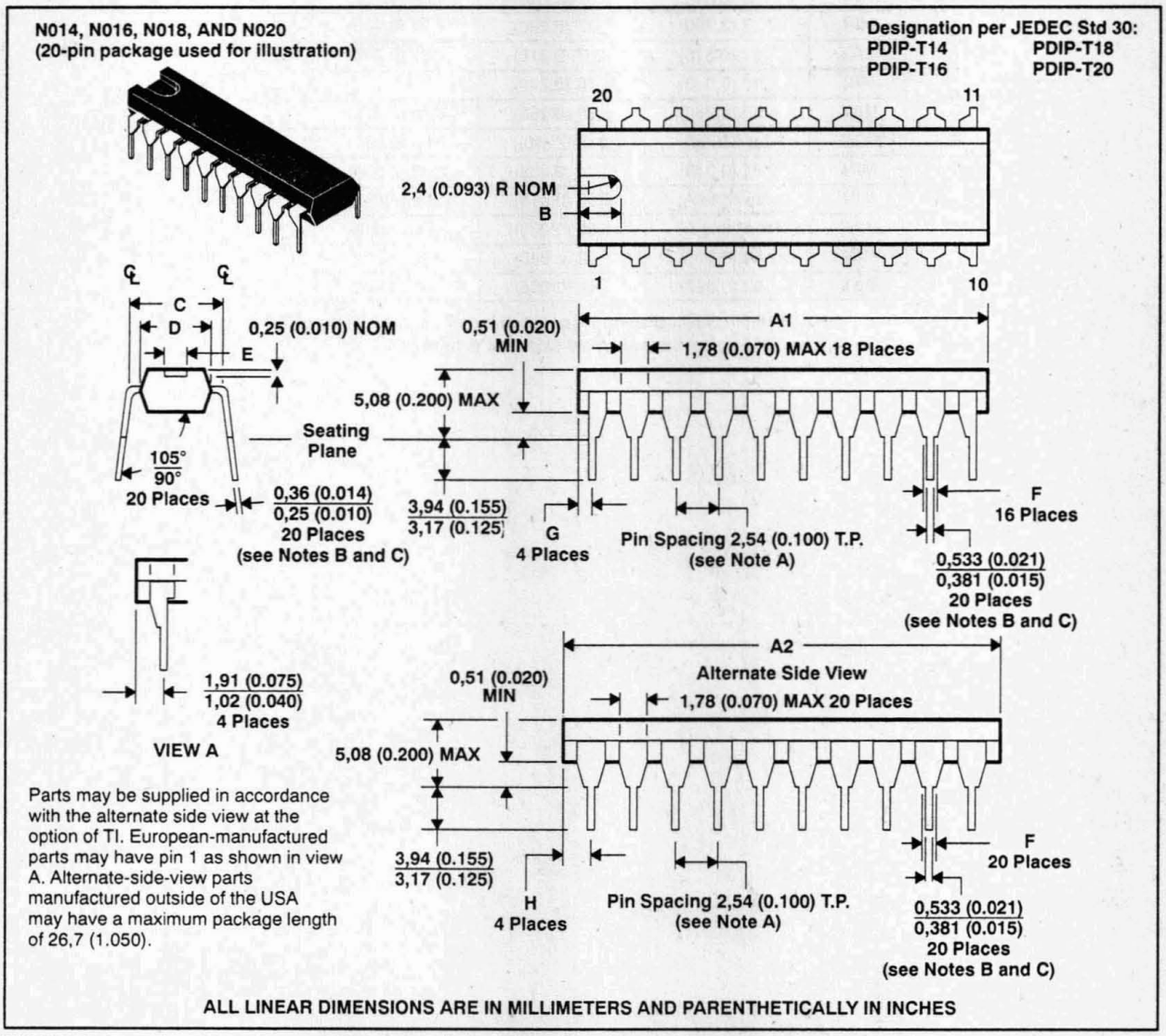
This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



NOTE A: Lead dimensions are not controlled within this area.

N014, N016, N018, and N020
300-mil plastic dual-in-line packages

These dual-in-line packages consist of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics will remain stable when operated in high-humidity conditions. These packages are intended for insertion in mounting-hole rows on 7,62 (0.300) centers . Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

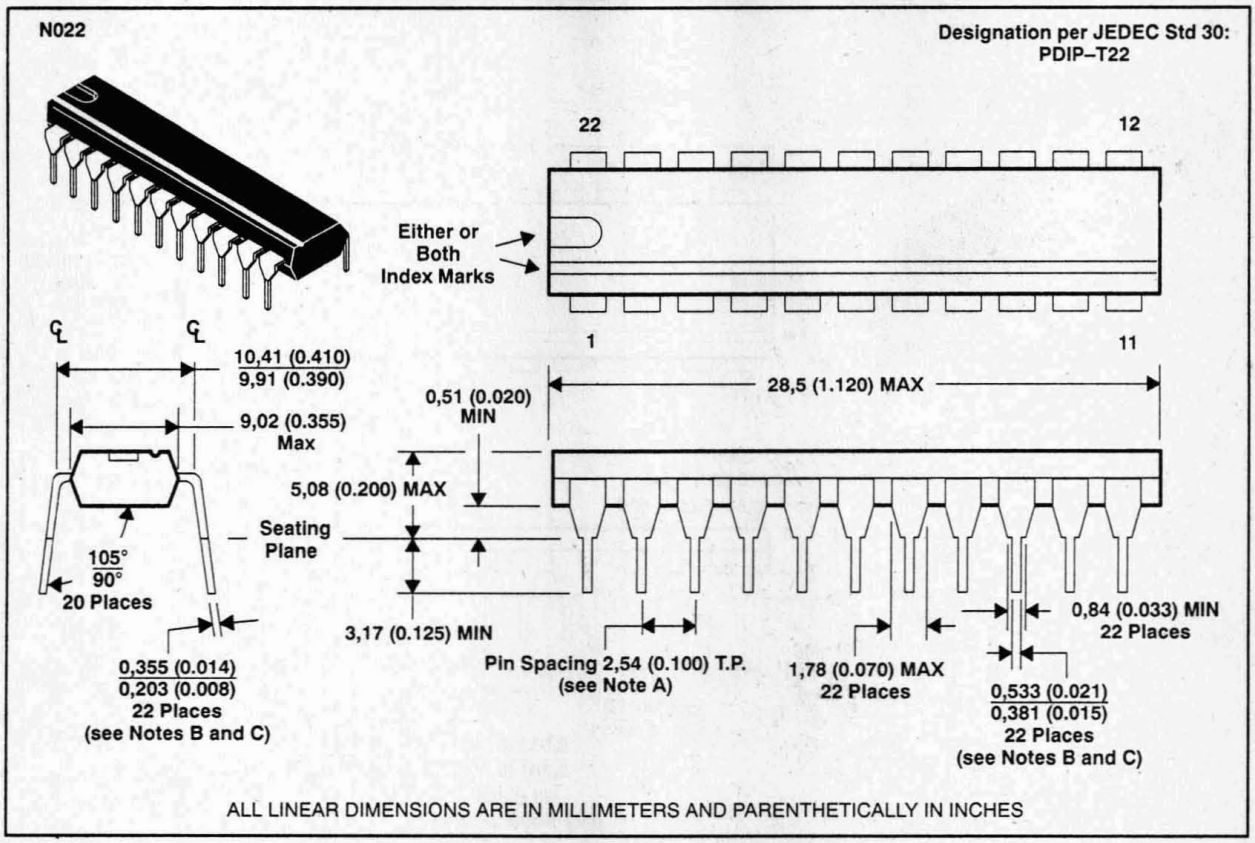
N014, N016, N018, and N020
300-mil plastic dual-in-line package (continued)

DIM \ PIN		14	16	18	20
A1	MIN	18,0 (0.710)			23,22 (0.914)
	MAX	19,8 (0.780)	19,8 (0.780)	23,4 (0.920)	24,77 (0.975)
A2	MIN	18,0 (0.710)			23,62 (0.930)
	MAX	19,8 (0.780)			25,4 (1.000)
B	NOM	2,8 (0.110)	2,8 (0.110)	4,06 (0.160)	2,80 (0.110)
C	MIN	7,37 (0.290)	7,37 (0.290)	7,37 (0.290)	7,37 (0.290)
	MAX	7,87 (0.310)	7,87 (0.310)	7,87 (0.310)	7,87 (0.310)
D	MIN	6,10 (0.240)	6,10 (0.240)		6,60 (0.240)
	MAX	6,60 (0.260)	6,60 (0.260)	6,99 (0.275)	7,11 (0.280)
E	NOM	2,0 (0.080)	2,0 (0.080)	2,03 (0.080)	2,0 (0.080)
F	MIN	0,84 (0.033)	0,84 (0.033)	0,89 (0.035)	0,84 (0.033)
G	MIN	(see Note A)	0,38 (0.015)	(See Note A)	1,68 (0.066)
	MAX	(see Note A)	1,65 (0.065)	(see Note A)	0,22 (0.009)
H	MIN	2,54 (0.100)	1,02 (0.040)	0,23 (0.009)	0,38 (0.015)
	MAX	1,52 (0.060)	2,41 (0.095)	1,91 (0.075)	1,27 (0.050)

NOTES: A. The 14-pin and 18-pin plastic dual-in-line package is only offered with the external pins shaped in their entirety, and do not have alternate side view dimensions.

N022
400-mil plastic dual-in-line package

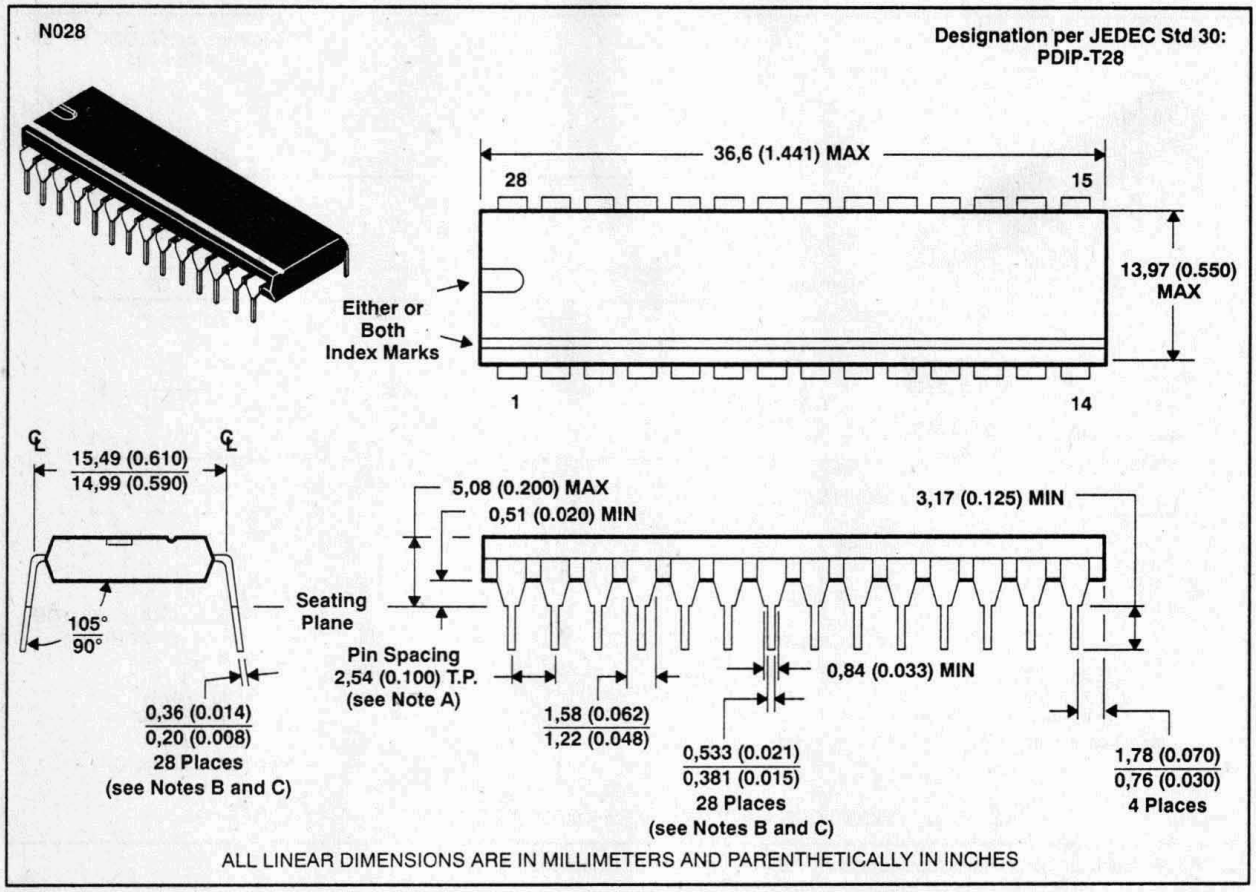
This dual-in-line package consist of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics will remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 10,16 (0.400) centers . Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: B. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
C. This dimension does not apply for solder-dipped leads.
D. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N028
600-mil plastic dual-in-line package

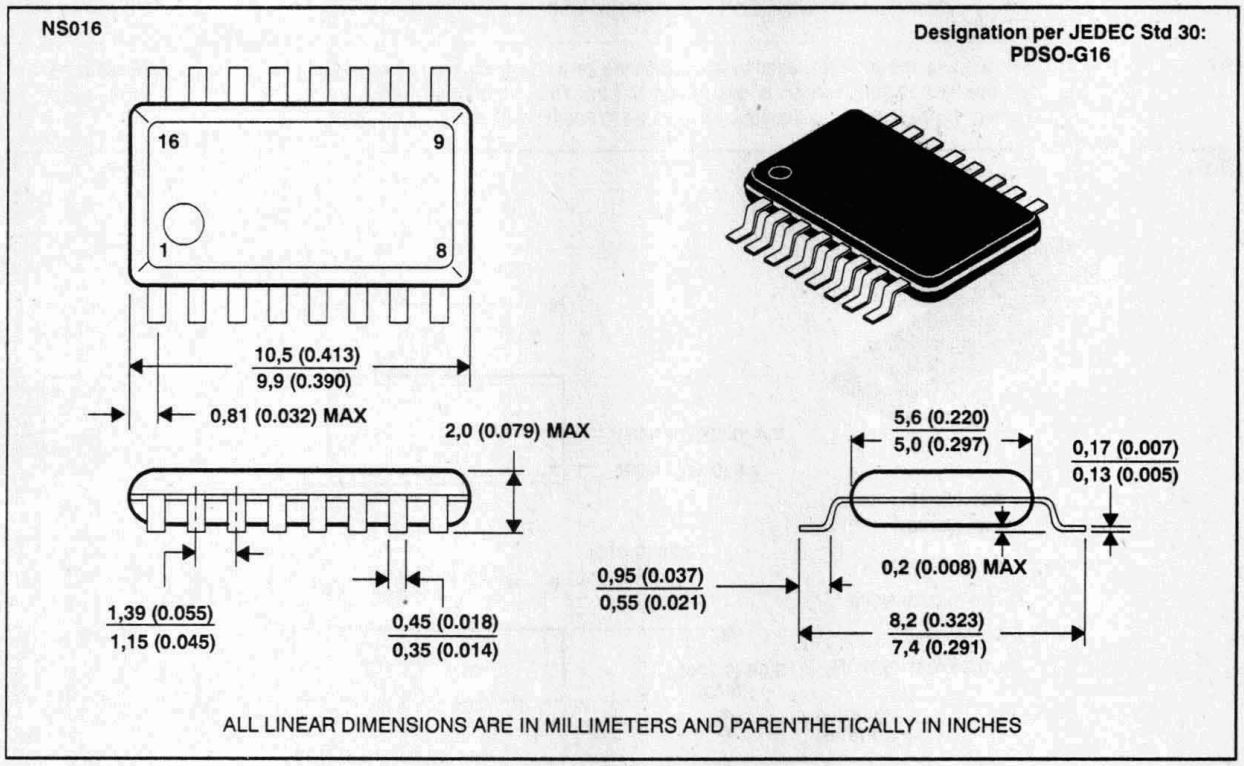
This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics will remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 15,24 (0.600) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

NS016
plastic package

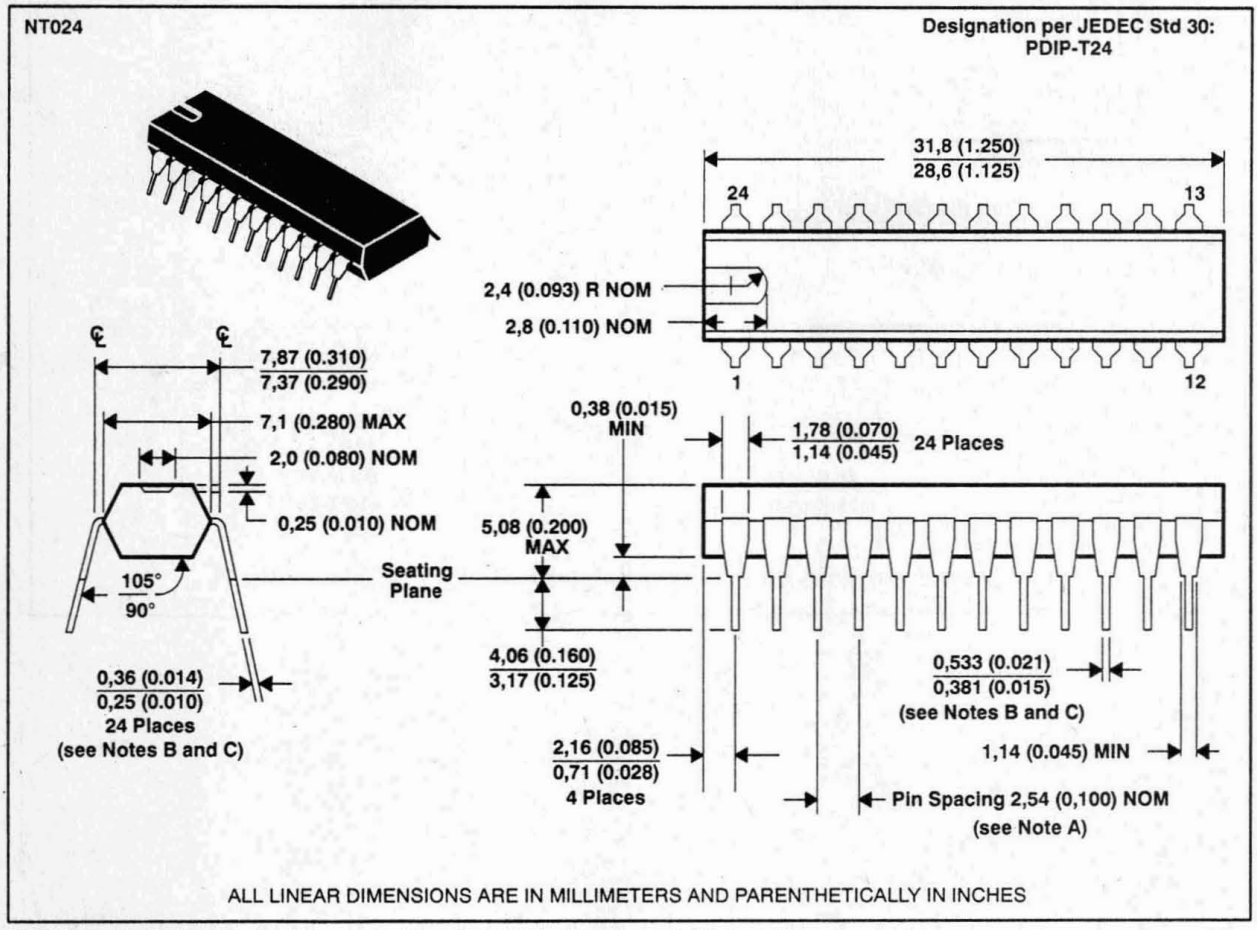
This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound withstands soldering temperature with no deformation, and circuit performance characteristics remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



NT024
300-mil plastic dual-in-line packages

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics will remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers . Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin package, the letter N is used by itself since the 24-pin package may be available in more than one row-spacing. For the 24-pin package, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.



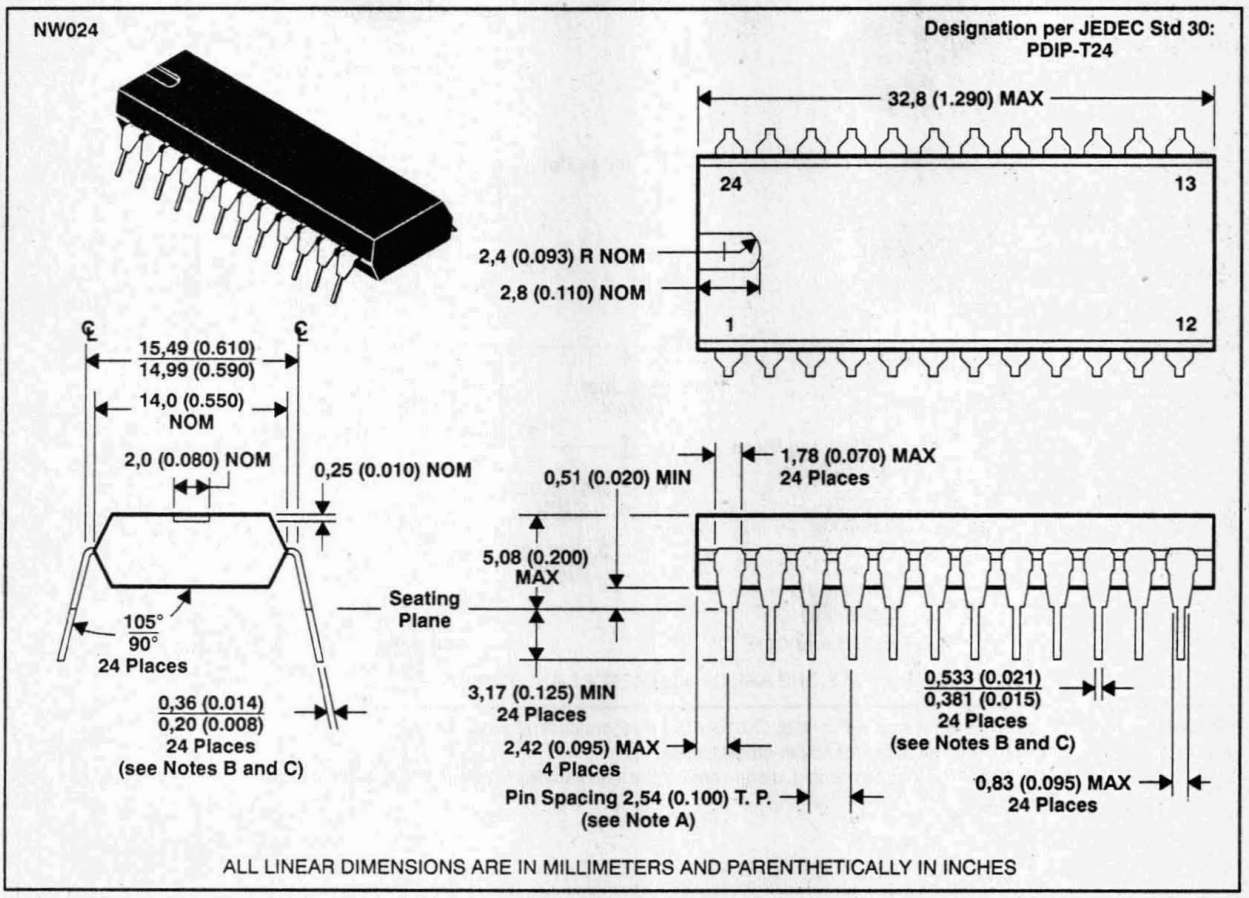
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

NW024
600-mil plastic dual-in-line package

This dual-in-line package consist of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics will remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 15,24 (0.600) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin packages, the letter N is used by itself since only the 24-pin package is available in more than one row-spacing. For the 24-pin package, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.

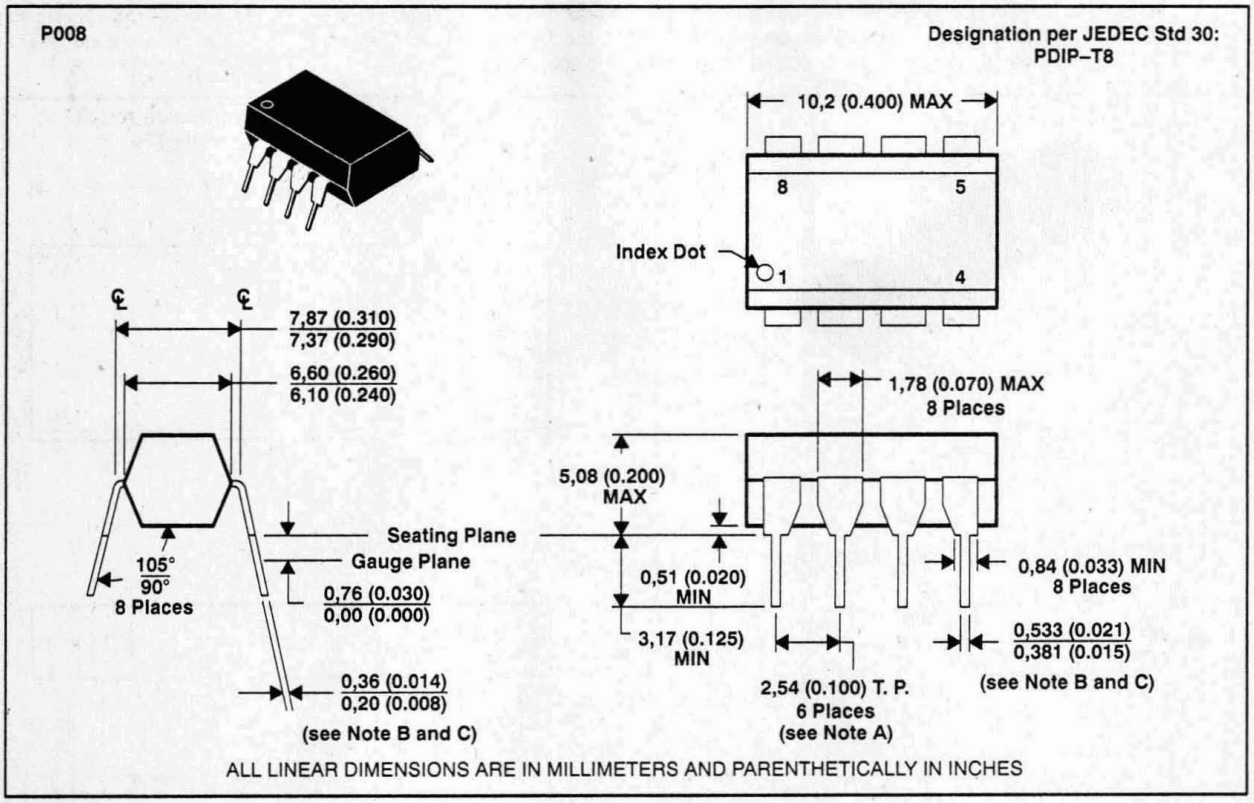


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

P008
plastic dual-in-line package

This package consists of a circuit mounted on an 8-pin lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Solder-plated lead require no additional cleaning or processing when used in soldered assembly.



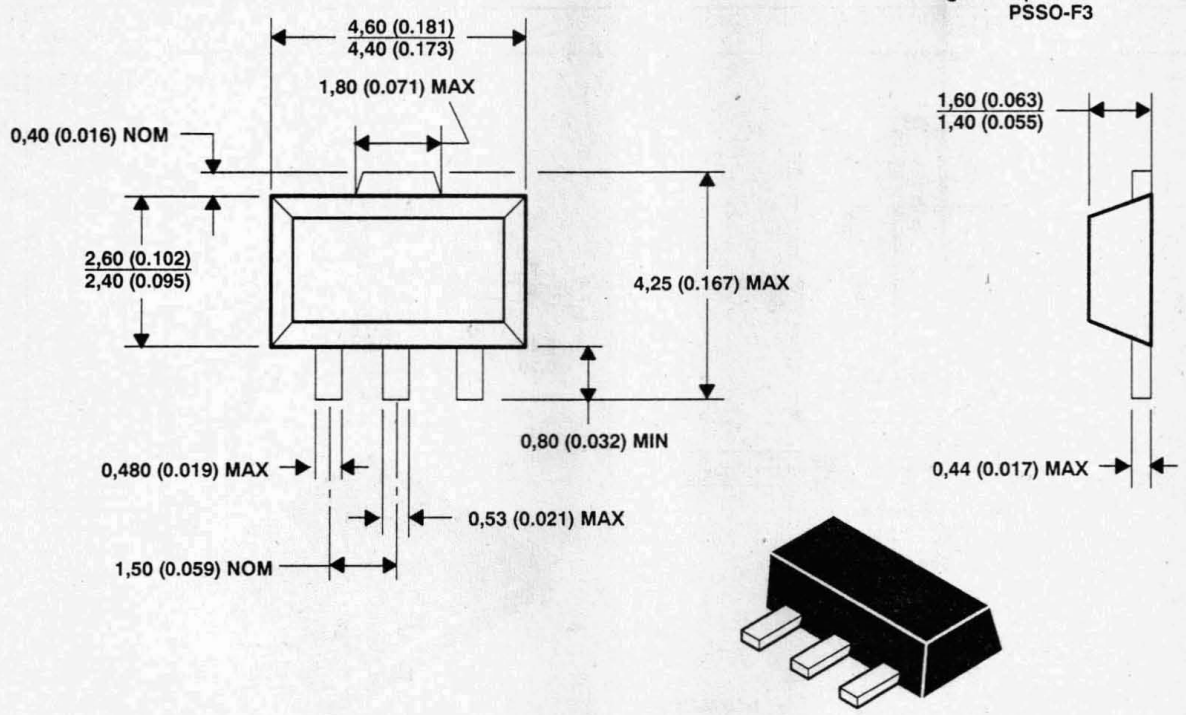
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

PK003
plastic lead-mount package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions.

PK003

Designation per JEDEC Std 30:
PSSO-F3

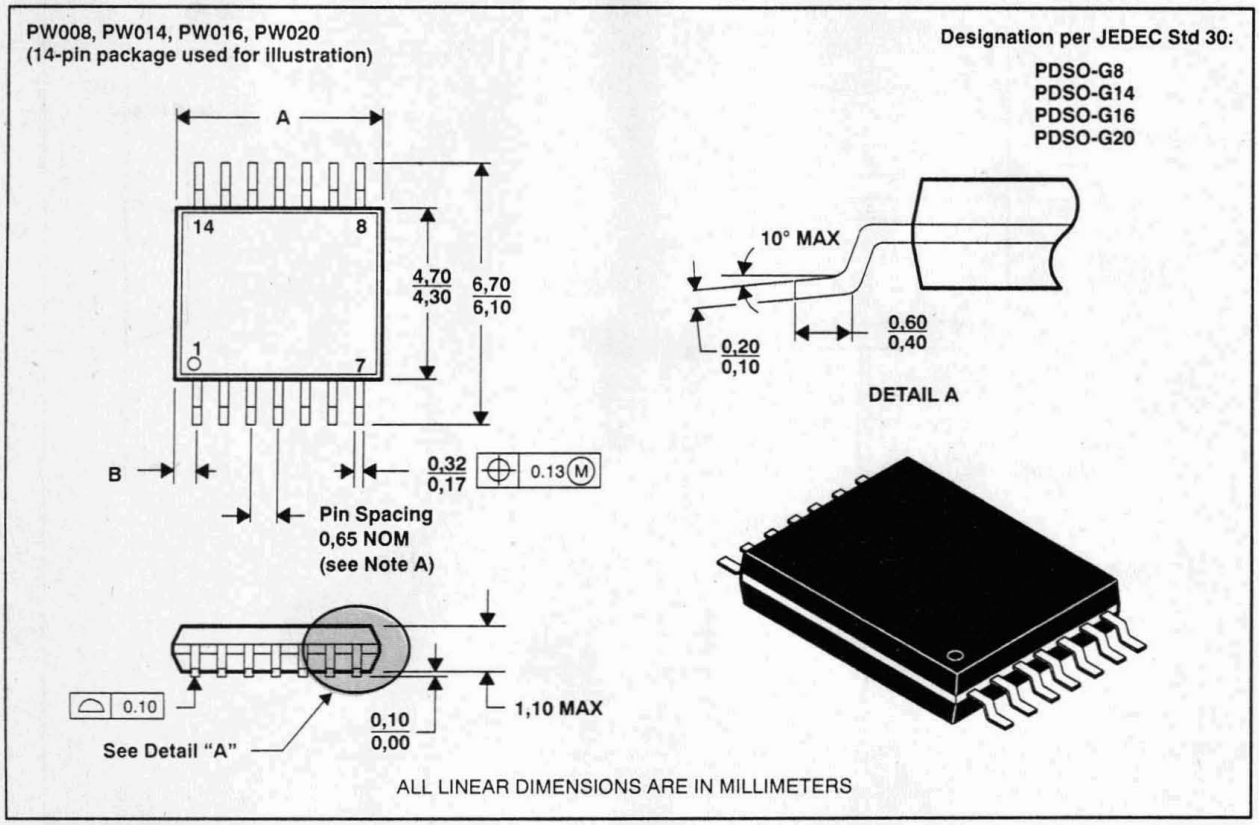


The center lead is in electrical contact with the tab

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

PW008, PW014, PW016, PW020
shrink small-outline packages

These shrink small-outline packages consist of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

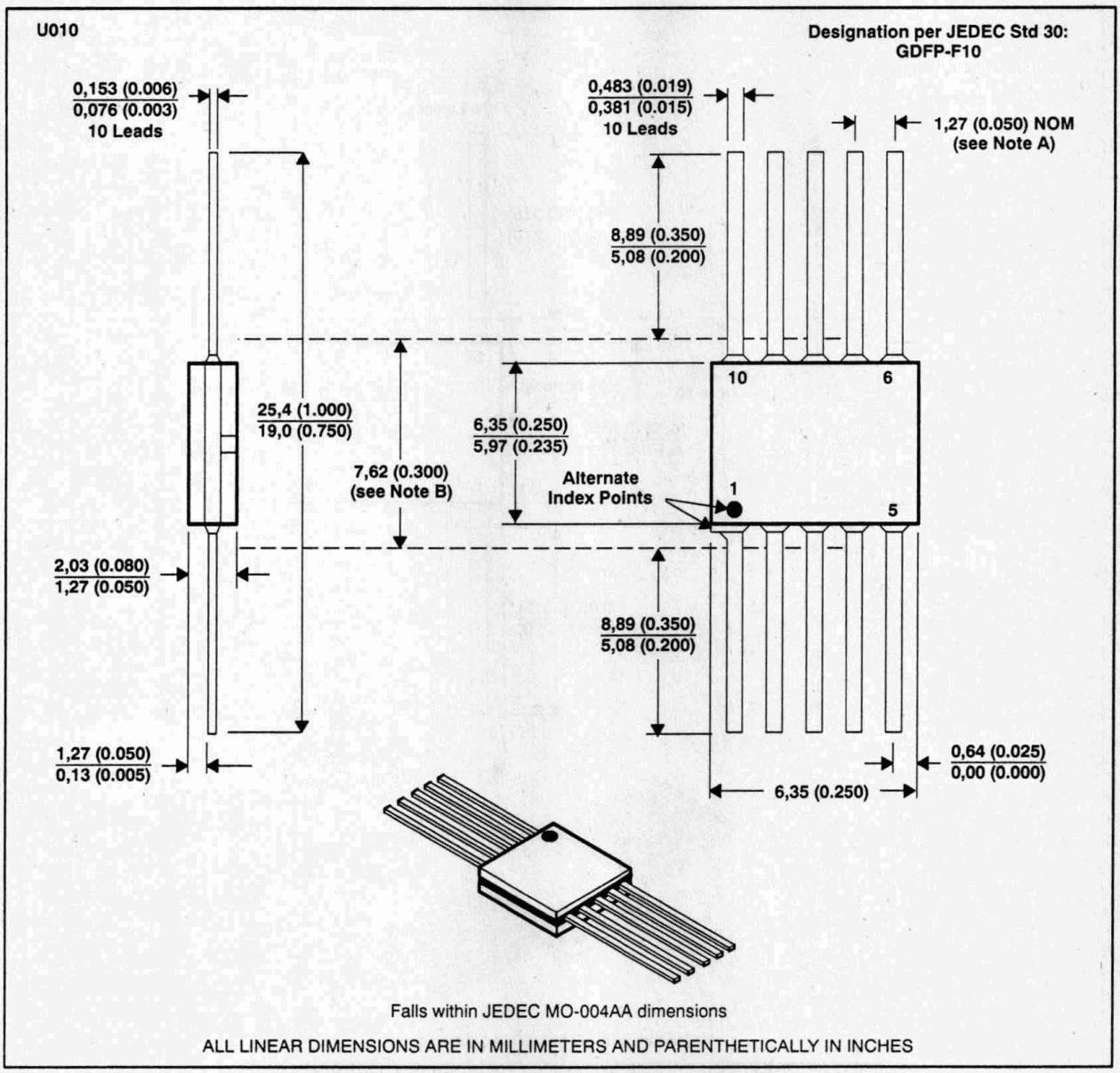


NOTES: A. Leads are within 0,25 mm radius of true position at maximum material condition.
B. Body dimensions include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 mm.
D. Lead tips to be planar within ±0,051 mm exclusive of solder.

DIM \ PINS	8	14	16	20
A MIN	2,99	4,99	4,99	6,40
A MAX	3,03	5,30	5,30	6,80
B MAX	0,65	0,70	0,38	0,48

U010
ceramic flat package

This flat package consists of a ceramic base, ceramic cap, and lead frame. Circuit bars are alloy mounted. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.



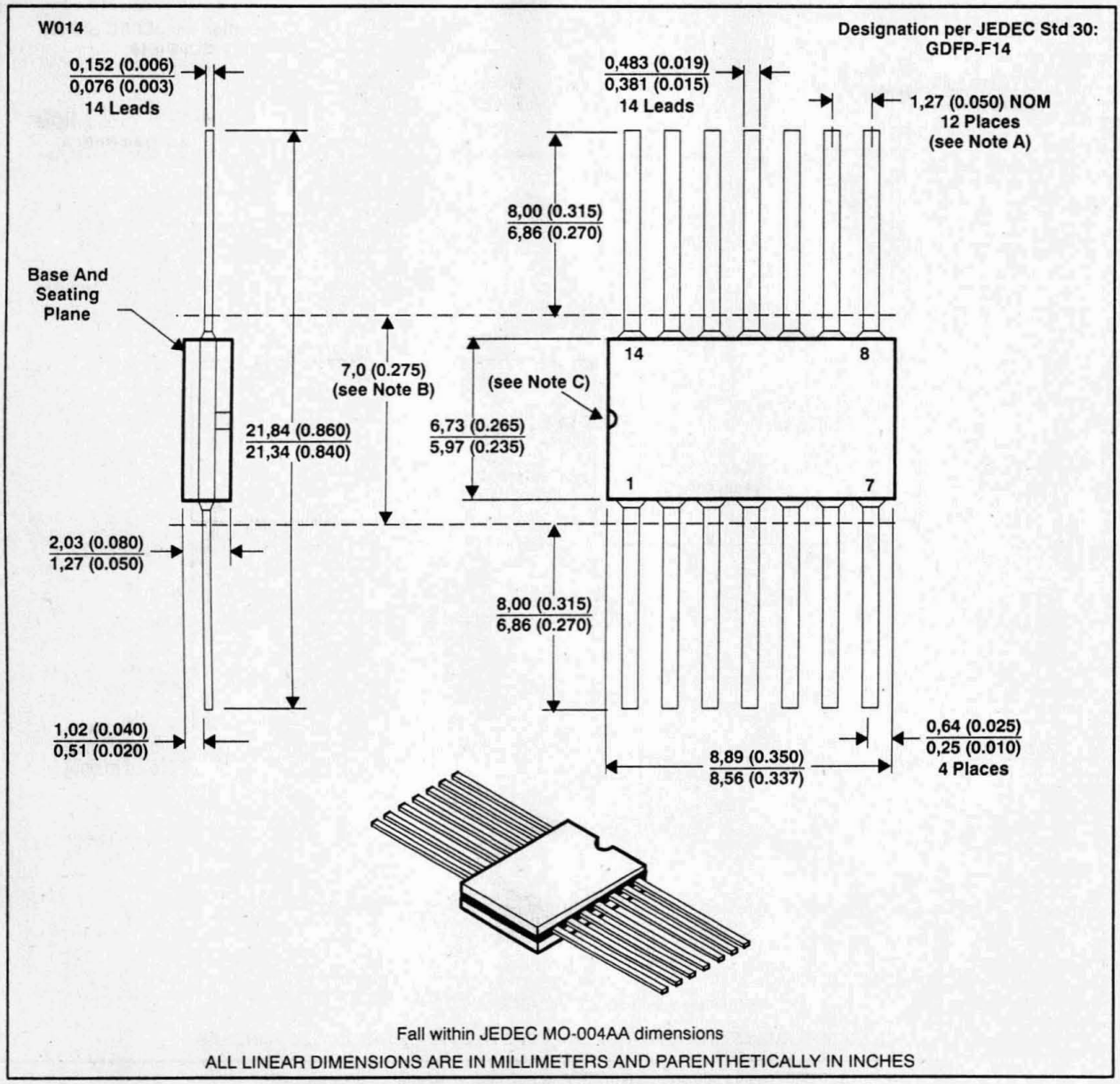
Falls within JEDEC MO-004AA dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material conditions.
B. This dimension determines a zone within which all body and lead irregularities lie.

W014
ceramic flat package

This hermetically sealed flat package consists of an electrically nonconductive ceramic base and cap and a lead frame. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.



Fall within JEDEC MO-004AA dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material condition.
B. This dimension determines a zone within which all body and lead irregularities lie.
C. Index point is provided on cap for terminal identification only.

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